

Yield Improvement, Fault-Tolerance to the Rescue?

J. Vial A. Bosio P. Girard C. Landrault S. Pravossoudovitch A. Virazel

Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier – Université Montpellier II / CNRS
 161, rue Ada 34932 Montpellier – France

Email: {vial, bosio, girard, landraul, pravo, virazel}@lirmm.fr URL: http://www.lirmm.fr/~w3mic

Abstract

With the technology entering the nano dimension, manufacturing processes are less and less reliable, thus drastically impacting the yield. A possible solution to alleviate this problem in the future could consist in using fault tolerant architectures to tolerate manufacturing defects. In this paper, we analyze the conditions that make the use of a classical Triple Modular Redundancy (TMR) architecture interesting for a yield improvement purpose.

1. Introduction

To increase the yield for future VLSI systems, fault tolerant architectures have been proposed as a potential solution [1]. Fault tolerant architectures are commonly used to tolerate on-line faults, *i.e.* faults that appear during the normal functioning irrespective of their transient or permanent nature [2]. In the near future, fault tolerant architectures could also be used to tolerate permanent defects due to an imperfect manufacturing process.

Fault tolerant architectures use redundancies. Redundancy is the property of having more resources than needed to perform a given function. They are generally classified depending on the type of redundant resources. Basically four types of redundancy are considered: hardware, software, information and time [3].

In this paper, we consider hardware redundancy to achieve yield ramp-up benefits since we consider manufacturing process defects. Hardware redundancy consists in modifying the design by adding extra hardware. For example, instead of having a single processor, we can use three processors, each performing the same operation. The failure of one processor is tolerated thanks to a voter that chooses the majority outputs. This is the basic principle of TMR architectures [3].

In the rest of this paper, we study the potential use of a TMR architecture for tolerating manufacturing defects and hence improve the yield.

2. The TMR approach

A TMR structure is a fault tolerant architecture based on three identical modules performing the same function. Their inputs receiving the same data are tied together, and their outputs feed a majority voter (V) circuit as shown in Figure 1. As a result, the TMR architecture significantly reduces the error probability at the primary outputs of the system. A defective module propagating an erroneous value can be masked thanks to the presence of the two other fault-free modules.

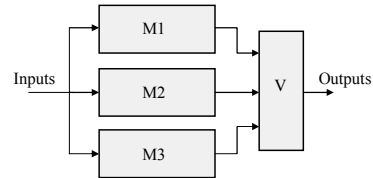


Figure 1: TMR principle

Basically, a TMR architecture can tolerate one defect but in practice it can tolerate more than one defect. To be not tolerated, two defects must be located in two different modules and then propagate an error towards identical outputs on each module. Let P be the input pattern, Ω_i be the set of erroneous outputs in module i due to the first defect when P is the input ($i = 1, 2, 3$) and Ω_j be the set of erroneous outputs in module j due to the second defect when P is the input ($j = 1, 2, 3$). Under these constraints, defects tolerance is formalized as follows:

- If $i = j$, defects are tolerated.
- If $i \neq j$ and $\Omega_i \cap \Omega_j = \emptyset$, defects are tolerated.
- If $i \neq j$ and $\Omega_i \cap \Omega_j \neq \emptyset$, defects are not tolerated.

In Figure 2, two examples are shown with the same pattern P feeding the three modules. The voter has been omitted. Each defect is modeled as a stuck-at fault (f_1 and f_2 respectively).

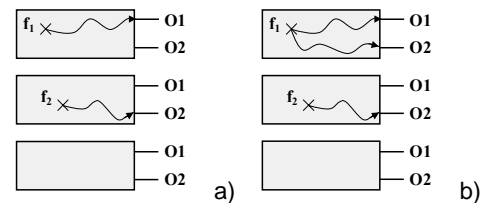


Figure 2: Tolerance of two stuck-at faults
 a) tolerated and b) not tolerated

In the case of Figure 2.a, f_1 is propagated towards O1 in the first module and f_2 is propagated towards O2 in the second module. The majority voter receives two correct values and one wrong value. The outputs of the TMR are therefore correct and faults f_1 and f_2 are tolerated. In the case of Figure 2.b, f_1 is propagated towards O1 and O2 while f_2 is propagated towards O2. The voter receives one wrong value for O1 and two wrong values for O2. So, the value on the second output of the TMR is faulty. Faults f_1 and f_2 are not tolerated.

Consequently, two stuck-at faults are tolerated when there is no pattern able to propagate errors coming from the two faults in different modules toward identical outputs in each module. In the case of more than two defects, multiple

defects can be handled by considering all the possible fault couples between them.

3 A TMR structure for yield improvement

In this section, we investigate the interest in producing the TMR version of a circuit, instead of its single version, in order to tolerate manufacturing defects and consequently improve the yield. We therefore analyze the conditions that have to be fulfilled to achieve benefits in implementing a TMR architecture.

For our analysis, we consider that the voter area is negligible. Thus, if we triplicate a circuit to implement a TMR architecture on a given silicon area S, we can have N TMR circuits having a yield equal to η_{TMR} ($\eta_{TMR} \times N$ fault-free circuits) or $3N$ circuits (without redundancy) having a yield equal to η_c ($\eta_c \times 3N$ fault-free circuits). A tolerant TMR architecture is worthwhile only if:

$$\eta_{TMR} \times N > \eta_c \times 3N \quad \text{with} \quad \eta_{TMR} \leq 1 \quad \text{and} \quad \eta_c \leq 1$$

Consequently:

$$\eta_{TMR} > 3 \times \eta_c \quad \text{with} \quad \eta_c \leq 1/3 \quad (1)$$

First of all, due to Eq. 1, it is important to notice that a TMR architecture can be profitable only if $\eta_c \leq 1/3$, i.e. when a low manufacturing yield is expected due to the use of aggressive nanotechnologies.

Let us now compute η_{TMR} and η_c by using the Poisson distribution. It would not be completely accurate to use the Poisson distribution for large circuits due to clustering effects on defects [4], but for a first and rough evaluation this is reasonable. In our case, the Poisson distribution is a discrete probability distribution that defines the probability that a number of manufacturing defects occur in a fixed area if these defects occur with a known probability.

Let X be the number of manufacturing defects and λ be the average number of expected defects for a given silicon area. Then, $\lambda = n \times p$ with n being the number of logic gates (or transistors) and p the average defect rate of a gate (or a transistor). Let $P\{X=k\}$ be the probability that the structure has k manufacturing defects. If n is high and p is low, the binomial distribution becomes the Poisson distribution:

$$P\{X=0\} = e^{-\lambda} \times (\lambda^k / k!) \quad (2)$$

The presence of a fault makes the entire system faulty. So, η_c is the probability that there is no defect inside the circuit:

$$\eta_c = \underbrace{P\{X=0\}}_{\text{Probability that there is no defect}} = e^{-\lambda} \times (\lambda^0 / 0!) \Leftrightarrow \eta_c = e^{-\lambda} \quad (3)$$

Probability that there is no defect

Let R be the probability that two defects are tolerated. The yield of the TMR structure η_{TMR} is thus given by:

$$\eta_{TMR} = P\{X=0\} + P\{X=1\} + R \times P\{X=2\} + R^2 \times P\{X=3\} + \dots$$

2 defects are equivalent to 1 couple of defect
3 defects are equivalent to 3 couples of defects ... etc

$$\Leftrightarrow \eta_{TMR} = e^{-\lambda_{TMR}} \times \left(1 + \lambda_{TMR} + R \frac{(\lambda_{TMR})^2}{2!} + R^2 \frac{(\lambda_{TMR})^3}{3!} + \dots \right)$$

There are three times more gates (or transistors) into a TMR architecture than into a non-redundant circuit. So, by substituting λ_{TMR} by $3\lambda_c$ we obtain:

$$\Leftrightarrow \eta_{TMR} = e^{-3\lambda_c} \times \left(1 + 3\lambda_c + \sum_{i=2}^{\infty} R^i C_i^i \times \frac{(3\lambda_c)^i}{i!} \right)$$

and with $\eta_c = e^{-\lambda_c} \Rightarrow \lambda_c = -\ln \eta_c$

$$\eta_{TMR} = e^{3 \ln \eta_c} \times \left(1 - 3 \ln \eta_c + \sum_{i=2}^{\infty} R^i C_i^i \times \frac{(-3 \ln \eta_c)^i}{i!} \right) \quad (4)$$

A TMR architecture will improve the resulting yield if $\eta_{TMR} > 3\eta_c$. Figure 3 gives η_{TMR} as a function of η_c for different values of the R probability. The bold dotted line represents the condition $\eta_{TMR} > 3\eta_c$. From Figure 3, it appears that the condition is satisfied only for values of R greater than 92.58%.

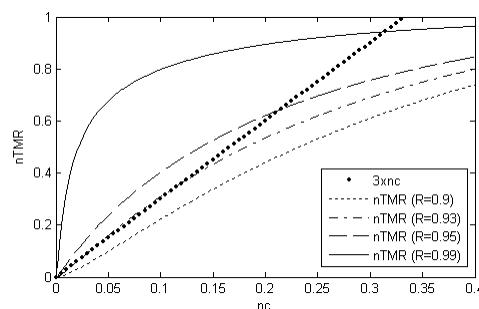


Figure 3: η_{TMR} as a function of η_c

To summarize, implementing a TMR architecture for a given circuit can improve the yield if i) the yield of the non-tolerant circuit is lower than 33.33% and ii) the percentage of tolerated fault pairs using a TMR architecture is greater than 92.58%. A question is still open concerning the meaning of 92.58% value of R. In order to answer this question we will investigate test issues related to TMR architectures.

Consequently, our future work will consist in proposing a test method able to deal with TMR architectures in order to evaluate the percentage of tolerated fault pairs (R probability) on a set of benchmark circuits. These evaluations are mandatory to demonstrate the interest of using TMR architectures for yield improvement purpose.

References

- [1] L. Fang and M. S. Hsiao, "Bilateral Testing of Nano-scale Fault Tolerant Circuits", Proc. of Defect and Fault Tolerance in VLSI Systems, pp. 309-317, 2006.
- [2] C. E. Stroud and A. E. Barbour, "Design for Testability and Test Generation for Static Redundancy System Level Fault Tolerant Circuits", Proc. of Int. Test Conf., pp. 812-818, 1989.
- [3] I. Koren and C. Krishna, "Fault Tolerant Systems", Morgan Kaufman Publisher, 2007.
- [4] Y. Gagnon et al., "Are Defect-Tolerant Circuits with Redundancy Really Cost Effective? Complete and Realistic Cost Model", Proc. of Defect and Fault Tolerance in VLSI Systems, pp. 157-165, 1997.