



Neutron Detection through an SRAM-Based Test Bench

Luigi Dilillo¹ Frédéric Wrobel² Jean-Marc Galliere¹ Frédéric Saigné²

¹ *Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier – LIRMM
Université de Montpellier II / CNRS
161, rue Ada – 34392 Montpellier Cedex 5, France
Email: <lastname>@lirmm.fr URL: <http://www.lirmm.fr/~w3mic>*

² *Institut d'Electronique du Sud
Université de Montpellier II / CNRS
Place Eugène Bataillon - 34095 Montpellier CEDEX 5, France
Email: first_name.last_name@ies.univ-montp2.fr URL: <http://www.cem2.univ-montp2.fr>*

Abstract

In this paper, we propose a technique for the detection of neutrons that relies on the sensitivity of SRAM cells to particle radiation. In particular, we introduce a system based on a memory test bench that records the neutron reactions in the memory array. This system allows a good flexibility from different points of view. It is conceived to be modular, programmable, low power consuming and portable. Consequently, it can operate in various experimental conditions such as under artificial sources of particles as well as in natural ambience, from the earth surface to spatial environment. The system is also independent of the type of memory, allowing the use and the study of the interaction between particles and electronic devices built with different technologies.

1. Introduction

Nowadays, one of the main concerns in microelectronics is the robustness of CMOS integrated circuits in relation to radiation effects. SRAM memories function can be seriously compromised by particle impacts, resulting in malfunctions of whole IC systems and in particular Systems on Chip (SOCs), where memories almost monopolize the overall surface (>80%), as shown by the ITRS roadmap for semiconductors [1]. In fact, in radiative environment, the SRAM memory presents certain likelihood to failure with unexpected bit flip of one or multiple cells. The bit flip is often related to the impact of cosmic rays [2]. Besides, with the continual miniaturization of transistors this event begins to appear at the ground level, where the event of particles collision is less probable than commercial aircraft altitude or spatial environment. The scaling rate and memory predominance in SOC increases significantly at each technology generation and imposes the industry to consider the effect of radiative natural environment on devices and circuits.

In some cases, the radiation sensibility of memories could be considered as a benefit. For example, memories could be used as neutron detector either in natural environment or under beam of particles. To do so, it is

firstly required to have a test bench able to detect every bit flip in the memory.

In natural environment the memory bit flips due to neutron collision have a weak rate of occurrence. In a 90nm SRAM, the rate of such bit flips is around a few hundreds per billion hours and per Mbit [3]. In order to quantify the reliability under radiation of a given components it is necessary to maximize the number of events by unit of time, i.e. to associate a large number of memories, increasing the active surface of the sensor and the number of cell devices. In this work, we conceived an innovative memory test bench with the aim to allow its employ in the most various environments, such as under artificial neutron sources or in natural environment at different altitude and latitude. For this purpose, the proposed design and architecture is modular (variability of number of memory elements), reduced dimension (easy to embed) and low power consuming.

The deal between power consumption constraints, good coverage of bit flips and optimal test bench flexibility (modular elements, programmable on line test algorithms, remote system control and test data acquisition) is a challenging matter. The solution that we propose is based on the use of an original architecture element: the BOBST (Built-On-Board Self-Test). Differently from BIST (Built-In Self-Test) where each circuit has its own embedded test circuitry, the BOBST can manage the test of a set of memories at board level. Besides reducing the consumption, this method offers the advantage to allow the boarding of standard memories and by consequence to allow the implementation and exploration of various technologies. For optimizing the power consumption, all groups of memories are driven by a single scheduler. This element has the functions of planning the test, regulate the power consumption in relation with the power at disposal, storage and test data transmission.

The rest of the paper is organized as follows. Section 2 gives some notions of natural radiative environment in atmosphere. In section 3, the SRAM core-cell is presented as well as its failure due to neutrons. In Section 4, the test bench architecture is presented. Conclusions are given in Section 5.

2. Radiation and nanoscaled electronics

Radiation is today not only a constraint to be taken into account for component function but a veritable threat to further technological downscaling. In fact, nowadays, ionizing radiation has become an intrinsic constraint for nanoscaled electronics. Because of nanometric circuit dimensions, the multitude of used materials, and the charge reductions in each operation, simple natural radiation is enough to make the devices unreliable. For the use of electronics in natural environment, the constraint that we consider at moment is atmospheric or terrestrial. Because of the stars and especially the Sun, the Earth is continually bombarded by cosmic rays. These cosmic rays are at the origin of major electronic reliability issue at terrestrial sites and at aircraft altitude, especially for very scaled electronic devices [1], [4], [5]. Through interactions between those cosmic rays and the atoms of the atmosphere, particles like neutrons, protons and electrons are released in the atmosphere from earth to tenth of kilometers of altitude, as shown by the graphic in Figure 1.

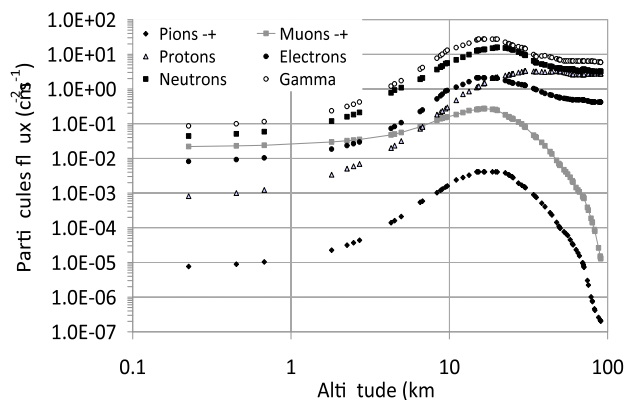


Figure 1- Total flux of particles in the atmosphere with the altitude [6].

Not all those particles are critical for the electronic device reliability. Until today, only neutrons, which are the most abundant, have been shown to induce failure on devices. For computer's memories, one of the main concerns is the Single Event Upset (SEU) that corresponds to a bit flip due to a single particle [4].

Neutrons flux varies with altitude and latitude. The increase of the neutrons flux with the altitude [7] is shown in Figure 2. A factor of 420 is reached between ground level and high altitude (20 km). Electronic involved in avionics has been the first to be concerned with neutrons but, with downscaling, applications at ground level are now concerned (automotive for instance).

The neutron flux variation with the latitude is reported in the graphic in Figure 3 for a fixed altitude of 19 km (NASA-Langley model [7]).

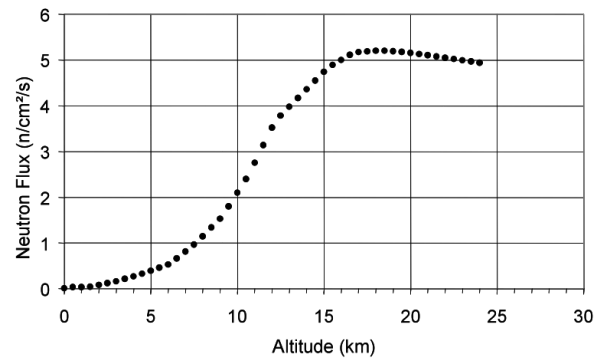


Figure 2 - Neutrons flux in atmosphere as function of altitude –at latitude of 45°- (NASA-Langley model [7]).

On field measures have shown that the neutrons flux at pole is five times larger than at the equator latitude, for a fixed altitude.

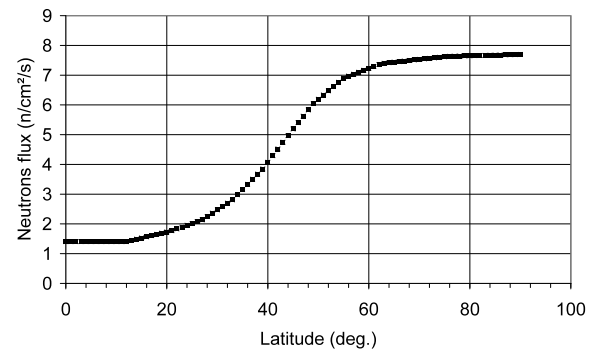


Figure 3 - Neutrons flux in atmosphere as function of latitude - at altitude of 19 km - (NASA-Langley model [7])

For reliability purpose, the determination of the SEU Rate, called SER (Soft Error Rate), is crucial. Cosmic rays cannot be shielded and the knowledge of the failures for a given device or technology is a fundamental requirement for production of correct electronic designs (e.g. aircraft, car, train production).

There are two methods to estimate the SER: electronic testing and the use of calculation codes.

Concerning the electronic test, the experiments can be run at *real time* and with *accelerated test*. For neutron detection, the real time test is commonly done by placing the device to test (memory) in real conditions either at ground level or at the top of a mountain [8], where the particles are more abundant [7], see Figure 2. The main drawback of such a method is that it is time consuming (experimentation time of one year or more) even in mountain. On the other hand real time test remains the best way to perform representative test. During accelerated tests, the component is put under a particle beam (neutron in our case, but also proton or ions). The conditions of the beam are linked to the natural ones and the error rate can be estimated [7], [9]. The accelerated test has three main drawbacks. Firstly, the beam cost is high for a systematic study. Secondly, it is necessary to book the beam generator long time (several months) before the experiments. The third drawback is that the link between the beam and the natural environment is

not well known and defined. Consequently, the method may not provide reliable results.

Considering calculations (*i.e.* prediction), the aim is to determine the error rate of a given device by using some models describing the radiation effects on a device [10-12].

Considering what exposed above, we have decided to produce an SRAM memories test bench for neutron detection, intended to be flexible enough to be placed in several environments. In this direction, in the next section, we analyze the interaction between neutrons and SRAM cell with more detail.

3. SRAM core-cell

The neutron sensor that we present is based on the capability of SRAM memories to record the nuclear reactions induced by a neutron. In particular, the record mechanism is due to the memory cell swap due to parasitic currents produced with the collision. For this reason, we first detail the SRAM core cell function and after its interaction with neutrons. Figure 4 depicts a typical six-transistor SRAM cell in CMOS technology. The circuit consists in a flip-flop comprising two cross-coupled inverters and two access transistors Mtn3 and Mtn4.

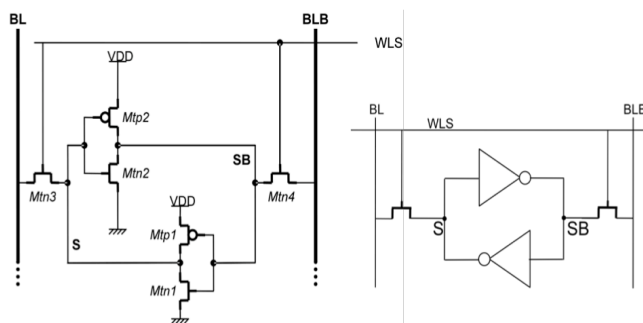


Figure 4 – Schemes of the six-transistor SRAM cell

The access transistors Mtn3 and Mtn4 are turned on when the word line is selected and its voltage raised to VDD, and they connect the flip-flop to the column lines BL and BLB, for read or write operation. When the cell stores a '1', node S is high at VDD, and node SB is low at '0' (0V). Node S is kept at '1' through the pulling up action of transistor Mtp1 (Mtn1 is OFF), while node SB is kept low through the pulling down action of transistor Mtn2 (Mtp2 is OFF). When the cell stores a '0', node S is at '0' and node SB is at '1'. In this case, the transistors of the two inverters are in the opposite operational state than '1' was stored. Here, we will not detail read and write operations on the cell, but we only underline the fact the only correct way to change the storage data ('1' or '0') is through a write access of the cell. All other phenomena that lead to a cell swap, such as data retention fault or single event swap due to a particle collision, have to be considered malfunction.

3.1 Neutron impact on SRAM core-cell

Let us now consider the failure mechanism in SRAM core-cell. Generally in memories, the SEU corresponds

to an unexpected bit flip of the core-cell due to a single particle. During the interaction of a neutron with the matter of an electronic device, many secondary ions can be produced with variable energies. Such ions will then produce further ionization along their path, as depicted in Figure 5.

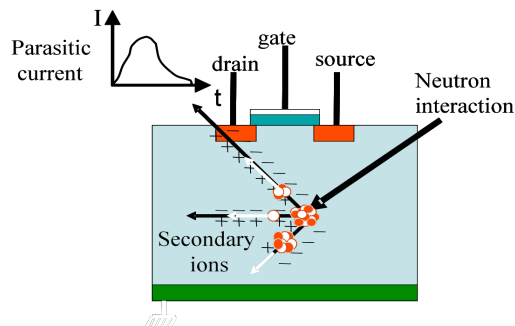


Figure 5 - Nuclear reaction inducing secondary ions. Secondary ions create electron-hole pairs along the ion track. Carriers are collected by the device electrodes leading to a parasitic current.

The knowledge of the kind of secondary ions that are produced is needed to evaluate the energy deposited in a component. In the radiation effect community, different nuclear codes are used [13-14]. Secondary ions create electron-hole pairs along the ion track, those charge carriers are then collected by transistor electrodes leading to a parasitic current in the device. If the transistor to be hit belongs to a memory cell and the parasitic current intensity and duration are large enough, the cell may swap (changing the stored data), recording the neutron reaction. The cell swap is described in detail in Figure 6, for a cell in hold state, *i.e.* the cell holds the stored vale and it is not accessed for read/write operation.

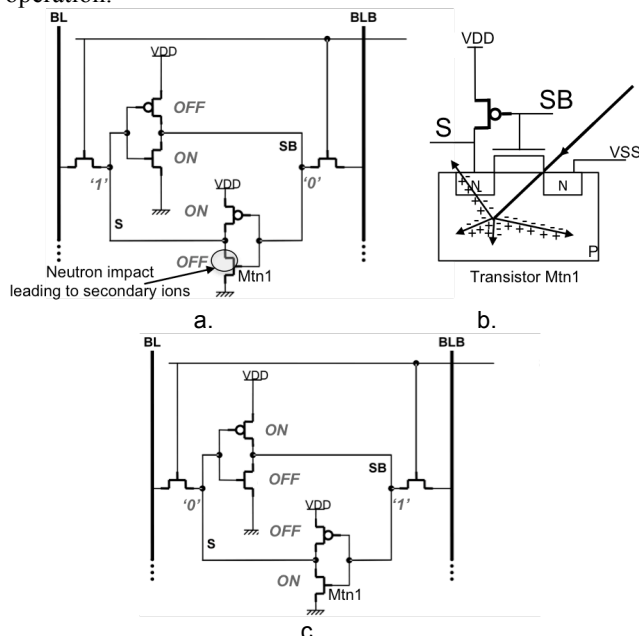


Figure 6 – a. Pre-impact state of the cell storing '1'. b. Incident neutron interacting with Mtn1 transistor in OFF state leading to parasitic currents. c. Node S voltage drops provoking the cell swap (new value stored '0')

As Figure 6.a shows, the cell stores a '1', thus node S is a '1' (VDD) and node SB is at '0' (VSS). The cell is not accessed, thus the pass transistors Mtn3 and Mtn4 are OFF and isolate the two-inverter loop that store the data. In particular, with reference to the scheme in Figure 4, transistors Mtp2 and Mtn2 are OFF, while transistors Mtn2 and Mtp1 are ON. With this state if the cell, the two main sensitive areas for the SEU are the drains of the two transistors in state OFF that are located in the refresh loop of SRAM, and in particular the NMOS in OFF state [15]. In fact, the probability for an SEU occurrence increases when the ion tracks are close to those transistor electrodes, because the parasitic current will be more important. As depicted in Figure 6.b, the incident neutron interacts with the device materials of NMOS transistor Mtn1 (in OFF state), producing secondary ions. At this stage, electron-hole pairs are produced, leading to a parasitic current in correspondence of the drain electrode. Such a current may discharge cell node S, which was at VDD. If the voltage drop of node S is important in value and duration the upper inverter (Mtn2 and Mtp2) will force a '1' on node SB, causing a faulty swap of the cell.

When high level of robustness is required, in operational environments with abundant particle impacts (high latitudes, commercial aircraft altitude, nuclear power stations), Error Correcting Codes (ECCs) may reduce the malfunctions due to cell swaps. This mitigation technique is then today widely used to protect SRAMs despite the inherent strong area and power penalties. The most used algorithm, because the less costly, corrects one single error and detects two errors in a bit-word. The efficiency of this algorithm (known with name of Single Error Correction /Double Error Detection) can be extremely high, detecting almost all soft errors, revealing that SEUs come from single strikes. This condition is likely to be unsatisfied in a close future with the occurrence of a new failure mode as the Multiple Bit Upset (MBU) [16-19]. MBU is defined as several adjacent simultaneous bit swaps due to a unique particle hit or to several secondary ions. The MBU is due to the ever-increasing SRAM integration with technology downscaling.

4. Detecting neutrons through SRAM

In this section, we describe the principles of the architecture of the SRAM test bench as well the test strategies. We also explain the choices that have been made in order to improve test bench functionalities as well as the possibility to place it in different environments.

4.1 The test bench architecture

As exposed in the previous section, in natural environment, at ground level or at high altitude in atmosphere, the occurrence of nuclear reactions followed by memory failure is very low in time scale. For this reason, in order to reduce the experimental time, it is likely to run the test in the best conditions, for example by choosing the test place richer in neutrons.

On the other hand, we can increase the probability of collision (reducing the test time) extending as much as possible the number of devices (thus the sensible surface, number of memory cells) under test. For our experimentation, we will employ about 250 4Mbit stand-alone SRAM devices for a total amount 1 Gbit. Another choice that we have done is that the circuits under test should not present any BIST (Built In-Self Test) feature. This choice forces the use of externally generated test vectors. The result of this choice is the introduction of an electronic device called BOBST (Built On-Board self Test). The BOBST represents a test generator placed on the same board of the memories. This test pattern generator can be programmed, allowing the operation of various test strategies and the use of different types of memory device and technology.

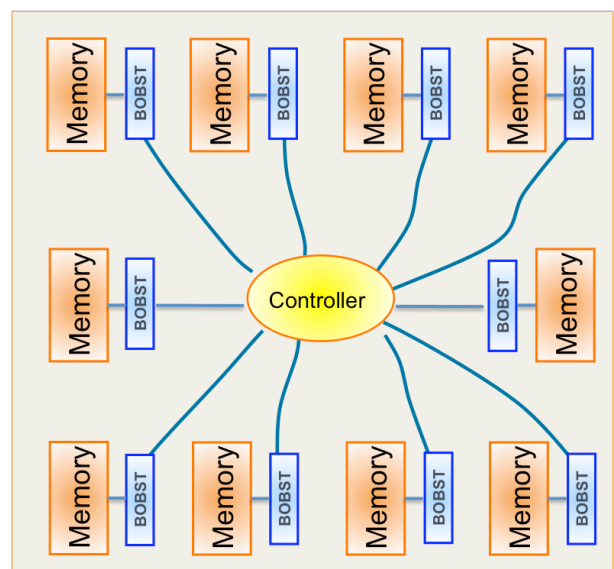


Figure 7 – First implementation scheme for the memory test bench

A first implementation scheme that we have considered is shown in Figure 7. In this scheme a central control unit administrates the overall test bench, collects all the test failure data, rules the input/output data communication. Each memory device is connected to one BOBST. The power management is made by the control unit, which may decide to run the test on all devices, or in case of lack of power reduce the number of devices under test. This implementation scheme is functional, but it cannot be used for a large number of memories, because of the amount of devices (memories and BOBST) and wiring that need to be on the same board.

For this reason, we have elaborated an evolution of the previous scheme that presents modular features. The new implementation scheme is depicted in Figure 8. The second test bench implementation presents the memory elements distributed in independent subsystem modules composed of four memory chips connected to a single BOBST.

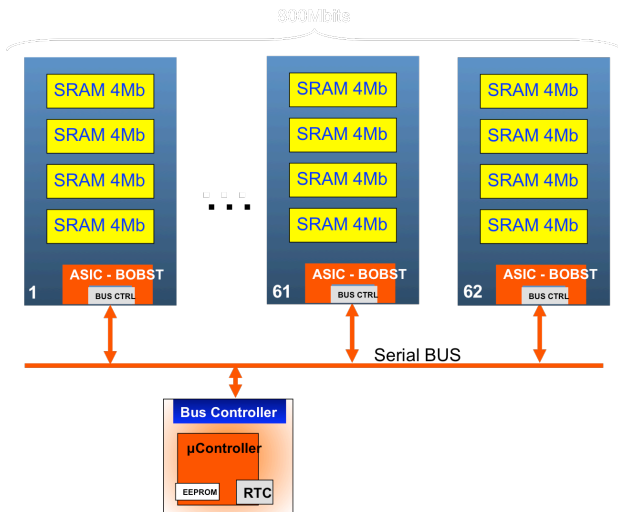


Figure 8 – Second implementation scheme for the memory test bench

Each subsystem is connected to a central control unit through a serial bus, which is similar to the BUS CAN currently used in automotive domain. The choice of the serial bus is due to the constraint to reduce the power consumption (~1W overall) and the wiring. Another reason of the choice of serial bus is the limited amount of data that circulates on the bus:

- Subsystem module diagnostics information
- Enabling signals for switching OFF and ON the subsystems for power consumption strategies or for detected malfunctions
- Reprogramming the test algorithms operated by the BOBSTs.
- Storage of test failure data
- Test failure data from subsystems and central control unit

The quantity of test failure data that passes through the serial bus is not large because, as mentioned above, SEUs are not particularly frequent in natural environment. The collection of test failure data is made with a periodic polling of all subsystems, on the base of *round robin* principle.

This implementation scheme allows a higher degree of flexibility than the previous one, because the test strategy adopted on one module is independent from the other modules. Adaptive power strategies can be operated, switching OFF and ON part of the modules. Moreover, the whole system is modular because the number of modules is not fixed, but it can be decided to at any moment in relation with power, weight and space constraints.

Concerning the subsystems, the local control action is made by the BOBST device, which has multiple functions:

- Test patterns generation
- Test sink
- Storage of test failure data
- Transmission of test failure data to the central control unit
- Subsystem diagnostics

At this stage of the project, we have produced a first subsystem prototype, which is shown in Figure 9.

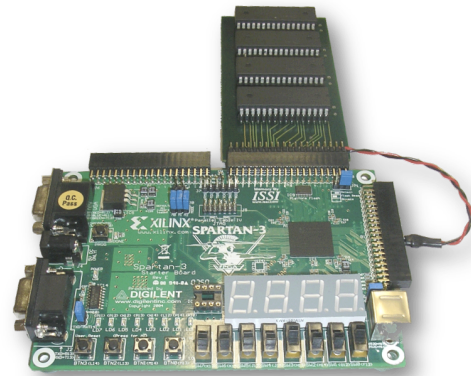


Figure 9 – Photography of a prototype subsystem module

This first prototype is composed of two elements: a board with four 4Mbit stand-alone SRAMs (on the top side of Figure 9), a programmable device (FPGA) in which we have implemented the functions of the BOBST. In the following prototype, the BOBST will be implemented in a dedicated ASIC circuit, in which the function will be performed by redundant circuitry, in order to reduce the possibility of failures in vector generation and test response verification. An improved version of the first prototype will be employed for memory and test characterization, with the use of a controlled artificial source of neutrons. For this operation, one module is sufficient because of the large number of neutron collisions warranted by the artificial source.

4.2 Test strategies

In this subsection, we give some detail on the two main test strategies that will be employed on the test bench. The first test strategy is referred as *static* and the second one *dynamic*.

Static test strategy. This test strategy takes its name from the fact that the cell bit flips occur when the memories are in hold mode. In other words, the memory cells are initialized with a certain data background and just after they left in hold mode. In practice, during the hold mode the memory only function is keeping the stored data, no read/write operations are performed. The memory content is periodically (e.g. once any 20 minutes for natural radiative environment) scanned in order to reveal potential cell bit flips due to neutrons. The most significant data backgrounds that can be used are the following ones:

- Solid '0', logic value '0' stored all over the memory array
- Solid '1', logic value '1' stored all over the memory array
- Checkerboard, the memory array composes a grid of '0' and '1'

Dynamic test strategy. This test strategy takes its name from the fact that the cell bit flips occur when the memories are in function, with read/write operations ongoing. In particular, several test algorithms, especially March tests, are cyclically performed. This second test strategy appears more effective than the previous one. The static strategy can detect neutron induced malfunction only in memory cells, but memories are not only composed of cells. In fact, peripheral circuits such as address decoders, write drivers, pre-charge circuits, sense amplifiers and input/output circuits compose about 30% of the memory device. Those circuits can be sensible to neutrons collisions as much as storage cells. Thus, dynamic test strategy may allow a better detection of neutron collisions. The dynamic test strategy may improve the success of cell bit flip, because during function (read/write access), SRAM cells have been demonstrate to be more prone to bit flip failures [20, 21]. Moreover, in modern systems, the common operational mode of memories is not the hold mode, but conversely they are accessed (read/write accesses) for the majority of the time, because system performance are strictly related with the memory efficiency. For this reason, the dynamic test strategy is the most close to reality, thus more meaningful.

5. Conclusions

In this paper, we have proposed a novel test bench architecture for the detection of soft errors in SRAMs due to the neutron reactions in the cross section of the device. The record of the memory upsets induced by neutrons is possible for SRAM core-cell capability to swap after a collision. An important element of the proposed architecture is the BOBST (Built-On-Board Self Test). The use of BOBST allows to employ a large number of memories, as required in natural environment, where the occurrence of neutron induced upsets is low. Since the structure must operate in various experimental conditions from the earth surface to spatial environment, it has been conceived to be modular, programmable, low power consuming and portable. A first prototype of a single sub-system module is presented. This module permits to handle the new BOBST concept and adjusts more effectively the test strategy to be implemented. In particular, the use of BOBST allows the execution of a dynamic test strategy that may lead to a better neutron detection than a static test strategy.

References

[1] Semiconductor Industry Association (SIA), "International Technology Roadmap for Semiconductors (ITRS)", 2005 edition
 [2] J. F. Ziegler et al, IBM J. Re. Develop., vol. 40, no. 1, pp. 19-39, (1996)
 [3] J. L. Autran, P. Roche, S. Sauze, G. Gasiot, and D. Munteanu, "Realtime neutron and alpha soft-error rate testing of CMOS 130 nm SRAM: Altitude versus underground measurements," in Proc. ICICTD, 2008, pp. 233-236.
 [4] E.H. Cannon, D.D. Reinhardt, M. S. Gordon, and P. S. Makowenski, Proc. 2004 IEEE Int. Reliability Physics Symp., pp. 300-304, (2004)
 [5] E. Normand, IEEE Trans. Nucl. Sci., vol. 43, pp. 2742-2750, (1996)

[6] Lei, F.; Clucas, S.; Dyer, C.; Truscott, P.; "An atmospheric radiation model based on response matrices generated by detailed Monte Carlo Simulations of cosmic ray interactions", IEEE, Trans. Nucl. Sci., Volume 51, Issue 6, Part 2, Dec. 2004 Page(s):3442 - 3451
 [7] IEC/TS 62396-1: 2006
 [8] Autran, J-L.; Roche, P.; Borel, J.; Sudre, C.; Castellani-Coulie, K.; Munteanu, D.; Parrassin, T.; Gasiot, G.; Schoellkopf, J-P.; Nuclear Science, « Altitude SEE Test European Platform (ASTEP) and First Results in CMOS 130 nm SRAM", IEEE Trans Nucl Sci, Vol 54, Issue 4, Part 2, pp1002 – 1009, (2007)
 [9] Yahagi, Y.; Ibe, E.; Yamamoto, S.; Yoshino, Y.; Sato, M.; Takahashi, Y.; Kameyama, H.; Saito, A.; Hidaka, M.; "Versatility of SEU function and its derivation from the irradiation tests with well-defined white neutron beams", IEEE Trans Nucl Sci, Vol 52, Issue 5, Part 2, pp1562 – 1567, (2005)
 [10] T. Mérelle, H. Chabane, J-M. Palau, K. Castellani-Coulie, F. Wrobel, F. Saigné, B. Sagnes, J. Boch, J.R. Vaillle, G. Gasiot, P. Roche, M-C. Palau, T. Carrière, "Criterion for SEU occurrence in SRAM deduced from circuit and device simulations in case of neutron-induced SER", IEEE, Trans. Nucl. Sci., vol. 52, Issue 4, pp 1148-1155, (2005)
 [11] F. Wrobel, G. Hubert, P. Iacconi, "A semi-empirical approach for heavy ion SEU cross sections calculations", IEEE, Trans. Nucl. Sci., vol. 53, No.6, pp3271-3276, décembre 2006.
 [12] Correas, V.; Saigne, F.; Sagnes, B.; Boch, J.; Gasiot, G.; Giot, D.; Roche, P.; "Simulation Tool for the Prediction of Heavy Ion Cross Section of Innovative 130-nm SRAMs", IEEE, Trans. Nucl. Sci., Volume 55, Issue 4, Part 1, pp2036 – 2041, (2008)
 [13] <http://geant4.web.cern.ch/geant4/>
 [14] F. Wrobel, « Detailed History of Recoiling Ions induced by Nucleons», Computer Physics Communications (2007), doi :10.1016/j.cpc.2007.08.005
 [15] V. Correas, F. Saigne, B. Sagnes, J. Boch, G. Gasiot, D. Giot, P. Roche, "Simulation Tool for the Prediction of Heavy Ion Cross Section of Innovative 130-nm SRAMs" IEEE Trans. Nucl. Sci., Volume 55, Issue 4, Part 1, Aug. 2008 Page(s):2036 – 2041
 [16] V. Correas, F. Saigné, B. Sagnes, F. Wrobel, J. Boch, G. Gasiot, P. Roche, "Prediction of Multiple Cell Upset induced by heavy ions in a 90nm bulk SRAM", RADECS 2008, Jyväskylä (Finlande), sept 2008
 [17] Tipton, A. D.; Pellish, J. A.; Reed, R. A.; Schrimpf, R. D.; Weller, R. A.; Mendenhall, M. H.; Sierawski, B.; Sutton, A. K.; Diestelhorst, R. M.; Espinel, G.; Cressler, J. D.; Marshall, P. W.; Vizkelethy, G.; "Multiple-Bit Upset in 130 nm CMOS Technology", IEEE, Trans. Nucl. Sci., Volume 53, Issue 6, Part 1, Dec. 2006 Page(s):3259 – 3264
 [18] Giot, D.; Roche, P.; Gasiot, G.; Harboe-Sorensen, R.; "Multiple-Bit Upset Analysis in 90 nm SRAMs: Heavy Ions Testing and 3D Simulations", IEEE, Trans. Nucl. Sci., Volume 54, Issue 4, Part 2, Aug. 2007 Page(s):904 – 911
 [19] Cannon, E.H.; Gordon, M.S.; Heidel, D.F.; KleinOsowski, A.J.; Oldiges, P.; Rodbell, K.P.; Tang, H.; "Multi-bit upsets in 65nm SOI SRAMs" Reliability Physics Symposium, 2008. IRPS 2008. IEEE International, April 27 2008-May 1 2008 Page(s):195 – 201
 [20] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan, "Efficient March Test Procedure for Dynamic Read Destructive Fault Detection in SRAM Memories", JETTA'05: Journal of Electronic Testing: Theory and Applications, Vol 21 N.5, 551-561, 2005, Springer Publisher
 [21] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, M. Hage-Hassan M., "Data Retention Fault in SRAM Memories: Analysis and Detection Procedures", IEEE VTS'05: 23rd VLSI Test Symposium, Palm Springs, CA (USA), May 1-5, 2005