Analysing the Memory Effect of Resistive Open in CMOS Random Logic

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Abstract—**This paper analyzes the electrical behaviour of resistive opens as a function of its unpredictable resistance. It is demonstrated that the electrical behaviour depends on the value of the open resistance. It is also shown that, due to the memory effect detection of the open by a given vector Ti depends on all the vectors that have been applied to the circuit before Ti. An electrical analysis of this memory effect is presented.**

I. INTRODUCTION

Due to the complexity of IC technological process, many physical defects occur during the manufacturing of any system. The typical defects encountered in today technologies and modeled in yield simulators are the so-called spot defects that may cause shorts and/or opens at one or more of the different conductive levels of the devices. Test generation for any type of defect is obviously not feasible due to the huge amount of CPU time and memory size required. Instead, test generation relies on fault models that are supposed to both represent the defect behavior and allow easy generation of test vectors through ATPG and fault simulation. However, it is well-known that these fault models cover only partially the spectrum of real failures in today's integrated circuits. In particular, a special attention must be paid to defects that exhibit complex behavior not accurately represented by classical fault models and defects with a high probability of occurrence [1-5]. A number of research works have been conducted in the past years dealing with the electrical characterization and modeling of resistive opens [6-9]. Classically, it is considered that the connection is fully open, i.e. the following gates are completely disconnected and called 'floating gates'.

In this paper, we analyze the case where the following gates are still connected but through a degraded line exhibiting some resistance [10-17]. It is important to note that the value of this resistance is an unpredictable parameter of the defect. The electrical behavior of the defect obviously depends on this random parameter as well as its detection conditions. In order to optimize and guarantee the detection of such a defect, its electrical behavior has to be analyzed as a function of this random parameter and optimal detection conditions must be derived.

The paper will be organized as follows. Section 2 gives the general definitions around resistive opens. In section 3 and 4, the detection of the open is analyzed considering a sequence of 2 test vectors, then considering a sequence of n test vectors. Starting from this analysis, section 5 proposes an electrical model for the memory effect of resistive opens. Finally, section 6 gives some concluding remarks.

II. DEFINITION

In this section, an electrical analysis of the resistive open is conducted using a didactic circuit. Figure 1 gives an example of an extremely simple circuit where node n_4 is affected by a resistive open. This didactic circuit has 4 inputs (I_1, I_2, I_3, I_4) and 2 outputs (O_1, O_2). Note that we do not care for the logic function; we just need a simple example to conduct our electrical analysis. Obviously, the demonstrations given below can be extended to real cases.

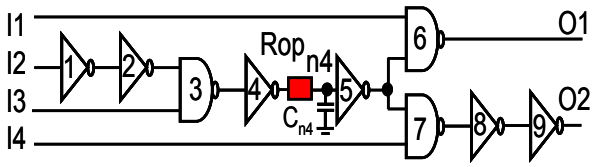

Figure 1. A resistive open

From a static voltage test point of view (Boolean testing), it is well known that a resistive open cannot be detected because the faulty node always ends up reaching its correct logic value. On the contrary, resistive opens modify the timing behavior of the circuit, so they can be detected by a dynamic voltage test strategy (delay testing).

A SPICE simulation of the defect-free circuit (R_{op} = 0Ω) using a 180nm technology is first performed. Analysis of the dynamic behavior requires to create some signal transitions on the circuit inputs and to propagate these transitions through the circuit. The initial state is given by vector T_0 = <I_1, I_2, I_3, I_4> = <0011> and the transition is created by vector T_1 = <0111>. Only input I_2 switches from 0 to V_{DD} at time t_0 = 0, creating the transition. This

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transition propagates through the critical path including gates 1/2/3/4/5/7/8/9 and output O_2 switches from 0 to V_{DD}. From this simulation, we consider that we can use a cycle time of about T_{cl} = 0.4ns with a small but reasonable security margin.

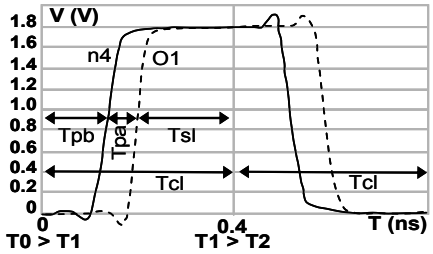


Figure 2. Defect-free path (I_2 to O_1)

We perform now another simulation of the fault free circuit (R_{op} = 0Ω) illustrated in Figure 2 with two different vectors: T_0 = <1010> and T_1 = <1110>. Input I_2 again switches from 0 to V_{DD} but, in this case, the rising edge is propagated to output O_1 through gates 1/2/3/4/5/6. The propagation of this rising edge allows to give the following definitions:

- T_{pb} (Propagation Before the defect),
- T_{pa} (Propagation After the defect),
- T_{sl} (Slack Time of path $I2 \rightarrow O1$).

The rising edge of input I_2 reaches the defect at time T_{pb} = 0.135ns, which is considered equal to the sum of the different gate propagation delays:

$$T_{pb} = T_{d1} + T_{d2} + T_{d3} + T_{d4} = 0.135\text{ns} \quad (1)$$

where T_{di}: propagation delay of gate 'i'.

In the above equation, each gate propagation delay T_{di} depends on:

- the node capacitance C_{ni}
- the strength of the driving gate W^n_i, L^n_i, W^p_i, L^p_i
- the resistance R_{ni} of line n_i (often neglected).

Then the edge propagates from the defect to the output and reaches output O_1 in a period of time T_{pa} = 0.065ns that depends on the propagation delay of gates 5/6:

$$T_{pa} = T_{d5} + T_{d6} = 0.065\text{ns} \quad (2)$$

Finally, output O_1 stays stable for a period of time T_{sl} = 0.2ns before being latched, assuming some output register. Obviously, the following relation links the different times:

$$T_{cl} = T_{pb} + T_{pa} + T_{sl} \quad (3)$$

III. DETECTION WITH A 2-VECTOR SEQUENCE

We consider now the faulty circuit, i.e. a non-zero resistance. The open resistance R_{op} is a random parameter of the defect and can not be predicted, but we can simulate different cases of resistance value. Figure 3.a gives an example of open where the value of the resistance is quite small: R_{op} = 3kΩ. Here again, a sequence of 2 vectors creating a transition is applied: T_0 = <1010> and T_1 = <1110>. Input I_2 switches and the rising edge is propagated to node n_4. It clearly appears that the signal at node n_4 is slowed down. An additional delay T_{op} = 0.13ns appears. But the size of the timing defect is still smaller than the slack time, a correct output value is latched in the output register and the circuit operates correctly:

$$T_{pb} + T_{op}(3\text{k}\Omega) + T_{pa} < T_{cl} \quad (4)$$

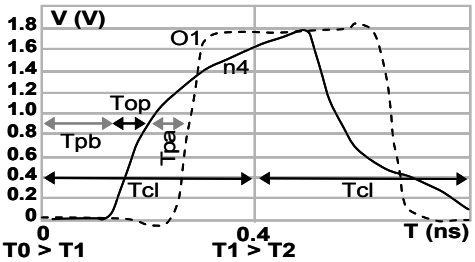
Figure 3.b gives another example where the value of the open resistance is higher: R_{op} = 7.5kΩ. In this latter case, the size of the timing defect is larger than the slack time and so the rising transition of output O_1 occurs after the end of the cycle time. A faulty output value is captured in the output register and the open can be detected:

$$T_{pb} + T_{op}(7.5\text{k}\Omega) + T_{pa} > T_{cl} \quad (5)$$

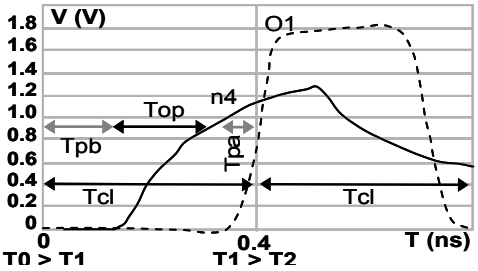
The above simple simulations demonstrate that detection of the open depends on its random resistance. In a more general way, the rising transition of a faulty node ni and therefore the additional delay T_{op} depend on:

- the node electrical parameters R_{ni}, C_{ni}
- the strength of the driving gate W^n_i, L^n_i, W^p_i, L^p_i …
- the defect random parameter R_{op}
- the initial voltage V_0

$$\Rightarrow \quad T_{op} = F(R_{op}, V_0, R_{ni}, C_{ni}, W^n_i, L^n_i, W^p_i, L^p_i) \quad (6)$$



a) Small resistance R_{op} = 3kΩ



b) High resistance R_{op} = 7.5kΩ

Figure 3. Dynamic behavior of a resistive open

From Figure 3, it is clear that an open with a small resistance (3kΩ) cannot be detected while an open with a large resistance (7.5kΩ) can be detected.

This means that a given resistive open can be detected by the 2-vectors sequence {T_0, T_1} if its unpredictable resistance R_{op} is larger than a critical resistance called

$R_c^{\{T0,T1\}}$. In other words, we associate to the resistive open the Detection Interval *DI* defined below:

$$DI^{\{T0,T1\}} = [R_c^{\{T0,T1\}}, \infty] = [7.5k\Omega, \infty] \quad (7)$$

The critical resistance is the resistance value such that the additional delay T_{op} is equal to the slack time:

$$T_{op} = T_{sl} = T_{cl} - T_{pb} - T_{pa} \quad (8)$$

In fact, the SPICE simulation of Figure 3.b corresponds to this critical resistance $R_c^{\{T0,T1\}} = 7.5k\Omega$. In other words, any open with a resistance larger than 7.5kΩ can be detected by the 2-vector sequence $\{T_0, T_1\}$. An open with a smaller resistance creates an additional delay which is too small to be detected.

IV. DETECTION WITH AN N-VECTOR SEQUENCE

Now, we consider a more realistic situation where, starting from an initial state given by T_0, a complete test sequence of m vectors is applied to the circuit targeting different defects/faults:

$$\text{Test sequence} = \{T_0, T_1, \ldots, T_{n-1}, T_n, \ldots, T_m\} \quad (9)$$

In this sequence, we assume now that vector T_n has been specifically generated to detect the resistive open on node n_4. Tn is such that the transitions created by the 2 vectors $\{T_{n-1}, T_n\}$ are able to detect the resistive open on node n_4. In other words, the pair $\{T_{n-1}, T_n\}$ creates a transition that passes through node n_4 and is propagated to an observable output.

It is important to note that the preceding vectors $\{T_0, T_1, \ldots, T_{n-1}\}$ may create some transitions of node n_4 but these transitions are not propagated to an output, i.e. the open is not detected before vector T_n. For detection of the resistive open, we consequently divide the sequence into 2 phases:

- The preparation phase corresponds to the application of the n - 1 vectors $\{T_1, \ldots, T_{n-1}\}$ starting from the initial state T_0, i.e. when the open cannot be detected but the faulty node may switch.
- The detection phase corresponds to the application of vector T_n, i.e. when the faulty node switches and it is observable on the outputs.

As an example, for the resistive open of Figure 1, we consider the preparation phase made of the initial state $\{T_0\}$ and a sequence of 5 vectors $\{T_1, T_2, T_3, T_4, T_5\}$, and the detection phase made of vector $\{T_6\}$, i.e. the case where n = 6. These vectors are given in Table 1.

Table 1: The simulated test sequence

Phase	Vector	Cycle	I1	I2	I3	I4	Transition Polarity on n4
	T0	Initial State	0	0	1	0	
Preparation	T1	#1	0	1	1	0	+
	T2	#2	0	0	1	0	-
	T3	#3	0	1	1	0	+
	T4	#4	0	1	1	0	+
	T5	#5	0	0	1	0	-
Detection	T6	#6	1	1	1	0	+

From the input vectors in Table 1, we deduce that:

- Inputs I_3 and I_4 are stable. I_3 is equal to 1, which always enable propagation of the I_2 input transition through gate 3 along the 6 cycles. I_4 is equal to 0 preventing propagation through gate 7 and so output O_2 remains at 1.
- Input I_1 is equal to 0 along the first 5 cycles (propagation phase) preventing propagation through gate 6 during the first 5 cycles. And so, the resistive open cannot be detected during the first 5 cycles. Then input I_1 switches to 1 in the sixth cycle allowing propagation through gate 6 and so enabling detection (detection phase).
- Input I_2, starting from 0, successively switches to 1, 0, 1, 1, 0 and 1, creating different transitions in the circuit.

In this simple and didactic example, node n4 is observable on output O_1 only during the 6th cycle when I_1 = 1. Vector T_6 has obviously been generated on purpose, i.e. to detect a fault on node n_4 and so it makes node n_4 observable. The previous vectors (T_1, …, T_5) have been generated targeting some other faults.

a) Preparation phase

We first analyze the preparation phase. As commented above, during the first 5 cycles node n_4 is not observable, but it may switch from 0 to 1 or from 1 to 0 according to the activity of the circuit induced by the input vectors. In other words, the successive input vectors may create successive transitions of node n_4. In the fault-free circuit node n_4 switches from *Gnd* to V_{DD} and vice-versa, but in the faulty circuit the signal is degraded by the resistive open. Two cases may appear:

- If the resistance of the open is small, the signal is slowed down but it is still able to reach the *Gnd* and V_{DD}.
- If the resistance of the open is large enough, the signal is slowed down and it is not always able to reach the V_{DD} and *Gnd* values as illustrated in Figure 4 with R_{op} = 7.5kΩ.

Let us explain in detail the second case with the example of Figure 4. Input I_2 is initially equal to 0 (initial state T_0) and switches to 1 (T_1) at time t_0. At time $t_0 + T_{pb}$, the rising transition reaches the output of gate 4 and so the voltage $V(t)$ of node n_4 starts switching from $V_0 = Gnd$ to V_{DD}.

Due to the resistance R_{op} of the defect, the time required by $V(t)$ to reach V_{DD} is much higher than the cycle time T_{cl}. At the end of the 1st cycle, i.e. at time ($t_0 + T_{cl}$), input I_2 switches from 1 to 0 (T_2) and this new transition reaches node n_4 at time ($t_0 + T_{cl} + T_{pb}$). This new transition interrupts the previous one even if node n_4 has not yet been able to reach V_{DD}. Consequently, we observe that, during the first cycle, node n_4 rises from $V_0 = V(t_0 + T_{pb}) = 0V$ to $V_1 = V(t_0 + T_{cl} + T_{pb}) = 1.26V$.

Obviously, we can make the same demonstration for the second cycle where a new transition on node n_4 interrupts the previous one and the voltage on node n_4 falls from $V_1 = V(t_0 + T_{cl} + T_{pb})$ to $V_2 = V(t_0 + 2T_{cl} + T_{pb})$. In a similar way, the voltage rises from $V_2 = V(t_0 + 2T_{cl} + T_{pb})$ to $V_3 = V(t_0 + 3T_{cl} + T_{pb})$ during the third cycle, and so forth.

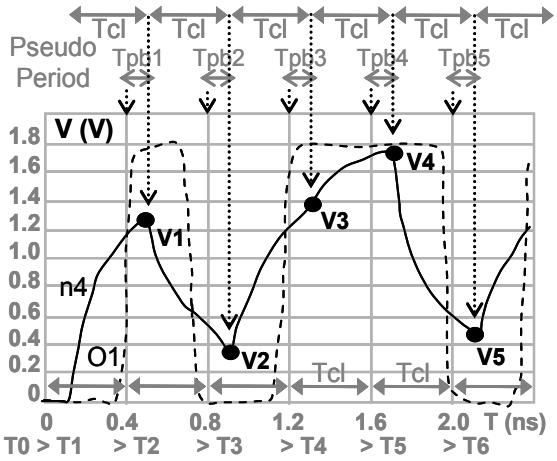


Figure 4. Dynamic behavior through a sequence

Table 2. Simulated successive intermediate voltages

Vector	Intermediate Voltages
Initial State	V0 = 0V
T1	V1 = 1.26V
T2	V2 = 0.36V
T3	V3 = 1.39V
T4	V4 = 1.70V
T5	V5 = 0.49V

So, we globally observe that the voltage on node n_4 does not simply switch between *Gnd* and V_{DD}. Instead, it rises and falls according to the input vectors and goes through a set of successive intermediate voltages V_0, V_1, V_2, V_3, V_4, V_5 whose values are given in Table 2.

Important is the fact that these successive voltages are more or less following the clock of the circuit. Indeed, they appear at a period of time T_{pb} after the clock pulse. In the general case, the transition may use different path for different vectors and so, the different points will appear at different after the clock. Consequently, the periodicity may vary from vector to vector but not too much because the propagation paths before the defect T_{pbi} are not varying too much. In addition, the transitions are always initiated by the circuit inputs that follow the circuit clock. And so the global period will correspond to the circuit clock frequency T_{cl}.

For the above reasons, we will say that the successive intermediate voltages exhibit a pseudo-period equals to the circuit clock T_{cl}.

Very important is also the fact that, for each vector T_j, the corresponding intermediate voltage V_j on node n_i depends on:

- the polarity of the transition
- the node electrical parameters R_{ni}, C_{ni}
- the strength of the driving gate W^n_i, L^n_i, W^p_i, L^p_i …
- the defect random parameter R_{op}
- the pseudo-period T_{cl}
- the previous intermediate voltage $V_{j\text{-}1}$

In other words, for a given vector T_j, the voltage V_j depends on the resistance of the open and on the previous voltage which also depends on the resistance of the open and on the previous voltage which in turn depends on the same parameters.

For a given node, some of the above parameters may be considered as 'constant' through out the test sequence: R_{ni}, C_{ni}, W^n_i, L^n_i, W^p_i, L^p_i. Lets call P these constant parameters, we can write:

$$V_j = V(t_0 + j \cdot T_{cl} + T_{pbj}) = F(R_{op}, V_{j\text{-}1}, P) \quad (10)$$

Consequently, at the end of the preparation phase, just before the detection phase (vector T_n), the faulty node n_i presents a voltage $V_{n\text{-}1}$ which depends on all the previous intermediate voltages through a sort of memory effect. And so it depends on all the previous vectors that have been applied to the circuit. We can write:

- $V_{n\text{-}1} = V(t_0 + (n - 1) \cdot T_{cl} + T_{pbn} - 1) = F(R_{op}, V_{n\text{-}2}, P)$
- $V_{n\text{-}2} = V(t_0 + (n - 2) \cdot T_{cl} + T_{pbn} - 2) = F(R_{op}, V_{n\text{-}3}, P)$
- ….
- $V_1 = V(t_0 + 1 \cdot T_{cl} + T_{pb1}) = F(R_{op}, V_0, P)$

$$\Rightarrow V_{n\text{-}1} = F(T_0, T_1, T_2, \ldots, T_{n\text{-}1}) \quad (11)$$

b) Detection phase

We now analyze the detection phase using again our small example. When vector T_6 is applied to the circuit, a transition is propagated from input I_2 to node n_4, the transition is delayed by the resistive open, and finally the delayed transition propagates to output O_1.

This situation is quite similar to the one described for the 2-vector sequence in the previous section. An input transition is initiated by 2 vectors: the last vector of the preparation phase T_5 and the vector of the detection phase T_6. So, we come to a similar conclusion: an open with a small resistance can not be detected while an open with a large resistance can be detected.

And so, the resistive open can be detected by the *n*-vectors sequence $\{T_0, T_1, T_2, T_3, T_4, T_5, T_6\}$ if its unpredictable resistance R_{op} is larger than a critical resistance called $R_c^{\{T0,T1,T2,T3,T4,T5,T6\}}$. Here again, we associate to the resistive open the Detection Interval *DI* defined below:

$$DI^{\{T0,T1,T2,T3,T4,T5,T6\}} = [R_c^{\{T0,T1,T2,T3,T4,T5,T6\}}, \infty] \quad (12)$$

But there is a fundamental difference between the 2-vector sequence and the *n*-vector one. In the 2-vector sequence, the additional delay is a function of the initial voltage $V_0 = 0$ as given by eq. (6). While, in the *n*-vector sequence, the additional delay T_{op} is a function of the previous intermediate voltage $V_{n\text{-}1}$. Indeed, it is clear that the transition in Figure 4 depends on:

- the node electrical parameters R_{ni}, C_{ni}
- the strength of the driving gate W^n_i, L^n_i, W^p_i, L^p_i …
- the defect random parameter R_{op}
- the previous voltage $V_{n\text{-}1}$

$$\Rightarrow T_{op} = F(R_{op}, V_{n\text{-}1}, R_{ni}, C_{ni}, W^n_i, L^n_i, W^p_i, L^p_i) \quad (13)$$

Coming back to our simple example, SPICE simulations show that the critical resistance is equal to $R_c^{\{T0,T1,T2,T3,T4,T5,T6\}} = 28k\Omega$. In other words, any open with a resistance larger than 28kΩ can be detected by the 6-vector sequence. An open with a smaller resistance creates an additional delay which is too small to be detected.

Note that the above range is completely different from the one obtained in the previous section with the 2-vector sequence $\{T_0, T_1\}$. This clearly demonstrates the significant impact of the preparation phase on the detection of the resistive open.

V. ELECTRICAL MODEL OF THE MEMORY EFFECT

In the previous section, simulations of Figure 4 clearly illustrate the series of successive intermediate voltages V_1, V_2, V_3, V_4, V_5. We understood that the logic commutation of the faulty node creates incomplete transitions due to the resistance of the open.

The objective now is to analyze these incomplete transitions using a simplified model of the faulty node. For this purpose, we consider a simple RC model where C is equal to the C_{n4} capacitance of the circuit of Figure 1 (C_{n4} = 1.6fF), and R has been tuned by simulation such that response of the RC model perfectly fits the simulation of the circuit in Figure 4 where R_{op} = 7.5kΩ. In fact, the resistance R is 'globally equivalent' (R_{eq}) to the transistor resistance of inverter 4 plus the resistance of the open R_{op} = 7.5kΩ.

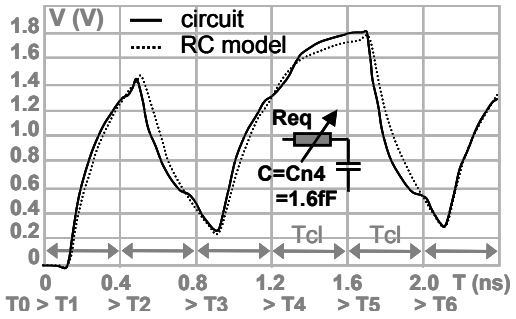


Figure 5. Fitting the RC model to the faulty circuit

Figure 5 shows the superimposition of the RC model response and the circuit response. The good agreement between the two responses allows us to use the RC model just with the purpose of analyzing the successive intermediate voltages.

We consider now the situation where an input pulse of amplitude V_a is applied to the RC circuit while the voltage of the output is equal to V_{old}. The problem being to compute the new voltage V_{new} as a function of V_{old}, R_{eq}, C_{n4} and the applied pulse V_a. According to the classical equation of a charge of a capacitance through a resistance, the new voltage is given by the following equation:

$$V_{new} = V_{old} + \Delta V(1-e^{-t/ReqCn4}) \quad (14)$$

Where ΔV is the difference between the applied voltage V_a and the current voltage V_{old}: $\Delta V = V_a - V_{old}$

The new voltage is obviously an exponential function of R_{eq} and C_{n4}. It is very important to note here that the new voltage is a function of the difference ΔV between the applied voltage V_a and the current voltage V_{old}. We also remember that the successive voltages appear with a pseudo-period equal to the period T_{cl} of the circuit. Consequently, the new voltage corresponds to time $t = T_{cl}$.

The input vectors create transitions that propagate to the faulty node, but the polarity of the transitions on the faulty node depends on the logic function. The transitions on the faulty node may be positive i.e. from *Gnd* to V_{DD}, in this case $\Delta V = V_{DD} - V_{old}$ or negative i.e. from V_{DD} to *Gnd*, in this case $\Delta V = 0 - V_{old}$. We finally obtain the two following equations for the faulty node:

- Positive transition

$$V_{new} = V_{old} + (V_{DD} - V_{old})(1 - e^{-Tcl/ReqCn4}) \quad (15)$$

- Negative transition

$$V_{new} = V_{old} \cdot e^{-Tcl/ReqCn4} \quad (16)$$

Considering the initial state $\{T_0\}$ and the 5 vectors of the preparation phase $\{T_1, T_2, T_3, T_4, T_5\}$ of the previous section (Figure 4), we know that node n_4 should switch from 0 to 1, 0, 1, 1, and 0. So, we can use equations 15 and 16 according to these different transitions to compute the successive voltages. Remember that R_{eq} has been set to match the simulation of Figure 4 with R_{op} = 7.5kΩ. Table 3 summarizes the obtained results.

Table 3: Computed successive intermediate voltages

Vector	Intermediate Voltages
Initial State	V0 = 0V
T1	V1 = 1.26V
T2	V2 = 0.38V
T3	V3 = 1.37V
T4	V4 = 1.67V
T5	V5 = 0.50V

The computed successive voltages given in Table 3 perfectly match with the simulated ones in Table 2. This proves that the fundamental cause for the appearance of successive intermediate voltages is due to RC-type phenomenon. Therefore, the RC model can be used to analyze the effect of the preparation phase on the voltage V_{n-1}.

VI. CONCLUSION

This paper analyzes the electrical behavior of a resistive open as a function of its unpredictable resistance. It is demonstrated that the detection of the resistive open not only depends on the unpredictable resistance but also on the successive intermediate values of the faulty node, i.e. depends on all the vectors that have been applied to the

circuit. An electrical analysis of this memory effect is presented.

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