Testing System-In-Package Wirelessly

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***Abstract*-The paper shows a new concept for testing a system-in-package (SiP) using a wireless communication. Trends of the SiP technology put more economic and technical constraints onto the test, while the contactless test techniques represent an opportunity to overcome the inherent problems. In this paper, we introduce a new test concept based on a wireless communication, a specific test access mechanism (TAM), and an optimised architecture. Although this approach is dedicated to an intermediate test of SiP, we explore other potential applications of this technology.**

***Keywords*—**SiP; system test; scan test; wireless testing;

I. TRENDS IN SYSTEM-IN-PACKAGE

A System-In-Package (SiP) is a package that combines all of the electronic components (digital ICs, analog ICs, RF ICs, passive components or other elements) needed to provide a system or subsystem in one package, essentially an alternative to a System-On-Chip (SoC).
The market for stacked die and stacked packages is driven by portable applications that require extremely small form-factors.
SiP has grown since year 2000, and will represent almost half of the quantities in year 2007. This growth is driven by the need to incorporate increased functionality in smaller spaces.
SiPs found their applications in numerous domains and result in a large variety of structures. Digital camcorders have been one of the first adopters of new and innovative packaging technologies. A variety of SiPs are also increasingly found in
the RF, digital baseband, transceiver sections of mobile phones and set top box applications that include source decoder, tuner, and channel decoder in the same package (figure 1).

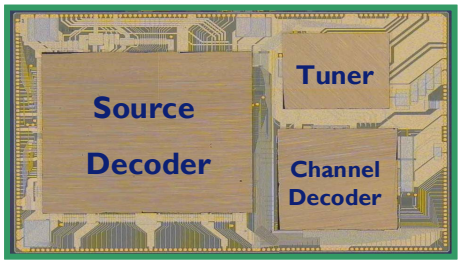

Figure 1. Example of a Set Top Box in one package
(Source: Philips Semiconductors)

SiP applications also include medical electronics such as smart pills and implanted devices, defense electronics, and aerospace applications. While these applications represent smaller unit volumes they represent higher value-added modules.
Some of the related structures are planar constructions. Several of them incorporate integrated passive substrates thanks to thin-film-on-silicon module that incorporates passive devices such as planar capacitors, pit capacitors, resistors, and inductors in the substrate [1].
Additional structures include stacked die packages or stacked modules. The first stacked packages utilized in market applications contained only memory, but increasingly logic devices are being added. While the thinnest packages (important for mobile phones) feature bare die stacked inside the package, issues of bare die availability, logics, and test resulted in a large number of stacked package configurations. A number of companies is promoting the package-on-package (PoP) concept. In this construction, one package is stacked on top of another. The package offers flexibility in the configuration of the memory and allows the memory to be fully tested before the packages are molded together.
Some configurations feature a bare die surrounded by packaged memory (Computer and telecommunication applications for instance).

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II. CONSTRAINTS AND CHALLENGES

Compared to a single IC, the assembly of a multi-die SiP requires a much more complex process, which inherently creates new types of failures, because:

a) More stress is applied during assembly, which may cause die cracks, or broken bonding.
b) Placement of active dies on passive die is a potential source of misalignment i.e. shift and rotation (figure 2)

Basically, the main difference between SoC and SiP manufacturing is that all components in a SoC are manufactured at the same phase while the SiP is an assembly of components manufactured independently. Test approaches must be adapted to the context. Conversely to SoC testing process, which consists in an unique test phase at the end of the system manufacturing, the SiP testing process includes preliminary tests for each die and system level tests.

Indeed, the defect level per die (% of faulty devices that pass the test) is a primordial economic aspect for SiP. Ideally, every die should be fault-free before assembly; this is classically referred as the Known Good Die (KGD) concept. However, KGD is sometimes not achievable, and since the assembly process may introduce additional failures (see above), intermediate tests after every die soldering are required. The system level test is thus made of several phases. This strategy combined with a die assembly ordering (from the less to the most expensive dies) allows one to optimize the overall SiP cost.

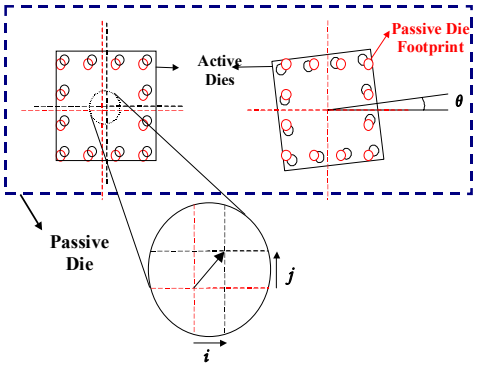

Figure 2. Misplacement parameters: shift (left), and rotation (right).

A major problem with this strategy is that intermediate tests require several probing on substrate pads. However, scrubbing the pad clearly may affect the quality of wire bonding. Actually, re-probing is restricted to a very small count, typically 3 impacts of needles is allowed. This limitation restricts to only 2, the number of dies soldered on the SiP, since the first contact is required to test the passive substrate.

Another concern is the probe technology limitation. Figure 3 shows the trend of bond pad pitch in short term. Clearly, it appears that the pitch will be equal to or smaller than 20µm, whereas the current probe technologies for mass production are capable of contacting with a 40µm pitch only.

Technology		Current	Q2 Y2005	Q4 Y 2005	Y2006
Wafer Technology Node		0.13um	0.09um	0.09um	0.065um
Bond Pad Pitch	In-Line	40um 0.7mil Au	35um 0.6mil Au	⇨	30um 0.5mil Au
	Staggered & Dual Inline	25/50um 0.7mil Au	⇨	20/40um 0.6mil Au	⇨
	3-row	30/60um 0.9mil Au	⇨	25/50um 0.7mil Au	20/40um 0.6mil Au
	Reverse	65um 1.0mil Au	60um 0.9mil Au	50um 0.8mil Au	45um 0.7mil Au
Bond Lead Pitch (Pitch/Width)	Laminate	110um/ 45um 1.0mil Au	⇨	95um/ 35um 1.0mil Au	85um/ 30um 0.8mil Au
	Leaded	140um/ 55um 0.8mil Au	⇨	135um/ 50um 0.7mil Au	⇨

Figure 3. Wire bonding roadmap
(Source: STATSChippac Inc.)

III. CONTACTLESS TEST TECHNIQUES

As seen in the previous section, probing will have to face very big challenges in a near future. Although the technologies are constantly improving (membrane, MEMS, etc…), non-contact techniques represent a real breakthrough in this area.

A new technology, relying on near-field communications to exchange test data at gigabit per second rates, has been recently proposed by an emerging company, namely Scanimetrics Inc. [3]. The "probe card" consists of a CMOS device with micro antenna structures and transceiver circuits.

The input/output cells of the DUT (Device Under Test) are changed, by adding an antenna and a transceiver to each test pad. The test data signals modulate/demodulate a carrier generated by the transceiver circuits (in the range of 3 to 5GHz). Because of the proximity of the probe with respect to the DUT (less than 100µm), the transmitted power is quite low (a few tens of µW), so that interferences between adjacent probes/pads can be minimized. Figure 4 shows the basic principle of this technology.

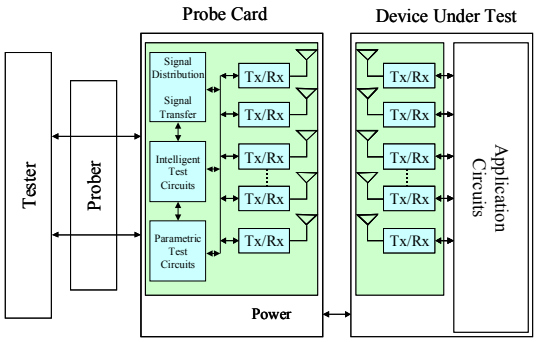

Figure 4. Block diagram of non-contact wafer probe system *(Source: Scanimetrics Inc.)*

A wireless JTAG is also proposed in another paper [4], in order to non-intrusively test a system made of several boards. According to the authors, a wireless version of the JTAG standard offers many advantages and opportunities. Daisy-chained wiring typically interconnects the JTAG ports of the components on a system board, and multiplexers and demultiplexers are required to select the boards to be tested, whereas radio communication gives selective access to each JTAG port.

Wireless JTAG further offers non-intrusive testing, debugging, and configuration. For example, with wireless JTAG, EEPROMs or FPGAs can be reprogrammed wirelessly without having to connect the programmer with the device to be programmed.

More recently, a paper describes a transparent solution for remote wired or wireless communication to board and system level boundary-scan architectures, in compliancy with the 1149.1 standard.
The solution makes use of a transceiver pair comprising of an Uplink located in close proximity to the boundary-scan test controller and a Downlink either located in close proximity or embedded within the target Board-under-Test [5].

A SiP being made of several ICs, a derivative technique may be developed to make intermediate tests during the assembly, given that it shows many similarities with a PCB assembly.

IV. APPLICATION OF WIRELESS COMMUNICATION TO INTERMEDIATE TEST OF SIP

We consider the assembly of a SiP made of 3 active dies soldered onto a passive substrate (Figure 5). For simplicity, we base our explanation on 3 dies, but there are already a few applications where 5 dies or more are embedded into one package.

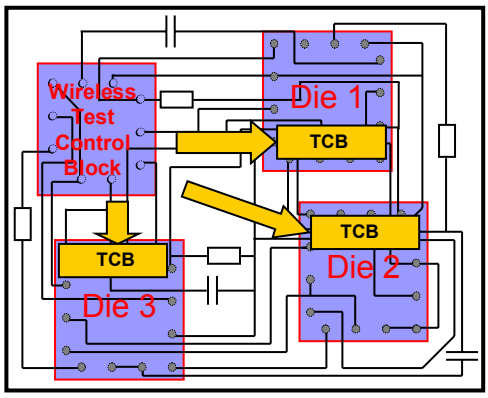

Figure 5. 3-die assembly process steps

In this example, we represent the Wireless Test Control Block (WTCB), including the Test Access Port (TAP) Controller, as a discrete element. The WTCB is first soldered, then the dies 1, 2, and 3 successively. Supposing that the cost of die 3 is dominant, then intermediate testing should be implemented after die 2 is soldered.
The test connection between ATE (Automatic Test Equipment) is depicted as following: every active die is ideally tested with a WTCB, usually JTAG-compliant for Mixed-Signal, and Digital devices.

A one-channel wireless communication is expected, because it offers many advantages, compared to a Scanimetrics-like solution, among them:

- Less sensitivity to interferences (one pad only)
- Longer distances between ATE and DUT (less constraints)
- More SiPs can be tested in parallel
- Test of encapsulated SiPs will be possible, at any time (production or in-situ tests)

Obviously, this solution also brings some difficulties that need to be addressed. Basically, they are twofold:

- How to build an optimized internal architecture for test?
- What is the “best” protocol stack for wireless test?

To conclude, the global wireless test architecture relies on two key elements: the “local” test mechanism (that included in each SiP) and the protocol stack that ensures exchanges between the SiPs and the ATE. Both are integrated in what we have defined as a Wireless Test Control Block (WTCB). A study about the organization is carried out, considering the ATE to TCB link as a serial one. Doing so, we separate the two issues: local test access mechanism on one hand (i.e. the “internal” architecture) and wireless communication on the other hand (i.e. the protocol stack).

IV.1. The Internal Architecture

Concerning the internal architecture, the first pre-requisite is linked to the compliancy with the 1149.1 standard. Actually, a SiP must react as a SOC when soldered on the PCB. In other terms, we have to keep the 4 fundamental JTAG connections available for the integrator or the customer (TDI, TDO, TCK, TMS). The second pre-requisite is that the manufacturer needs JTAG resources for intermediate tests while some dies are missing.

Therefore, we have defined a JTAG implementation with two modes of operation, so-called 'ring' and 'star' configurations. An extra signal $\overline{R}/S$ (Ring/Star) allows switching from one mode to the other one through additional multiplexers.

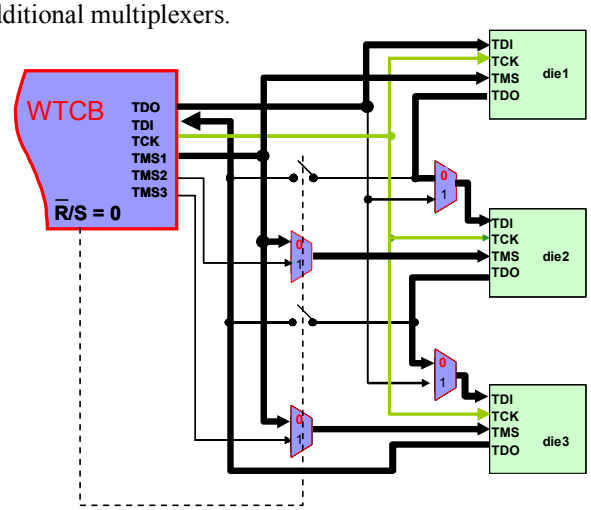

Figure 6. Ring configuration

The 'ring' configuration is designed such that the end-user cannot detect the presence of several dies, either for identification (one ID code), or for boundary-scan test. Only one test control signal TMS is required in this configuration (figure 6).

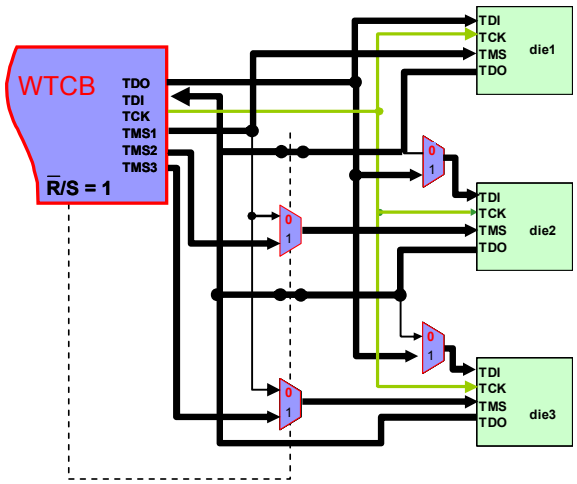

Figure 7. Star configuration

The 'star' configuration aims at making intermediate testing during the assembly. Obviously, the link between the dies (daisy-chain) is broken when making intermediate testing since all dies are not soldered onto the substrate yet. So the boundary-scan test cannot be performed using the ring architecture. This configuration requires as much control signals TMSi as dies in the system (Figure 7).

Finally, in addition to the extra elements required for switching between the two modes of test configurations, a serializing/de-serializing circuitry and a RF transceiver must be added in the WTCB to transmit and convert the test data and signals.

IV.2. The protocol stack

The global architecture (figure 8) is based on one ATE communicating with a set of top-level TCBs (one for each SiP: the WTCB). Each one has a communication dedicated module, and is thus considered as a node of the wireless test network. This network corresponds to a unique domain of collision; as a consequence, collision avoidance is an important issue, a fortiori in such context which requires deterministic communication.
We propose a protocol stack reduced to 3 layers. The lowest layer deals with "low-level", i.e. physical asynchronous transmission of packets: its specifications concern the signal frequency, the modulation (with the lowest error rate as possible), the maximum distance between DUT and ATE antennas, etc. The second layer is dedicated to Medium Access Control (MAC): it has to offer mechanisms allowing efficient and deterministic use of the medium. Finally, the highest layer is application oriented: it supports the protocol used for the test itself, but also used for node configuration purposes (from a network point of view).

We won't detail the whole protocol stack (out of the scope of this paper), nevertheless let us give the main characteristics of the MAC layer which is a key issue of the protocol stack.
As we resort to RF communication, broadcasting of packets is ensured at the lowest level. We need however to be able to distinguish nodes by means of logical addressing:

- unicast addressing to communicate with individual nodes (e.g. for network configuration purposes),
- broadcast addressing to allow, for example, to simultaneously launch the test on all nodes (parallel testing of dies of concerned SiPs),
- and multicast addressing to allow selective exchanges (e.g. exclusion of failing SiP).

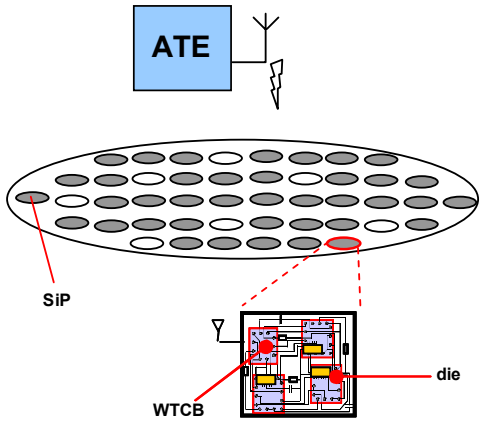

Figure 7. Global architecture

For overall performance purposes, simultaneous test of all the SiP (all the concerned dies) is performed. That induces the problem of local test results getting (i.e. how to get the result of the test for each SiP). It's unconceivable that all nodes simultaneously respond as it would generate collisions and so require a complex algorithm to solve such situation (with solutions often based on random medium allocation) without guaranty of efficiency. It is neither conceivable to scan all nodes by request-response exchanges as the efficiency would be low. A predetermined static medium allocation (a given time interval allocated to each node) is not a better solution as it doesn't take into account dynamically rejected failing-SiP (static allocation would also change according to the number of SiP on the wafer). So, we propose a MAC method based on group allocated temporal window within which we perform sliding member time interval [6]. This method ensures deterministic medium allocation (each SiP can by itself send its test result) and allows dynamic adapting of the group membership (rejection of failing-SiP). This method also ensures that the ATE (i.e. the central node) can, if necessary, retake the control of the medium access, in a deterministic way. With this MAC method we do not have anymore to manage collisions.
A deeper study of the WTCB is in progress in order to master its complexity and memory size. Moreover, several test strategies are considered (from centralized to distributed comparison of test results) as well as their impact on the application protocol features.

V. CONCLUSION

The evolution to wireless communication is now a reality in the daily life, with many advantages such as reliability, flexibility, cost savings, and sustainability. The test in general may also benefit from such technologies, and especially when contacting becomes a very big issue.
The growth of the SiP technology represents an opportunity to develop a wireless test architecture and its appropriate protocol stack and mechanisms. We have proposed this solution to make an intermediate test of the SiP in the assembly process, as a starting point. However, we have seen that this technology could be more extensively used in many other cases, offering many benefits, especially when no intrusion is allowed.
Works are now conducted on the WTCB in order to define an optimized architecture for the TCB at top level, but also for the local TCBs, at die level. In parallel, we deeply investigate a protocol stack adapted to the specific needs for a robust and efficient wireless test.

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