

# DC–100-GHz Frequency Doublers in InP DHBT Technology

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**Abstract**—Broad-band monolithic integrated active frequency doublers operating in dc-100-GHz frequency range are presented. Circuits are fabricated in a self-aligned InP double heterojunction bipolar transistor process. Three integrated doubler versions have been designed. Inductive peaking and active splitting effects are quantified and compared. Circuit measurements give sinusoidal output waveform at 100 GHz with an rms timing jitter of 400 fs. Circuits have a maximum conversion gain of +1 dB at 60 GHz. The fundamental suppression is better than 24 dB in the whole frequency range.

**Index Terms**—Active splitter, doubler, frequency multiplier, Gilbert cell, InP double heterojunction bipolar transistor (DHBT).

## I. INTRODUCTION

**F**REQUENCY multipliers, and in particular frequency doublers, are important building blocks for many applications, as well as for measurement equipment. The progress of semiconductor technologies based on both specific materials and proper scaling of devices enables us to contemplate high-speed broad-band system applications up to 100 GHz. Design and measurement of such high-speed circuits present important challenges. Specific design methodology should be applied. For measurement, high-frequency sources are necessary but the usual sources such as manufacturer synthesizers are limited to 60 GHz.

Broad-band active frequency doublers have been described in Si BJT at 12 GHz [1], in SiGe heterojunction bipolar transistor (HBT) at 42 GHz with 8.6-dB gain [2], and in GaAs pseudomorphic high electron-mobility transistor (pHEMT) at 50 GHz with 5-dB loss [3]. Also, other monolithic microwave (MMIC)  $V$ -band frequency doublers have been reported (see [4, Table I]), but these circuits have a limited band of operation. Indeed, their  $-3$ -dB output power bandwidth is, in the best case, around 30%. We can note for very high-frequency applications a MMIC doubler in InP HEMT at 164 GHz with 2-dB loss and 8.5% bandwidth [5] dedicated to narrow-band applications.

In this paper, we present the design, fabrication, and characterization of broad-band frequency doublers operating from dc

to 100 GHz. To implement these frequency doublers, we have chosen a Gilbert multiplier structure [6]. This double-balanced architecture allows us to achieve good fundamental and odd-harmonics rejection. We have designed three doubler versions. One of them is composed of a Gilbert cell with an input active splitter to achieve multiplication up to 100 GHz. To the authors' knowledge, this is the highest frequency of operation for a broad-band active frequency doubler in any technology.

The InP double heterojunction bipolar transistor (DHBT) technology, used for doubler fabrication, is presented in Section II, the doubler design in Section III, and measurement results up to 100 GHz and comparisons in Section IV.

Preliminary results of this study were presented in [7].

## II. TECHNOLOGY

The InP–InGaAs DHBT technology presents several attractive aspects for the fabrication of high-speed circuits.

The very high-frequency characteristics are due to excellent electron transport properties of InP and InGaAs; the small bandgap of InGaAs base results in a low turn-on voltage, which means a potential for low power consumption; the double heterojunction gives a high breakdown voltage ( $BV_{CEO} > 7$  V), necessary for large-signal applications such as optical modulator drivers; finally, the vertical technological process yields a very good built-in threshold voltage uniformity, which is very convenient for differential bipolar logics such as current-mode logic (CML) and emitter-coupled logic (ECL).

The in-house InP–InGaAs self-aligned DHBT technology was presented in [8].  $F_t$  of 150–180 GHz and  $F_{max}$  of 210–220 GHz are currently obtained on circuit-oriented devices at a current density of about 2 mA/ $\mu\text{m}^2$ . Three Ti/Au interconnection levels, TaN resistors, MIM capacitors, and spiral inductors are also available to realize the circuit layout.

In Fig. 1,  $F_t$  and  $F_{max}$  frequencies for  $2 \times 3 \mu\text{m}^2$  and  $2 \times 10 \mu\text{m}^2$  emitter transistors are compared as a function of collector current.  $F_t$  above 100 GHz and  $F_{max}$  over 170 GHz are achieved for currents of 2 mA and up. This means that low-power high-frequency operation can be targeted.

## III. CIRCUIT DESIGN

The frequency doubler is based on a Gilbert cell with both inputs connected together, as shown in Fig. 2. Frequency multiplication results in generating harmonics due to nonlinear characteristics of the transistors in the Gilbert cell.

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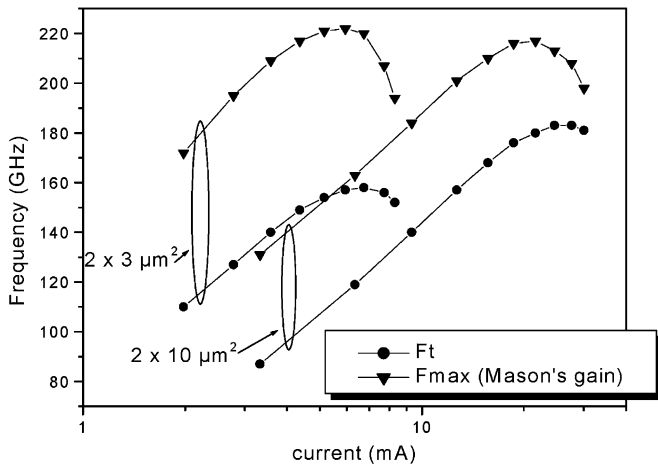


Fig. 1.  $F_t$  and  $F_{max}$  for  $2 \times 3$  and  $2 \times 10 \mu\text{m}^2$  emitter transistors.

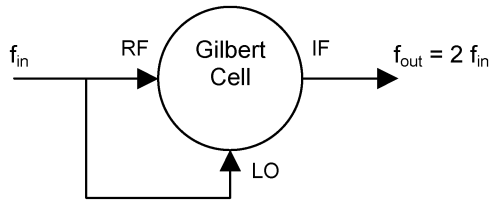


Fig. 2. Gilbert cell as a frequency doubler.

A. Electrical Design

The first goal of this design was the high frequency of operation (up to 100 GHz). Three integrated doubler versions have been designed. The first version (V1) is the usual Gilbert cell. The second version (V2) adds a peaking inductor on the output in order to improve output-doubler amplitude at high frequencies [9], [10].

Usually, frequency doublers based on the Gilbert-cell structure use an external frequency splitter to provide the necessary two symmetrical inputs. This is the case for versions V1 and V2. In the last version (V3), we decided to circumvent this problem by using an internal splitter. Only one RF input signal is thus needed plus a reference dc value (REF). Still, the design and layout of version V3 offer the possibility to work in differential mode, i.e., with two symmetrical input signals.

Doubler block diagrams are presented in Fig. 3. The top diagram represents V1 and V2 versions, while the bottom graph shows the V3 version. In this version, the IN input signal is transformed by the input active splitter into two symmetrical signals (OUT1 and OUT2). These two signals enter on RF and local oscillator (LO) Gilbert cell inputs. They are converted by the cell into an IF output signal of double frequency while the fundamental frequency is suppressed.

Fig. 4 shows electrical schemes of frequency doublers.

The first version (V1), to serve as a reference, presents two stages: the emitter followers and the Gilbert cell. The circuit is composed of two pairs of emitter followers that feed the LO lower differential pair and one emitter follower pair connected to the RF upper differential pairs (Gilbert cell). These emitter follower stages realize a level shifting and impedance matching. Frequency multiplication occurs in the differential pair stage.

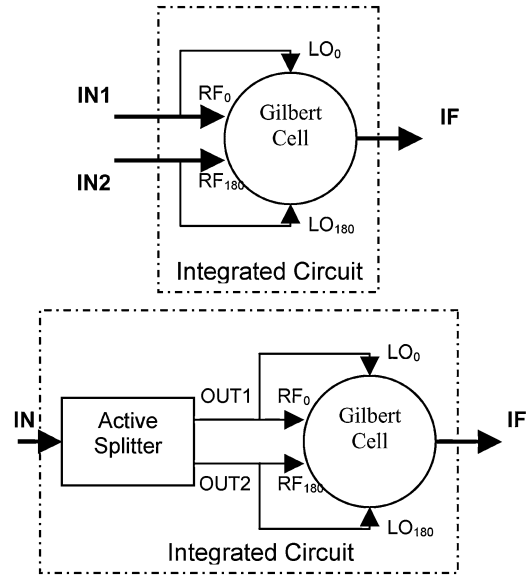


Fig. 3. Block diagrams of frequency doublers with (top) external splitter and (bottom) internal splitter.

Current mirrors act as stable current sources. All transistor sizes are optimized for the maximum frequency performance. Switch transistors (emitter size  $2 \times 10 \mu\text{m}^2$ ) operating at  $1.5\text{-mA}/\mu\text{m}^2$  collector current density are used. For biasing, larger transistors (emitter size  $2 \times 15 \mu\text{m}^2$ ) are chosen. No output buffer is used: to optimize output swing at high frequencies, the doubler output is directly connected to the Gilbert cell output. In contrast to most Gilbert cells, we have chosen to use only one Gilbert cell output to minimize layout parasitics. Even if the bandwidth power is half of that of a differential output, post-layout simulation demonstrates that, for a single-ended application, the use of an asymmetrical output architecture increases the bandwidth thanks to a strong reduction of output parasitic capacitances.

The peaking inductor of the second version (V2) has been realized with a grounded coplanar waveguide (GCPW) line. The GCPW line equivalent inductance is about 200 pH.

The active splitter of the third version (V3) is composed of a differential amplifier with feedback resistors that provides broad-band amplification (Cherry-Hooper topology [11]). Emitter degeneration is used in the amplifier to linearize output splitter signals.

B. Layout Design

A microphotograph of the V3 doubler circuit is presented in Fig. 5. The chip dimensions are  $1400 \times 1600 \mu\text{m}^2$ .

Signal lines (two inputs) are fed via matched  $50\text{-}\Omega$  GCPW lines. Similarly, the output signal is connected to output pads with  $50\text{-}\Omega$  GCPW lines. The signal part of the layout is compacted to shorten high-frequency paths. The circuit core is optimized for minimum wire length and maximum symmetry. The core footprint is  $250 \times 350 \mu\text{m}^2$ . DC-bias connections are decoupled on-wafer with RC circuits.

As mentioned before, this circuit can be fed with two symmetrical input signals. Indeed, the GCPW line has been used on the REF pad to allow operation with both internal and external splitter modes.

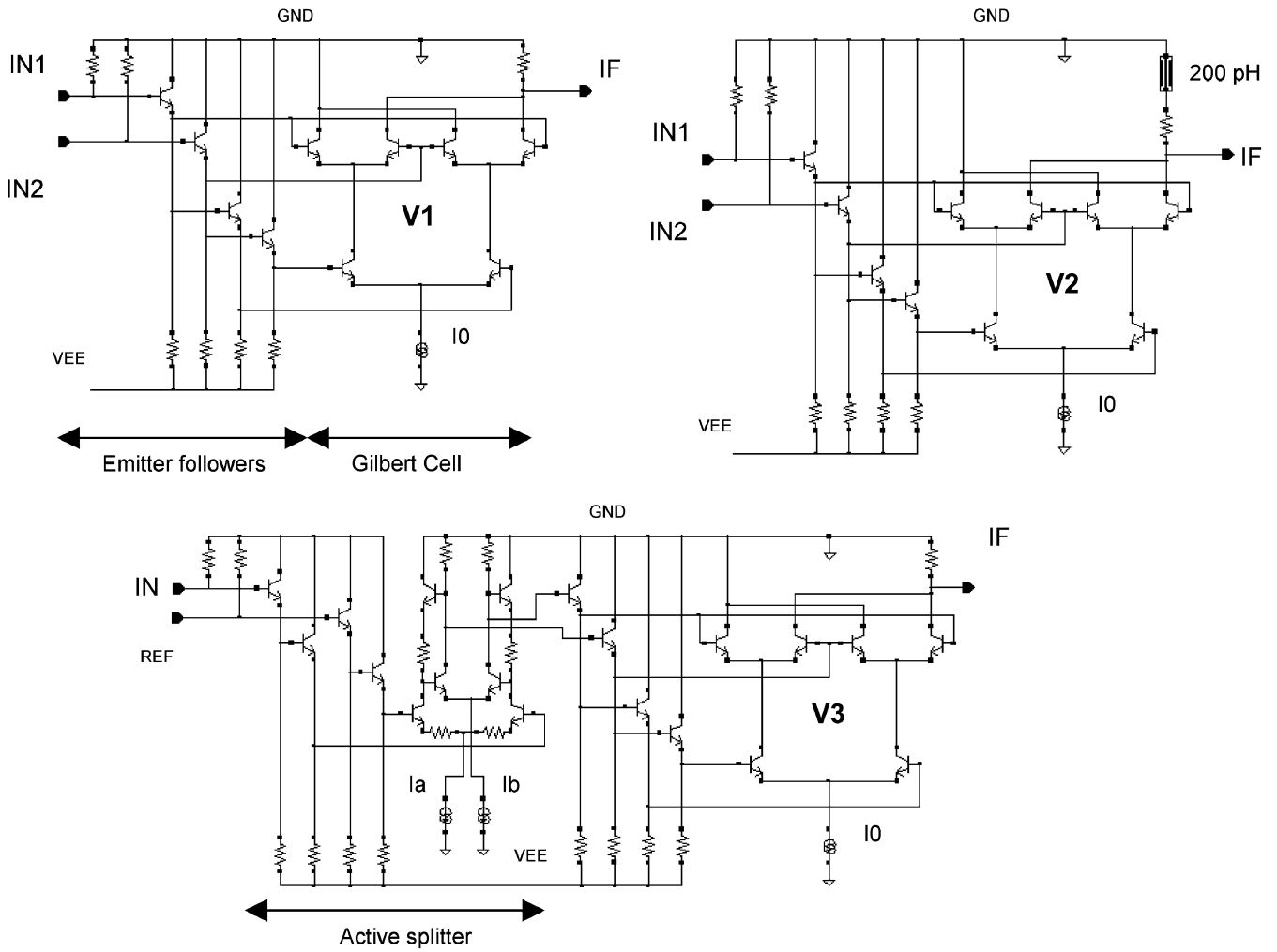


Fig. 4. Electrical schemes of frequency doublers. (V1) Reference doubler. (V2) Doubler with peaking inductor. (V3) Doubler with active splitter.

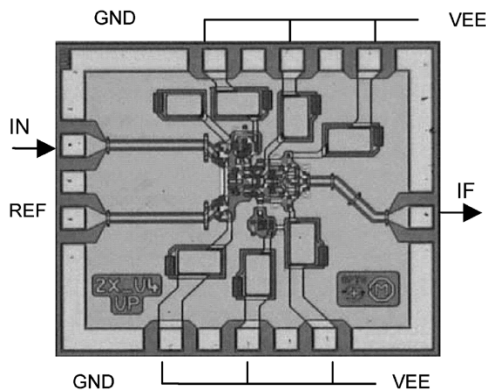


Fig. 5. Microphotograph of the fabricated V3 doubler.

IV. MEASUREMENT RESULTS AND COMPARISONS

After presentation of simulation tools and measurement equipment, V1 and V2 doubler measurements are shown and compared with simulations. Next, a comparative performance graph between the three versions is given. Finally, results of the best version are detailed.

A. Simulation Tools and HBT Model

The design of integrated circuits (ICs) operating at very high frequencies needs adequate methodology at the electrical as well as at the layout level.

To evaluate correct operation, precise transient simulations have been used. These simulations should be based on correct models for active, passive, and parasitic elements.

Particular attention has been paid to transistor models. Limitations of the popular Gummel-Poon bipolar transistor model when applied to III-V compound transistors are now well identified.

In the presented design, we used the University of California at San Diego (UCSD) HBT model which allows us to implement the most important features of III-V compound transistors necessary for the correct simulation of high-speed circuits [12], [13].

B. Measurement Setup

The characterization of the frequency doubler requires adequate measurement equipment as well as special care in the measurement setup. The doubler characteristics were measured using on-wafer probing and bias lines. The measurement setup is composed as follows.

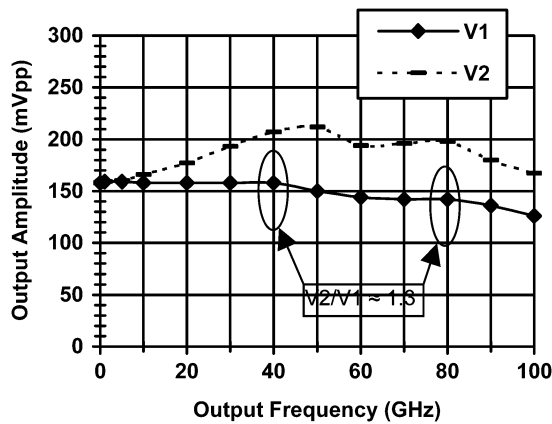


Fig. 6. Simulated V1 output amplitude and V2 output amplitude versus output frequency. Input power is  $-8$  dBm.

A frequency synthesizer provides a signal up to 60 GHz. Output signal waveform is displayed on an oscilloscope.

The 65-GHz probes are used at the circuit output. Measurements are realized with a remote sampling head (70 GHz) and very short cables. The use of a precision timebase module allows us to characterize precisely the time jitter of the doubler.

It is clear from the equipment characteristics that, above 70 GHz. Our measurements are cumulating hard-to-estimate losses from different measurement elements (e.g., probes, cables, and sampling head). Indeed, e.g., the sampling head data sheet shows the frequency response up to 70 GHz. At 70 GHz, head losses are about 2.6 dB, but it is very difficult to extrapolate its behavior above 70 GHz. In the best case, extrapolation is linear, but, in the worse case, a bandwidth hole may appear, and, thus, losses can be very important. Measurements were realized in spite of these limitations. In consequence, experimental results above 70 GHz cannot be guaranteed, but we can estimate the actual bandwidth of the doubler as higher than the measured one.

V1, V2, and V3 doublers were characterized by applying RF signals on IN1 and IN2 pads (external splitter mode). V3 was characterized also by applying an RF signal on IN1 (IN) pad and a dc reference voltage signal on IN2 (REF) pad (internal splitter mode).

The VEE bias voltage was  $-4.5$  V.

### C. Inductive Peaking Effect

In this section, we present results from the inductor addition on the output of the Gilbert cell. Fig. 6 shows simulation of V1 and V2 output amplitudes' output frequency.

Above a 20-GHz output frequency, inductive peaking effect is important. For  $-8$ -dBm input power, V1 amplitude is around 150 mV<sub>pp</sub> whereas V2 amplitude is around 200 mV<sub>pp</sub>.

V1 and V2 doublers have been measured at 40 and 80 GHz (output frequency). Comparison between simulated and measured V2 and V1 output amplitude is shown in Fig. 7. Inductive peaking effect on output amplitude in the frequency range 40–80 GHz can be summarized as multiplication by a factor of 1.3, which agrees with the simulation.

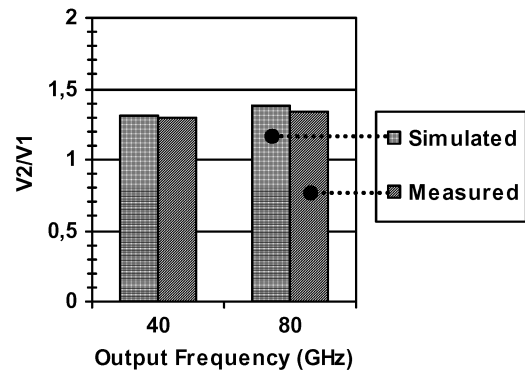


Fig. 7. V2/V1 output amplitude ratio versus frequency: inductive peaking result.

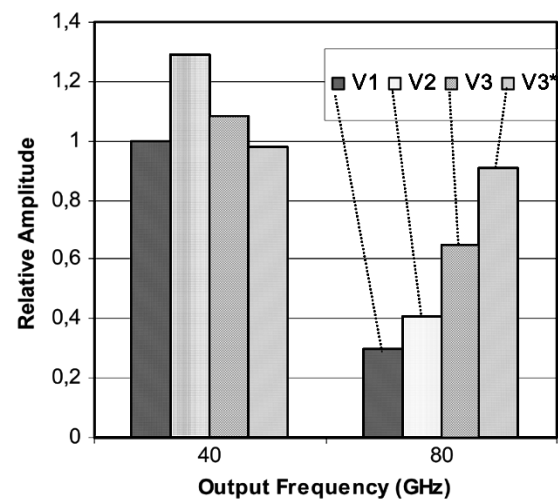


Fig. 8. Doubler performance measurement comparison. V1, V2, and V3 differential mode; V3\* reference mode.

### D. General Comparison

Fig. 8 summarizes the measured performance of different doubler versions. Reference output amplitude is 158 mV<sub>pp</sub> and input power  $-8$  dBm.

As pointed out before, we observe a V2 amplitude increase (1.3) due to inductive peaking.

Let us analyze the effect of the active splitter. Two measurement modes of V3 were realized: V3 (external splitter mode—differential operation) and V3\* (internal splitter mode—referenced operation). We can note that the ratio between V3 and V3\* changes from 40 to 80 GHz. The V3\* mode of operation is more advantageous for higher frequencies. The explanation of this fact is as follows: when operating with an external splitter (V3\*), we need cables and delay lines which have a limited bandwidth. These additional elements induce signal degradation at higher frequencies, making operation with an internal splitter more advantageous. However, at lower frequencies (40 GHz), differential operation results in better output signal amplitude than does the referenced one. At 80 GHz, we observe a V3\* amplitude increase of factor 3 compared to the reference version V1.

We can note a large difference between measured and simulated V1 and V2 amplitudes at 80-GHz output frequency. This is

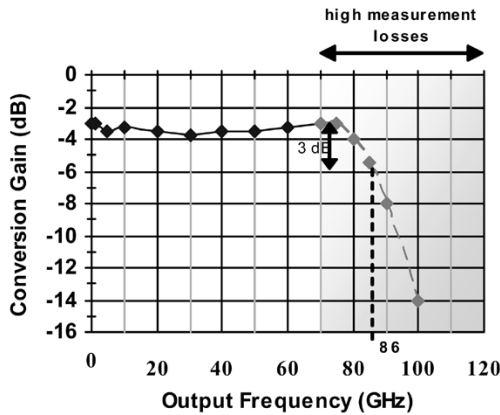


Fig. 9. Measured conversion gain versus output frequency for  $-8$ -dBm input power ( $V3^*$ ).

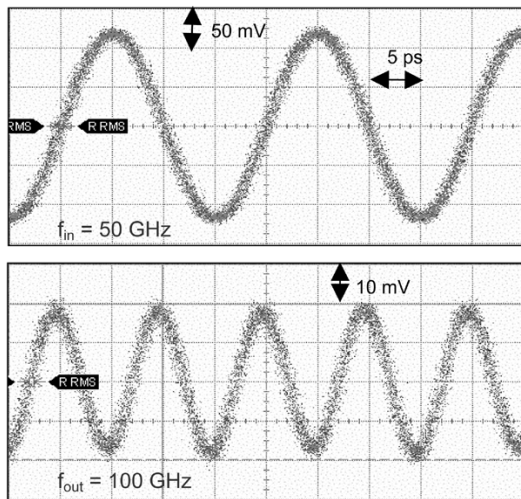


Fig. 10. Measured (top) input and (bottom) output waveforms at 100 GHz ( $V3^*$ ).

mainly due to bench losses for frequencies greater than 70 GHz. In fact, these discrepancies demonstrate that, when an external splitter is used ( $V1$ ,  $V2$ , and  $V3$ ), a strong attenuation is measured between 40–80 GHz, while the referenced doubler ( $V3^*$ ) is nearly constant over this band.

$V1$  and  $V2$  frequency doublers consume 150 mW. The  $V3$  frequency doubler consumes 730 mW shared between the active splitter (580 mW) and the multiplier (Gilbert cell) core (150 mW).

#### E. Measurements of a Doubler With an Active Splitter

Following the reported comparison, more in-depth measurements were carried on the active splitter doubler with internal splitter mode ( $V3^*$ ).

In Fig. 9, the conversion gain versus output frequency is shown for  $-8$ -dBm input power.

As already mentioned, above 70 GHz, the conversion gain is certainly underestimated because of measurement bench losses. The actual 3-dB bandwidth is then greater than the measured dc–86 GHz.

Fig. 10 shows the 50-GHz input signal and the 100-GHz output signal of the  $V3^*$  frequency doubler. The rms timing

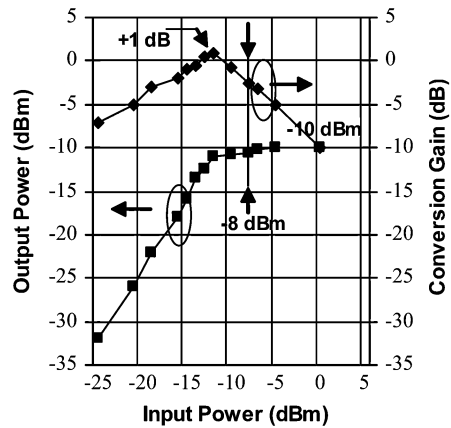


Fig. 11. Measured output power and conversion gain versus input power at 60 GHz ( $V3^*$ ).

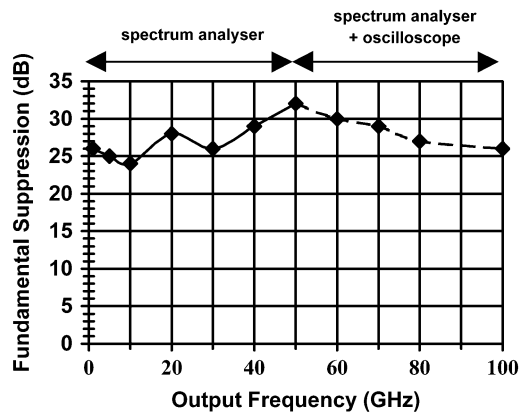


Fig. 12. Measured suppression of fundamental frequency versus output frequency ( $V3^*$ ). Input power is  $-8$  dBm.

jitter of the output signal is 390 fs, which is comparable to the 420-fs rms timing jitter of the input signal. Due to measurement bench losses, the actual output signal amplitude is greater than the measured  $41 \text{ mV}_{pp}$ .

In Fig. 11, output power and conversion gain versus input power are presented at 60 GHz. For input power values larger than  $-12$  dBm, the doubler is in saturation mode. The maximum output power is  $-10$  dBm. A maximum of  $+1$ -dB gain is achieved at  $-12$ -dBm input power.

In Fig. 12, we now present measurements of fundamental suppression in the whole frequency range of operation.

The fundamental and second harmonic are measured using a spectrum analyzer up to 50 GHz. Above 50 GHz, fundamental power is measured with spectrum analyzer and second-harmonic power is measured as an oscilloscope output waveform.

Up to 100 GHz, the fundamental signal is suppressed to the desired spectrum with more than 24 dB. The circuit presents an optimum rejection of fundamental signal of 32 dB at 50 GHz.

## V. CONCLUSION

In this paper, we presented the design, fabrication, and characterization of broad-band frequency doublers operating at the

upper limit of the state of the art in the dc-100-GHz frequency range. A Gilbert cell with integrated active-splitter architecture allowed us to obtain such a high frequency of operation. The fundamental signal suppression in the whole frequency range is better than 24 dB. At 60 GHz, the maximum conversion gain is 1 dB. These results were obtained in spite of measurement equipment limitations. Also, combination of inductive peaking and active splitting on the same frequency doubler should further enhance the doubler performance.

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