Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test

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Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test*†

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Abstract. This paper presents the results of resistive-open defect insertion in different locations of Infineon 0.13 μm embedded-SRAM with the main purpose of verifying the presence of dynamic faults. This study is based on the injection of resistive defects as their presence in VDSM technologies is more and more frequent. Electrical simulations have been performed to evaluate the effects of those defects in terms of detected functional faults. Read destructive, deceptive read destructive and dynamic read destructive faults have been reproduced and accurately characterized. The dependence of the fault detection has been put in relation with memory operating conditions, resistance value and clock cycle, and the importance of at speed testing for dynamic fault models has been pointed out. Finally resistive Address Decoder Open Faults (ADOF) have been simulated and the conditions that maximize the fault detection have been discussed as well as the resulting implications for memory test.

Keywords: memory testing, dynamic faults, address decoders, core-cells

1. Introduction

Functional faults traditionally employed in RAM testing, such as stuck-at, transition and coupling faults [9] are nowadays insufficient to give correct models of the effects produced by some defects that may occur in VDSM technologies. Advances in process manufacturing densities and memory architectures have carried the development of new fault models, which are tightly linked to the internal memory structure [1–3, 10, 20, 23]. These faults are not directly detectable with standard March algorithms and thus they need specific test sequences and, in some cases, *at-speed*

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tests, which are necessary especially for delay fault detection.

Many links have been established between delay faults and resistive-open defects [5, 14]. Resistive-opens generally cause timing-dependent faults. A two-pattern sequence is usually necessary to sensitize the faults, but, in contrast with stuck-open faults, detection of resistive-opens should be performed at-speed.

The occurrence of resistive-open defects has considerably increased in recent technologies, due to the presence of many interconnection layers and an ever-growing number of connections between each layer. In particular in [16] Intel reports that open/resistive vias are the most common root cause of test escapes in deep-submicron technologies.

Hence resistive-open defects are the primary target of this study. Resistive defects have been injected in the Infineon 0.13 μm synchronous embedded-SRAM family with the main purpose of verifying the presence of timing-dependent faults. Due to the internal self-timed architecture, two types of timing-dependent faults can be identified:

– Faults whose effect appears after more than one operation. The detection of these faults depends on the clock speed. We have investigated the presence of such faults by inserting resistive-opens in several locations of the memory core-cell.
– Faults affecting the memory external timings. These faults originate from defects in the non-self-timed parts of the memory periphery, thus they depend on input signals timings. In particular we have investigated the effects of resistive defects in the address pre-decoder.

For both types of faults, electrical simulations have been performed with many parameters such as defect size, supply voltage, operating temperature and process corner. Results reported in this paper demonstrate the sensitivity of embedded SRAMs to resistive-open defects and provide a characterization of these defects in terms of timing-dependent fault detection.

In Section 2 the simulation flow is described. Section 3 shows the most relevant results with regard to the identified fault models for each injected defect. Test implications are discussed in Section 4. Finally, Section 5 summarizes the results of the study and gives some directions for future works.

2. Simulation Flow

All electrical simulations have been performed with the Infineon internal SPICE-like simulator. A reference 8 K $\times$ 32 memory structure has been considered, organized as an array of 512 word lines $\times$ 512 bit lines. In order to reduce the simulation time, the simulations have been performed using a simplified version of the memory circuit that includes a reduced set of core-cells and all peripherals of the memory as pre-charge devices, sense amplifiers, write drivers, output buffers and the column and row address decoders.

2.1. Core-Cell Simulations

Several resistive-open defects have been analyzed in the memory core-cell. Fig. 1 depicts the scheme of a standard 6-transitors cell with six different resistive-open defects. The first criterion for the choice of the defect location is layout dependent. The defects have been injected in correspondence with the interconnections where there is a higher probability of their presence. Moreover, some locations have been discarded due to the symmetry of the structure. For example we have considered the defects only on one of the two inverters.

The whole operating environment range has been selected in order to maximize the fault detection probability. Hence simulations have been performed by the variation of the following parameters:

- Process corner: slow, typical, fast
- Supply voltage: 1.35 V, 1.5 V, 1.6 V
- Temperature: -40°C, 27°C, 125°C

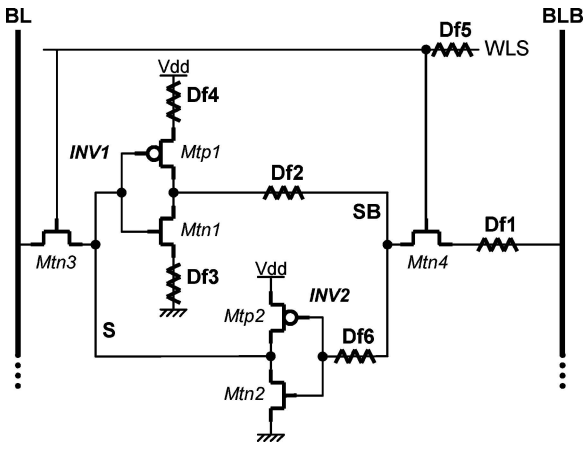

Fig. 1. Resistive-open defects injected in the memory core-cell.

- Resistance values have been chosen from few Ωs up to several MΩs since a large range of possible values have been reported [19].

When we have identified a timing-dependent behavior, we have performed more precise simulations in order to explore the connections between fault and memory timing parameters, such as clock cycle and address setup time.

2.2. *Address Decoder Simulations*

When a resistive-open defect appears between gates (inter-gate defects), it produces faults that can be detected by standard March tests. When the defect is located inside the gate (intra-gate defect) and in particular in the parallel plan of transistors, it produces dynamic fault due to its sequential behavior [21]. Referring to the NOR-gate of Fig. 2, such a defect has been located in the drain of transistor TN1 and it may produce a delay during the pull-down of node ZA0. This fault is a dynamic one because it needs a specific sequence of operations (read and write) with a specific address sequence.

In the memory under study, only the X and Y predecoders are subject to this fault, since the remaining part of the decoder is activated by an internally generated enable signal and is thus insensitive to the specific address sequence. Hence a resistive defect has been injected in the pull-down path of the NOR-based word line pre-decoder. Referring to Fig. 2, the fault has to be sensitized by applying a $0 \rightarrow 1$ transition on the A0 input, and keeping A1 at zero. This means that WL0 is selected, followed by WL1. Normally when a new word line is selected the previous one is automatically de-selected. If a resistive defect is present, the ZA0 output may stay high for more than one access cycle, due to a memory effect of the node ZA0. The consequence is that WL0 remains selected a certain time (depending on the defect size) when WL1 is selected.

The following sequence has been used to sensitize and detect this dynamic fault:

– *Sensitization*: Write d at WL0, Write $\bar{d}$ at WL1;
– *Detection*: Read WL0. d is expected.

This sequence, originally proposed in [20], will be always called Sachdev-like sequence in the rest of this paper.

A possible alternative (March-like sequence) has also been considered:

– *Sensitization and detection*: Write d for each WL, read d and write $\bar{d}$ for each WL.

The interest of the latter sequence is that it could be integrated in industry-standard March C- tests [15] by using a proper address generator, e.g. the LFSR reported in [18]. The March-like sequence sensitizes and detects the fault during a read operation. In other words there is a double faulty access to two cells with different stored values, during a read operation. Since conflicting values are driven on the bit lines and the final fault detection is uncertain. Detailed simulations have confirmed that the fault detection

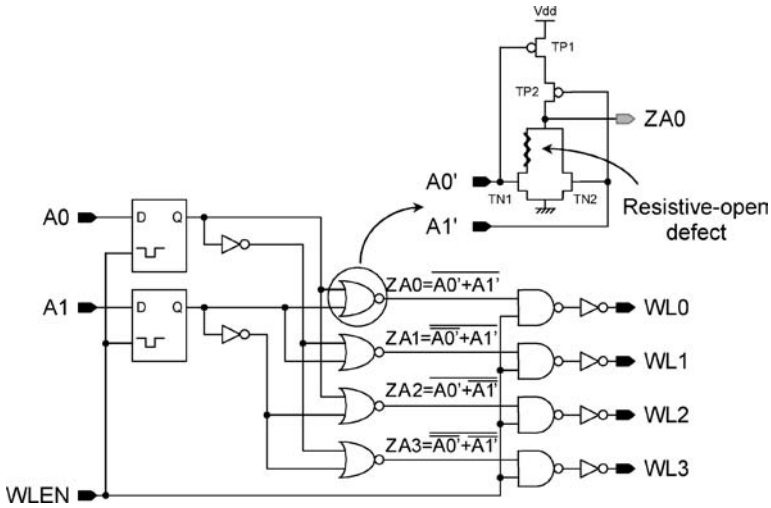

Fig. 2. Intra-gate resistive-open in the pull-down path of NOR-based address pre-decoder.

reliability is very low, while the Sachdev-like sequence is very effective. Therefore we have disregarded the March-like sequence found in bibliography and we have applied only the Sachdev-like sequence for our study.

3. Simulation Results

In the following, the most significant simulation results are presented, with particular emphasis on the detected dynamic fault models. Referring to the classification presented in [11], a fault is considered dynamic if the sequence of operations needed to sensitize it consists of more than one operation. Additionally, in order to characterize precisely the conditions which maximize the fault detection probability, we have analyzed the dependence of the detected faults on the relevant memory timings, e.g. the clock cycle time.

In the presence of resistive-open defects, the detection of a particular fault depends on environmental conditions, such as supply voltage, operating temperature and the considered process corner.

3.1. Core-Cell Simulations

The simulations have been performed with all the different PVT conditions. In Table 1 we show only the most significant results according to the conditions which maximize the fault detection, i.e. the minimum detectable resistance value. The PVT conditions have only an impact on the minimal defect size that induces a faulty behavior but not on the fault model. This means that in all the other cases not shown here, the fault models are still valid but there are related to larger defect size. All the fault models have been detected by 1w0r0 (i.e. '1' stored in the cell, a w0 operation immediately followed by a r0) or 0w1r1 sequences.

Table 1. Summary of worst-case PVT corners for the defects of Fig. 1 and corresponding minimum detected resistance and fault model.

Dfi	Process corner	Voltage (V)	Temp (°C)	Min res (kΩ)	Fault model
1	Fast	1.6	−40	∼25	TF
2	Fast	1.6	–	∼8	RDF/DRDF
3	Fast	1.6	125	∼3	RDF/DRDF
4	Fast	1.6	125	∼130	Dynamic RDF
5	Fast	1.6	−40	100/140	IRF/TF
6	Fast	1.6	125	∼2 MΩ	TF

In this table the first column (Dfi) indicates the defect location in the core-cell. The following four columns correspond to the electrical parameters which maximize the fault detection. The last column gives the corresponding fault models that have the following definitions:

- *Transition Fault (TF)*: A cell is said to have a TF if it fails to undergo a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written.
- *Read Destructive Fault (RDF)* [2]: A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output.
- dynamic Read Destructive Fault (dRDF) [11, 13]: A cell is said to have an dRDF if a write operation immediately followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output.
- *Deceptive Read Destructive Fault (DRDF)* [2]: A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell.
- *Incorrect Read Fault (IRF)*: A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell.

A general result is that fault detection is usually better at high voltage with a fast process, while it can greatly vary with the operating temperature. When a fast process is adopted, high supply voltage makes the memory surprisingly less stable than a lower supply voltage. This unexpected phenomenon is a consequence of the decrease of stability of the core cell due to the fast process that maximizes the leakage and the threshold voltage. For high supply voltage, the commutations become quicker as the voltage difference gets higher. In this condition the cell is more sensitive to any perturbation. Moreover leakage is enforced at high temperature while voltage threshold is minimal at low temperature. The presence of effects of second or third order does not make it easy to determine exactly which of them is predominant.

Defects in the Cell Pull-Down. A resistive defect in the pull-down path of one of the core-cell inverters (Df3 in Fig. 1) may cause a destructive read operation [2]. The read value can be wrong or correct, thus a second

read access is necessary to detect the fault (*deceptive destructive read*).

The impact of the defect on memory robustness has been taken into account since the fault detection is more or less reliable depending on the voltage difference between BL and BLB during the read access (referred to as ΔBL). As a reference for this technology, we consider a "good" absolute value of ΔBL to be higher than 80 mV. When ΔBL is lower than 80 mV a wrong value can be read during the access because of transistor mismatches in the sense amplifier or for low-drive core cell. Nevertheless, since these effects are not taken into account in standard "perfect" Spice simulations, the simulated read value will always be the correct one. Hence it is extremely important to characterize the impact of the defect also in terms of variations of ΔBL compared to its reference value.

The simulation results, in presence of Df3, are shown in Fig. 3 for a typical process at room temperature and 1.5 V supply voltage. Still referring to the notation presented in [11], the operation sequence considered here is: 0w1r1 ('0' previously stored, operation of w1 and r1). However this read disturb fault can be considered static, since the single-operation sequence 1r1 has shown the same sensitization effect. Likewise, additional read accesses did not improve the fault detection.

It is important to note that, even though a destructive read (a.k.a. read disturb) takes place for resistance values higher than $\sim$7 kΩ, the reduction in ΔBL affects the memory robustness starting from a value of $\sim$4.5 kΩ. Besides, in the entire RDF region corresponding to a read disturb fault, the fault detection is considered uncertain, because ΔBL is consistently lower than the 80 mV "safe" value. Thus a second read access is always necessary to ensure proper fault detection, regardless of the simulation outcome. A deceptive read disturb is also identified in simulation for a resistance value of 7.5 kΩ.

Defects in the Cell Pull-Up. A resistive defect in the pull-up path of one of the core-cell inverters, as Df4 in Fig. 1, is a classic hard-to-detect fault [11]. When a defect is on Mtp2 source, a *dynamic Read Destructive Fault* occurs when a zero is stored in the cell. A '0' stored correspond to a '0' on node S and a '1' (VDD) on node SB, see Fig. 1.

The first step of the read operation is the precharge at VDD of BL and BLB. Then the cell is connected to the bit lines, the word line signal actives transistors Mtn3 and Mtn4, which are switched on. BLB and node SB are at same potential, while BL and node S have a different potential. As BL has a high capacitance, its discharge is long. So, we can consider that BL and BLB values remain at VDD at the beginning of the read operation. Moreover, the current in Mtn3 is high due to the voltage difference between BL and S (see Fig. 4). The S node is thus charged a little ($0 + \delta$V). As the value at the inverter input has slightly increased, the value at its output (SB) decreases because Mtp2 cannot compensate this leak of charge due to the resistive defect. Consequently, SB voltage decreases a little (VDD $-$ δ V) causing the degradation of the logic '0' on S. If SB value becomes close to VDD/2, there is a swap of the value stored in the cell. Note that, in normal condition, when there is not a resistive defect in the pull-up path, the current in the Mtp2 transistor is sufficient to maintain the SB node close to VDD.

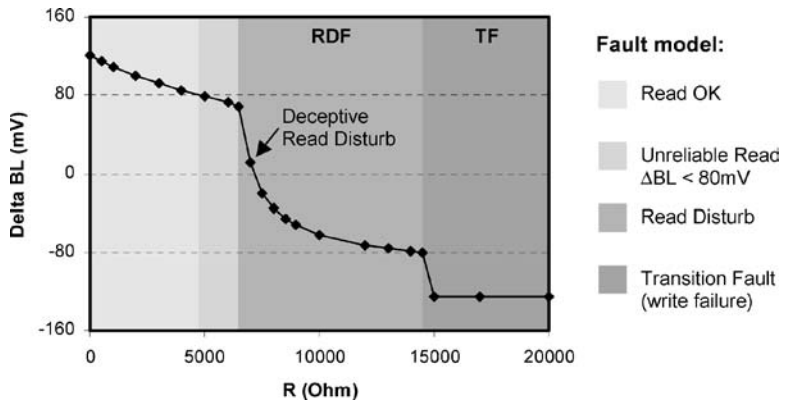

Fig. 3. Variation of ΔBL during read as a function of injected resistance value (Df3).

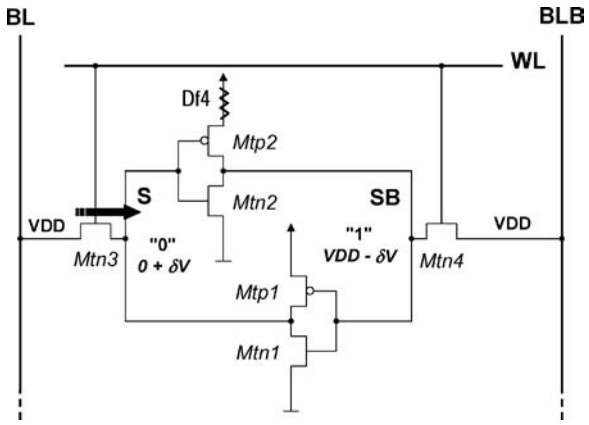

Fig. 4. Effect of Df4 during a read '0' operation.

When in the faulty cell is stored '1' and a '0' is written just before a read operation, the cell loses its content more easily. Actually, after the w0 operation, SB does not have enough time to reach VDD and it begins to discharge when it is not at an actual '1' logic. If the defect is sensitized by a write operation followed by a read access, the corresponding fault model is a *dynamic Read Destructive Fault*. If the cell flips after several reads, it is a *dynamic Multiple-Read Destructive Fault*. Before the destruction of the cell content, the SB level is slightly degraded after each read (see Figs. 5 and 6).

Thus, depending on the resistance value, the fault is detected by a different sequence. In Fig. 5, a 10 MΩ resistance is sensitized by a Write-Read sequence, while a 3 MΩ resistance needs a Write-Read-Read operation series. A resistance value if 1 MΩ is never detected at this clock frequency.

Therefore the detection of this defect can be improved by a series of read operations performed at high speed. The simulation waveforms in the typical process corner, at 125°C temperature and 1.6 V supply are shown in Fig. 6. Here a 1.5 MΩ resistive defect produces a read disturb fault after the fifth consecutive read access performed *at-speed* (cycle time = 3 ns). The sensitization sequence for this fault is $1w0(r0)^5$, i.e. a w0 followed by five r0. This fault can thus be regarded as a *dynamic Multiple Read Destructive Fault*, and it is an extension of the *dynamic Read Destructive Fault* already reported for e-DRAMs [4]. Note that the memory data output is still correct during the fifth read, so that an additional read operation is necessary to observe the fault (*deceptive Multiple Read Destructive Fault*).

In general, the dependence of dRDF has been studied in relation to the cycle time and the defect size. The results are presented in the graph of Fig. 7 where each point corresponds to a determined couple (cycle time, defect size) and is placed in a certain area corresponding to a sensitization sequence like $1w0(r0)^N$, where $N = 1$ to 5.

The graph in Fig. 7 clearly shows that the minimum detected resistance value largely depends on the length of the clock cycle. The range for the resistance value is about between some hundreds Ω up to 10 MΩ, so

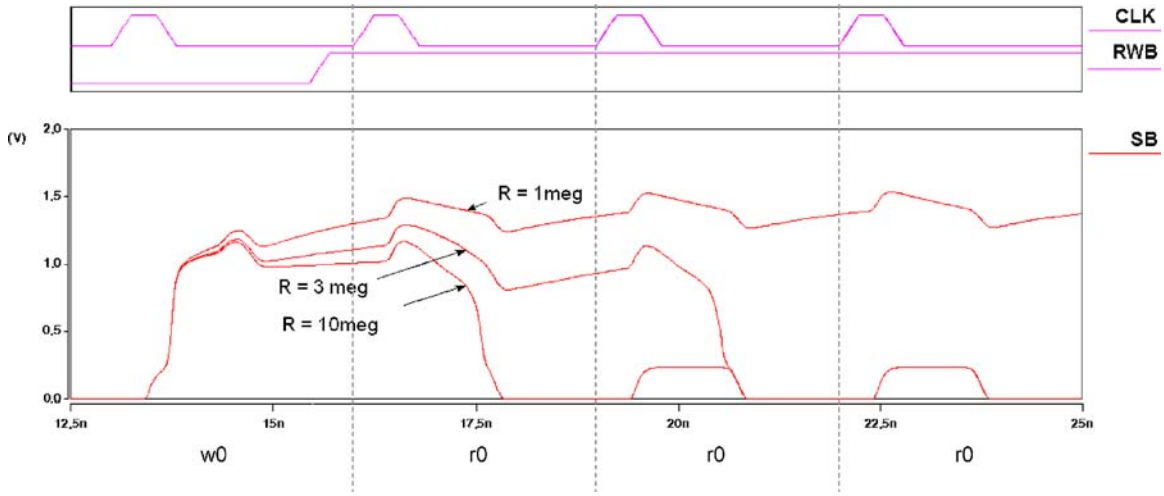

Fig. 5. A destructive read occurring after consecutives "at-speed" read access (typ proc, $T = 125°C$, $V = 1.6$ V, $T_{cyc} = 3$ ns).

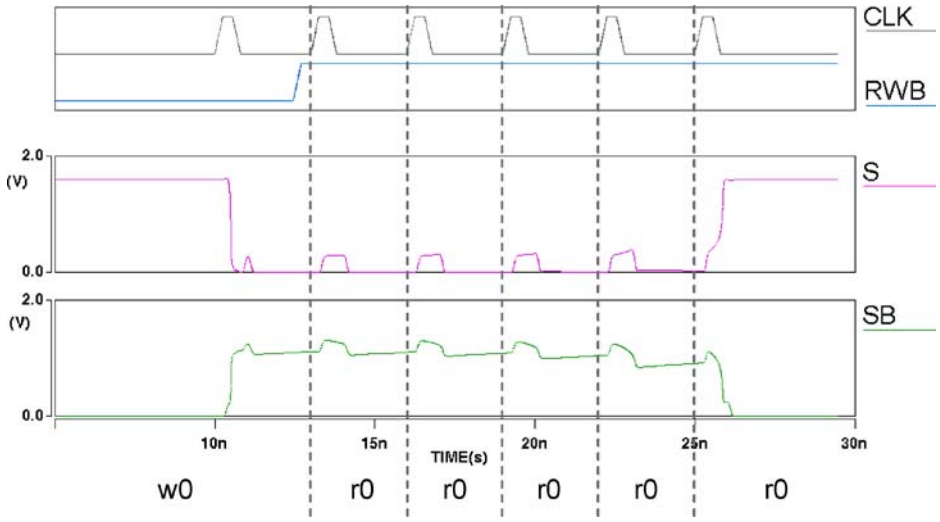

Fig. 6. A destructive read occurring after the 5th consecutive "at-speed" read access (typ proc, $T = 125°C$, $V = 1.6$ V, $T_{cyc} = 3$ ns, $R = 1.5$ MΩ).

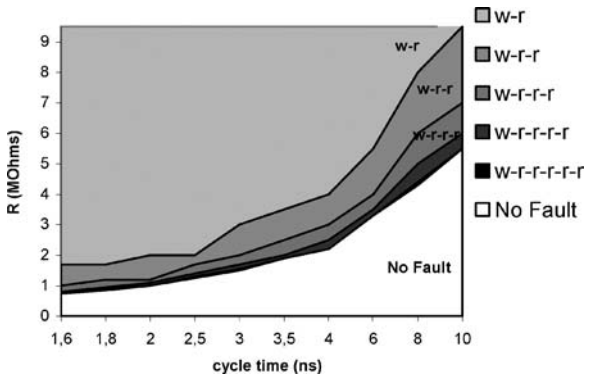

Fig. 7. Defect detection as a function of cycle-time for different sensitization sequences (typ proc, $T = 125°C$, $V = 1.6$ V).

one order of magnitude occurs in the processed window for the resistance variation. Besides, even at the highest simulated speed (i.e. 1.6 ns, which is the minimum clock cycle for the memory under study), it can be observed that the fault detection can still be improved by a factor of ∼2X by applying a series of 4–5 consecutive reads. It is also interesting to note that this fault can equivalently be represented as a degradation of the memory minimum cycle time.

Finally, the "dynamic" nature of the fault is confirmed by the fact that a fully static read test (i.e. a 0r0 sensitization sequence) is able to detect only faults produced by high resistance values, larger than 140 MΩ.

3.2. Address Decoder Simulations

The outcome of a simulation of a 50 kΩ resistive defect injected in the pull-down path of one of the NOR gates of the word line pre-decoder is shown in Fig. 8. During the first cycle, WL0 is addressed and the corresponding NOR-gate output (ZA0 in the graph and in the scheme of Fig. 2) is '1' logic. This first access produces a w1 at WL0. During the second cycle, WL1 is accessed (ZA1 is activated, '1' logic), but, due to the presence of the defect, ZA0 remains still high. Consequently both WL0 and WL1 are selected and the '1', that is written in the cell addressed by WL1, overwrites the '0' that was previously stocked at WL0. Hence the final access at WL0 will read a '1' instead of the expected '0'.

In presence of stuck-open faults in the address decoder (a.k.a. SOAFs or ADOFs) are always detected by applying a proper address switching sequence, the detection of resistive-opens depends on the resistance value and the access speed. In particular the presence of a resistive-open is equivalent to a degradation of the address setup time for a particular address sequence. This effect is confirmed by the graph of Fig. 9, where the detected resistance value is given as a function of the address setup time. Interestingly enough, the fault detection does not depend on the clock cycle time since the fault is sensitized in the memory cycle immediately following the address change. However, if the addresses are generated by registers, which are clocked on a certain clock edge, an increase in the clock speed

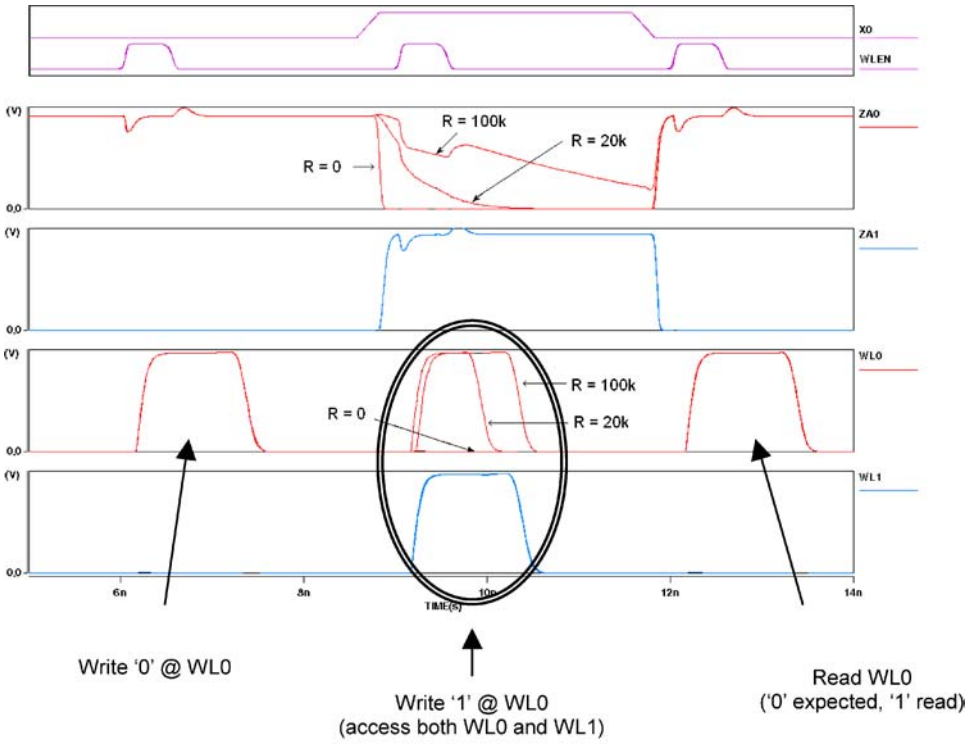

Fig. 8. A resistive-open fault in the X address decoder sensitized by a Sachdev-like sequence ($T_{cyc} = 3$ ns, $T_{Asetup} = 0.3$ ns, $R_{defect} = 50\,k\Omega$).

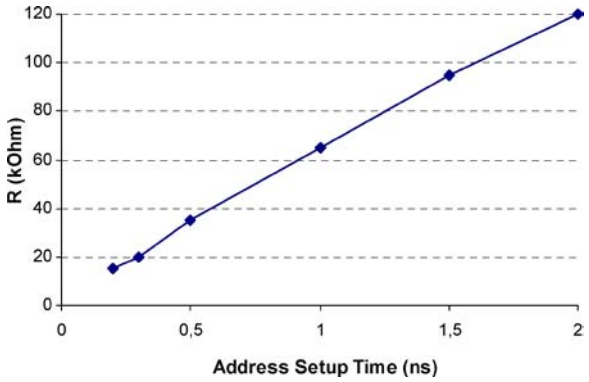

Fig. 9. Minimum detected resistance vs. address setup time (typ proc, $T = 27°C$, $V = 1.5$ V).

would also decrease the address setup time, thus improving the fault detection.

4. Implications for Memory Test

The results obtained during the simulations performed for this study have shown the importance of resistive-open defects in SRAM memories. In particular, among the numerous fault models related to the injected defects it is interesting to put the attention on those that involve a dynamic behavior because of their hardness of detection. In the following sub-sections we introduce some elements of our consequent works on this subject and the efficient test solutions developed for ADOFs and dRDF detection.

4.1. Address Decoder Open Fault

Several test solutions can be used for ADOFs and resistive-ADOFs detection but March tests remain the most attractive solution due to their linear complexity and effectiveness for detection of a large number of other faults. However, March tests are constructed essentially for the detection of static faults such as stuck-at and transition faults. ADOFs and resistive-ADOFs are not targeted by such test algorithms due to their dynamic nature and thus require either new algorithms or some modifications in existing algorithms.

As mentioned in Section 2, ADOF detection requires a specific address sequence in order to sensitize all the faults. This is done by using an address sequence

including all the pattern pairs with an Hamming distance of 1. The Sachdev-like sequence includes this property. The basic idea proposed in [7] consists in developing new March elements having the same properties than the operations (read and write) used in the Sachdev-like sequence as well as the specific address sequence. These new March elements are able to detect all ADOFs and resistive-ADOFs without sensitization and observation problems.

An extension of this study was presented in [6] where we propose to embed in the March C- the properties of these new March elements. The reformulation of the March C-, called March iC-, is essentially based on introducing a particular address sequence and a particular read/write data sequence making it able to detect ADOFs and resistive-ADOFs. We also show that these modifications do not change the complexity and, in particular, the ability of March C- to detect the faults initially covered by this algorithm (SAFs, TFs, coupling faults, AFs).

4.2. Dynamic Faults in the Core-Cell

Among the known dynamic faults that may affect SRAM memories, we also concentrate on those that concern the core-cell. One of these faults is the dynamic Read Destructive Fault (dRDF). It has the following behavior: a write operation immediately followed by a read operation causes the flip of the logic value stored in the cell. A possible defect that may involve a dRDF is the defect 4 in Fig. 1.

Recently, a test solution, referred as March RAW (Read After Write) [13], has been proposed to detect all single-cell dynamic faults in core-cells. Its complexity is 13N including the initialization. This algorithm detects dRDFs by March elements that perform a write operation followed by a read operation, e.g. 1w0r0. As shown before (Section 3.1) this test can be improved by applying $1w0r0^M$ sequences where $r0^M$ denotes a sequence of M successive r0 operations, e.g. $1w0r0^4$ = 1w0r0r0r0r0. In this case, the multiple read operations after the w0 allow a more efficient fault detection. However, if a large number of read operations is needed to sensitize the fault, the test complexity increases dramatically.

In [8] we have proposed a more efficient alternative to March RAW. For this purpose, we have improved the standard March C- algorithm (10N) in order to make it able to detect also dynamic faults in the core-cell. Our modified March C- detects dRDFs by using a particular address sequence. This modification is allowed by the first of the six Degrees of Freedom (DOF) [17] of March tests, and does not change the capability of March C- to detect the former target faults.

The multiple read operations can be achieved by our modified March C- by an indirect way. During a read or write operation the pre-charge circuit is turned off in the selected column; the others columns have the pre-charge left on. Consequently, all the cells on the same word line of the selected cell fight against the pre-charge circuit. In [8] we have shown that this event, that we called "Read Equivalent Stress" (RES), can be used to sensitize dRDF as actual read operations. The occurrence of a maximal number and distribution of RESs for all the cells is warranted by a simple address ordering, word line after word line.

5. Conclusions

The present study has been focused on the extraction of defect-based fault models. The primary targets have been the study of the consequences of resistive-open defect injection because this kind of defects seems to be responsible of most of delay faults and "hard-to-detect" faults in memories. Among all the identified fault models we have focused the attention on those that have a dynamic behavior. In particular a detailed analysis has been done for ADOFs and dRDF, respectively in the address decoder and in the core cell.

In order to operate a correct characterization we have identified specific test sequences for ADOFs and dRDF sensitizations. All the simulations have been performed for different values of temperature, supply voltage and process corner. Moreover, we have considered the variations of other parameters as the value of the resistance of the injected resistive-open defects and the clock cycle of the circuit. This way we have identified those conditions that maximize the fault sensitization.

The here presented investigations have been the bases for our further studies in which we have proposed efficient algorithmic solutions for the considered dynamic faults.

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