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Abstract. This paper presents an analysis of dynamic faults in core-cell of SRAM memories. These faults may appear as the consequence of resistive-open defects that appear more and more frequently in VDSM technologies. In particular, the study concentrates on those defects that generate dynamic Read Destructive Faults, dRDFs. In this paper, we demonstrate that read or write operations on a cell involve a stress on the other cells of the same word line. This stress, called Read Equivalent Stress (RES), has the same effect than a read operation. On this basis, we propose to modify the well known March C-, which does not detect dRDFs, into a new version able to detect them. This is obtained by changing its addressing order with the purpose of producing the maximal number of RES. This modification does not change the complexity of the algorithm and its capability to detect the former target faults.

Keywords: memory testing, SRAM core-cell, dynamic faults, resistive open defects, March test

1. Introduction

The silicon area dedicated to memory elements is constantly growing in recent designs. This fact is confirmed by the SIA Roadmap which forecasts a memory density approaching 94% of System on Chip (SoC) silicon area in the next ten years [10]. Therefore, memories are becoming the main responsible of the overall SoC yield. Consequently, efficient test solutions and repair schemes for memories are needed.

RAM testing is traditionally based on functional fault models such as stuck-at, transition and coupling fault models. In VDSM technologies these fault models are not sufficient to guaranty a good test efficiency. In

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fact, the improvements in manufacturing process density and memory architecture have brought new fault models as dynamic faults [2, 5] that require more than one operation in sequence to be sensitized. For this reason, dynamic faults are not directly detectable with standard March tests [7].

Among the known dynamic faults that may affect SRAM memories, we concentrate on those that concern the core-cell. One of these faults is the dynamic Read Destructive Fault (dRDF) [5]. It has the following behavior: a write operation immediately followed by a read operation causes the flip of the logic value stored in the cell. So, such a fault requires a specific read/write sequence to be detected.

Recently, a test solution, referred as March RAW (Read After Write) [6], has been proposed to detect all single-cell dynamic faults in core-cells. Its complexity is 13 N including the initialization. This algorithm detects dRDFs by March elements that perform a write operation followed by a read operation, e.g. $1w0r0$. It has been shown in [3] that this test can be improved by applying the sequence of operations $1w0r0^M$, where $r0^M$ denotes a sequence of M successive $r0$ operations, e.g. $1w0r0^2 = 1w0r0r0$. In this case, multiple read operations are performed after the write operation, allowing a more efficient fault detection. However, if a large number of read operations is needed, the test complexity increases drastically.

In this paper we propose a more efficient alternative to March RAW. Without increasing its complexity, we improve the standard March C- algorithm (10 N complexity) [4, 8] in order to make it able to detect also dynamic faults in the core-cell. The modified March C-, that we propose, detects dRDFs by using a particular addressing sequence. This modification is allowed by the first of the six Degrees of Freedom [9] of March tests, and does not alter the capability to detect the former target faults.

Multiple read operations after a write operation can be achieved by the March C- (with the address modification) for the following reason: during a read or write operation the pre-charge circuit is turned off in the selected column; other columns have the pre-charge left on. Consequently, all the cells on the same word line of the selected cell fight against the pre-charge circuit. In this paper we show that this action, that we call Read Equivalent Stress (RES), is equivalent to a read operation for the non-selected cells. In other words, a read or write operation on a certain cell involves a stress (RES) on the other cells of the same row. This phenomenon can be used for dynamic fault sensitization.

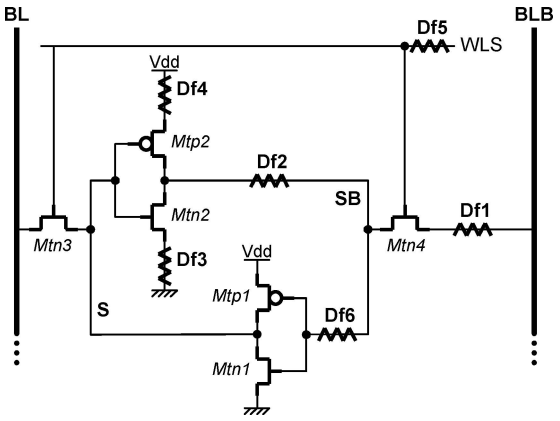

Fig. 1. Resistive-open defects injected into the memory core-cell.

The rest of the paper is organized as follows. Section 2 gives an analysis of resistive-open defects insertion in the core-cell. Section 3 provides explanations and electrical simulations of the RES phenomenon. In Section 4, a March test solution is presented. Concluding remarks are given in Section 5.

2. Dynamic Faults in the Core-Cell

In this section we present the main results of resistive-open defects insertion in the core-cell that we obtained in a study that we have started with [3]. Fig. 1 depicts the scheme of a standard 6-transitors cell where we have inserted six different resistive-open defects. They have been placed on the interconnections, where the probability of occurrence is higher. The defects are not injected into all possible locations because of the symmetry of the core-cell, the chosen six locations allow an exhaustive analysis of the resistive-open defects in the core-cell.

All the electrical simulations have been performed with the Infineon internal SPICE-like simulator. A reference 8 K $\times$ 32 memory block has been considered, organized as an array of 512 word lines $\times$ 512 bit lines. In order to reduce the simulation time, the simulations have been performed on a simplified version of the memory circuit that includes a reduced set of the core-cells and all the critical paths as pre-charge devices, sense amplifiers, write drivers, output buffer and the column and row address decoders. The whole operating environment range has been selected in order to

Table 1. Summary of worst-case PVT corners and fault models.

Defect	Process corner	Voltage (V)	Temp (°C)	Min Res (kΩ)	Fault model
Df1	Fast	1.6	−40	∼25	TF
Df2	Fast	1.6	–	∼8	RDF
					DRDF
Df3	Fast	1.6	125	∼3	RDF
					DRDF
Df4	**Fast**	**1.6**	**125**	**∼130**	**dRDF**
Df5	Fast	1.6	−40	100/140	IRF/TF
Df6	Fast	1.6	125	∼2 M	TF

maximize the fault detection probability. Hence simulations have been performed by the variation of the following parameters:

- Process corner: Slow, typical, fast (silicon dependent)
- Supply voltage: 1.35 V, 1.5 V, 1.6 V
- Temperature: −40°C, 27°C, 125°C
- Resistance values have been chosen from few ohm up to several Mohm.

In the following, the most significant simulation results are presented, with particular emphasis on dynamic fault models. Table 1 shows a summary of the fault models identified for each injected resistive-open defect, according to the conditions which maximize the fault detection, i.e. the minimum detectable resistance value. The first column gives the defect names (Df*i*). The second, third and fourth ones indicate the simulated parameters. The fifth and sixth columns give respectively the minimum resistance value that induces a faulty behavior and the related fault models. Note that the faults have been detected by $1w0r0$ or $0w1r1$ sequences. Moreover, definitions of the fault models reported in Table 1 are the following ones:

- Transition Fault (TF): A cell is said to have a TF if it fails to undergo a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written.
- Read Destructive Fault (RDF) [1]: A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output.
- dynamic Read Destructive Fault (dRDF) [5, 6]: A cell is said to have an dRDF if a write operation **immediately** followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output.
- Deceptive Read Destructive Fault (DRDF) [1]: A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell.
- Incorrect Read Fault (IRF): A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell.

A general result is that fault detection is usually better at high voltage with a fast process, while it can greatly vary with the operating temperature. When a fast process is adopted, high supply voltage makes the memory surprisingly less stable than a lower supply voltage. This unexpected phenomenon is a consequence of the decrease of stability of the core cell due to the fast process that maximizes the leakage and the threshold voltage. For high supply voltage, the commutations become quicker as the voltage difference gets higher. In this condition the cell is more sensitive to any perturbation. Moreover leakage is enforced at high temperature while voltage threshold is minimal at low temperature. The presence of effects of second or third order does not make it easy to determine exactly which of them is predominant.

Now let us detail the faults induced by the injected defects with more details. For this purpose we analyze the effects produced for different resistance sizes by each single defect. A special care is dedicated to the behavior that may involve dynamic faults that are notoriously hard to detect.

Defect 1 involves essentially a transition fault (TF) for a defect size larger than **25 kΩ**. The defect produces a delay in the operation of charging/discharging of the node SB during the writing phases. This kind of fault is static and many common March tests are able to detect it.

Defect 2 implies a RDF and in certain cases a DRDF. The defect induces a delay in the output of INV1 during the discharge of node SB. This delay may be the cause of a destructive read. During the r0 operation, BLB is pre-charged at Vdd and for a certain time it pulls-up SB that is at '0'. The capacitance of a bit line is much larger than the equivalent capacitance of cell node at SB. Moreover, the pull-up action is not well counterbalanced as expected by the pull-down action of INV1 because of the resistive defect. For this reason the read operation may cause the commutation of INV2 and so the swap of the cell. Sometimes the destruction of the stored value does not involve

an incorrect read, so it is necessary a further read operation to observe the fault.

Defect 3 produces effects similar to those of defect 2. We can add that for both the faults inducted by defect 2 and 3, RDF and DRDF, the simulations have shown that the best sequence useful for the sensitization is the $0w1r1$, not necessarily performed at speed frequency. This constraint is useful in the selection of the detection algorithm.

Defect 4 is placed in the pull up of INV1 and produces a hard to detect fault. In this case a test for static faults can detect a faulty behavior only for very large resistance values **(10 MΩ)**. The detection of the faults inducted by defect 4 can be improved by a series of read operations performed at speed. Under simulation, the sequence that allows the best fault sensitization is $1w0(r0)^n$, i.e. '1' is stored, a w0 is operated followed by $nr0$ operations [3]. At the nth $r0$ operation the stored '0' swap to '1'. The number n is connected with the defect size. This is a dynamic Read Destructive Fault (dRDF).

Defect 5 may represent the resistive effect of long connections as the word lines are. It implies an IRF for defect size larger than **100 k**Ω and also a TF for Df5 larger than **140 k**Ω. IRFs and TFs are static faults. These two faults occurs because the read and write operations need a certain minimal time to be performed. During these operations the nodes S and SB are connected to the bit lines BL and BLB by the pass-transistors Mtn3 and Mtn4. The defect involves a delay in the switching on of these two transistors reducing the operative time of the read/write operations. The read operation needs a time larger than a write one to be acted, thus the IRFs appear for littler resistance size than the TFs.

Defect 6 is at the input of INV2 and involves a transition fault (TF). The fault appears for high values of resistance **(2 M**Ω**)** because the defect is placed at the gates of the two transistors of INV2. No bias current enters in the MOS transistor gate thus the resistive defect has to be very large to generate large delay. The TF appears during the write operations. Defect 6 produces a delay for both the operations of pull-up ($w1$, '1' on BL and '0' on BLB) and pull-down ($w0$, '0' on BL and '1' on BLB) of INV2, thus the write operation may fail.

We can divide the elaborated fault models in two groups. The first one includes the dynamic fault produced by defect 4. The second group is composed by the faults induced by defects 1, 2, 3, 5 and 6. These

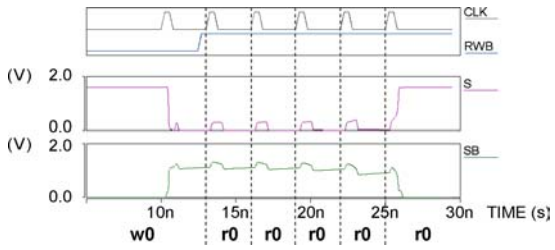

Fig. 2. A destructive read occurring after the 5th consecutive $r0$ operation (typical process, $T = 125°C$, $V = 1.6$ V, $T_{cyc} = 3$ ns, $R = 1.5$ MΩ).

faults are static. We can remark that the dynamic fault is generated by a defect that contrasts the loop of the two inverters. In fact this defect disturbs the self refreshment of the stored value. Even if defect 2, 3 and 6 are also on the loop path, they present a static behavior as accurately shown by the simulations.

On the basis of these results, a dynamic Read Destructive Fault (dRDF) occurs in presence of Df4. This fault is detectable by a read after write operation. However, in case of small defect sizes, multiple read operations are needed. This statement is confirmed by the waveforms presented inFig. 2 which shows that a sequence of five $r0$ operations, is needed to detect the fault carried by a 1.5 MΩ resistance defect.

In general, the dependence of dRDF has been studied in relation to the cycle time and the defect size. The results are presented in the graph of Fig. 3 where each point corresponds to a determined couple (cycle time, defect size) and is placed in a certain area corresponding to a sensitization sequence like $1w0(r0)^M$, where $M = 1$ to 5.

It should be observed that the minimal detected resistance value depends on the cycle time. The fault

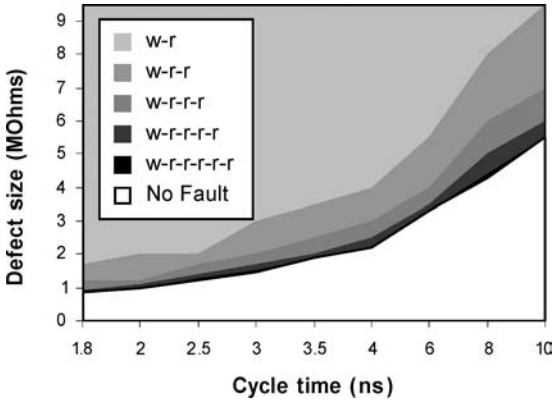

Fig. 3. Fault detection as a function of the cycle time and defect size (typical process, $T = 125°C$, $V = 1.6$ V).

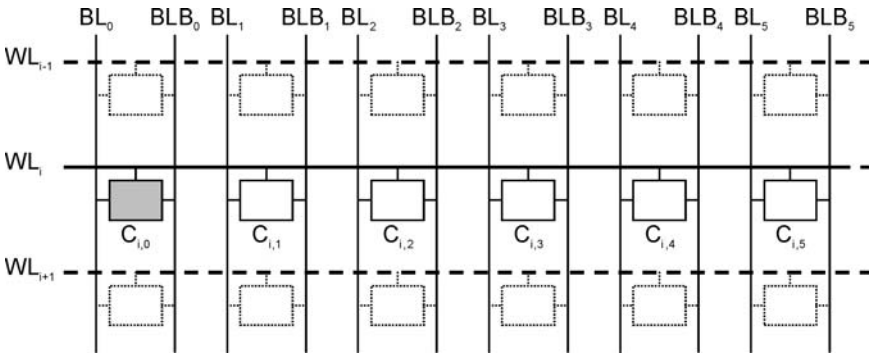

Fig. 4. A portion of an SRAM block.

detection is twice more effective when we pass from $1w0r0$ to $1w0r0^5$.

3. Read Equivalent Stress

In the previous section it has been shown that a dRDF can be the consequence of resistive-open defects in the core cell of SRAMs. In particular it has been emphasized that in presence of the resistive-open defect Df4, depicted in Fig. 1, the action of single or multiple read immediately after a write operation may cause the inversion of the value stored in the cell. In this section, we show that a cell can undergo a stress equivalent to a read operation (RES: Read Equivalent Stress) when a read/write operation is performed on other cells of the same word line. Moreover, we demonstrate that RESs are more effective to sensitize dRDFs than read operations.

For this purpose, it is useful to remember that when a cell is selected for a read or write operation the pre-charge circuit is normally turned off in its bit line. For the bit lines that are not involved in the operation, the pre-charge circuit is commonly left on. With the pre-charge active and the word line signal high on the unselected columns, the cells fight against the pre-charge circuit. A consequent deduction is that the stress produced by a read operation on a cell is equivalent to the stress caused by a read or write operation performed on whatever cell on the same word line. It is also possible that, in the latter case, the stress is larger. In fact, during a read action the perturbation of the cell is produced by the charge stored previously on its two bit lines, while in the other case the cell is stressed by the same bit line charge, but with the pre-charge circuit still on. In order to simplify what exposed above we produce the example referred to the scheme in Fig. 4.

This scheme depicts a section of an SRAM block, and in particular in the middle there are the first six cells of the word line WL_i. We assume that on WL_i the first cell on the left $C_{i,0}$ is affected by a resistive-open defect in the pull-up transistor of one of the two inverters (as Df4 in Fig. 1). This defect may cause a dRDF. This fault is detectable when, immediately after a write data on cell $C_{i,0}$, one or multiple read operations are performed on the same cell. An equivalent faulty behavior can also occur when the write data in cell $C_{i,0}$ is followed by read or write operations on the other cells of the same world line. This is possible because, if for example cell $C_{i,1}$ is selected, the pass transistors Mnt3 and Mnt4 in Fig. 1 of all the cells on the same word line, in particular the faulty cell $C_{i,0}$, are saturated. So, $C_{i,0}$ fights against the pre-charge circuit that is in the on state as for all the non-selected columns. Consequently, the faulty cell $C_{i,0}$ undergoes a stress (RES) similar to a read operation.

In order to give a formal confirmation to the previous assumptions and assertions, electrical simulations have been performed on the Infineon 0.13 μm embedded-SRAM family with the Infineon internal SPICE-like simulator. It has been considered a reference 8 K $\times$ 32 memory, organized as an array of 512 word lines $\times$ 512 bit lines. The cell array of this memory is split in 128 blocks. When a word line is selected all the 512 cells on this word line are connected to respective bit lines. The bit line selection is performed by a pre-decoder, that selects a column for each block (for example the first column of each block), followed by different lines of multiplexers.

In Fig. 5 there is an example of a two-block SRAM with the column decoding made by a pre-decoder and multiplexers. Consequently, when a read operation is done on a cell, it is actually performed on all the corresponding cells for each block, and after, there

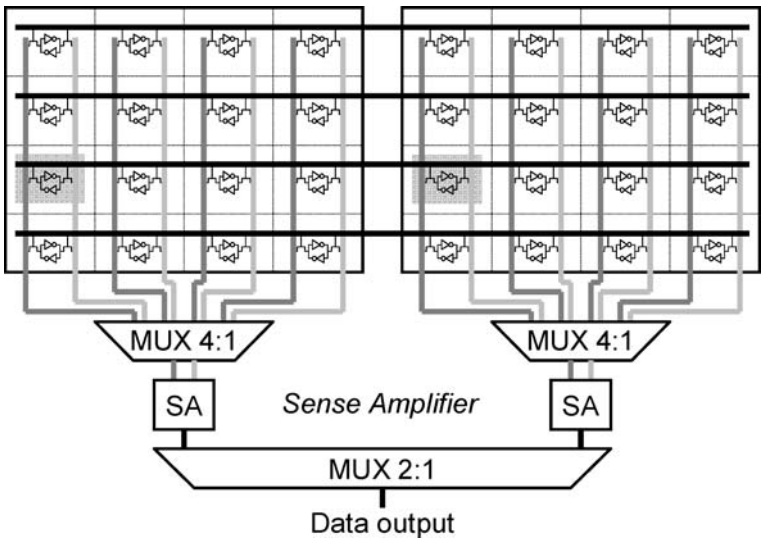

Fig. 5. Scheme of a two-block SRAM memory.

is a further selection made by multiplexers. Thus, in the considered Infineon architecture, when a cell is selected to be read or written, 512 cells are contemporarily selected because they are on the same word line. For 128 of them the pre-charge circuit is off, because they are in the same position of the selected cell in the different blocks. In term of stress, for each read or write operation, there are 128 cells with a actual read stress, because they are selected by word line and bit lines, and 384 ($= 512 - 128$) cells that undergo a RES, because they are selected only by the world line signal.

The simulations have been performed to estimate and confront the stresses produced in the following situations:

1. On the faulty cell one $w0$ operation is performed, immediately followed by one $r0$ operation. This case is denoted (a) in the following waveforms.
2. On the faulty cell one $w0$ operation is done, immediately followed by read (denoted b_1 in the following waveforms) or write (denoted b_2 in the following waveforms) operations on the cells placed on the same word line.
3. On the faulty cell one $w0$ operation is performed, immediately followed by read or write operations on the cells on the same word line, but placed in other blocks in the same position of the faulty cell (highlighted cells in Fig. 5). This case is denoted (c) in the following waveforms.

The waveforms shown in Fig. 6 are the results of the electrical simulations made with the previous conditions in the case of a faulty cell, where the defect Df4 is present and has a size of 1.4 MΩ.

The waveforms in Fig. 6.1 represent the control signals; CLK, RWB which are the read/write selection, the word line and bit line enable signals (WLEN0, WLEN1 and BLEN0). These signals perform the synchronization of the address decoders. The voltage values of S and SB nodes (see core cell presented in Fig. 1) are reported in Fig. 6.2, for the comparison of case a and b (b_1 and b_2) and in Fig. 6.3 for a comparison between cases a, b_1 and c. These waveforms show that after a w0 operation the fault free inverter of the cell has its output (node S) normally switched to '0' logic, that is an effective electrical 0 V. The other inverter has its output switched to '1' logic, that does not correspond to an exact Vdd value, due to the delay effect involved in defect Df4.

In all cases a, b and c, the disturb operations performed immediately after the $w0$ made on the same cell or in other cells of the same word line, produce an abnormal swap of the faulty cell after two cycles. This is a confirmation of the hypothesis done at the beginning of this section, i.e. the effects produced by the read equivalent stress in terms of sensitization of dRDF are very similar to actual read stresses. In fact, in both graphs (Fig. 6.2 and 6.3) the waveforms show different cases of RES (b_1, b_2 and c) which are very similar to a read after write (case a).

Considering Fig. 6.2, it can also be observed that in case of read operation the word line enable signal is on for a period a little bit longer than for the write

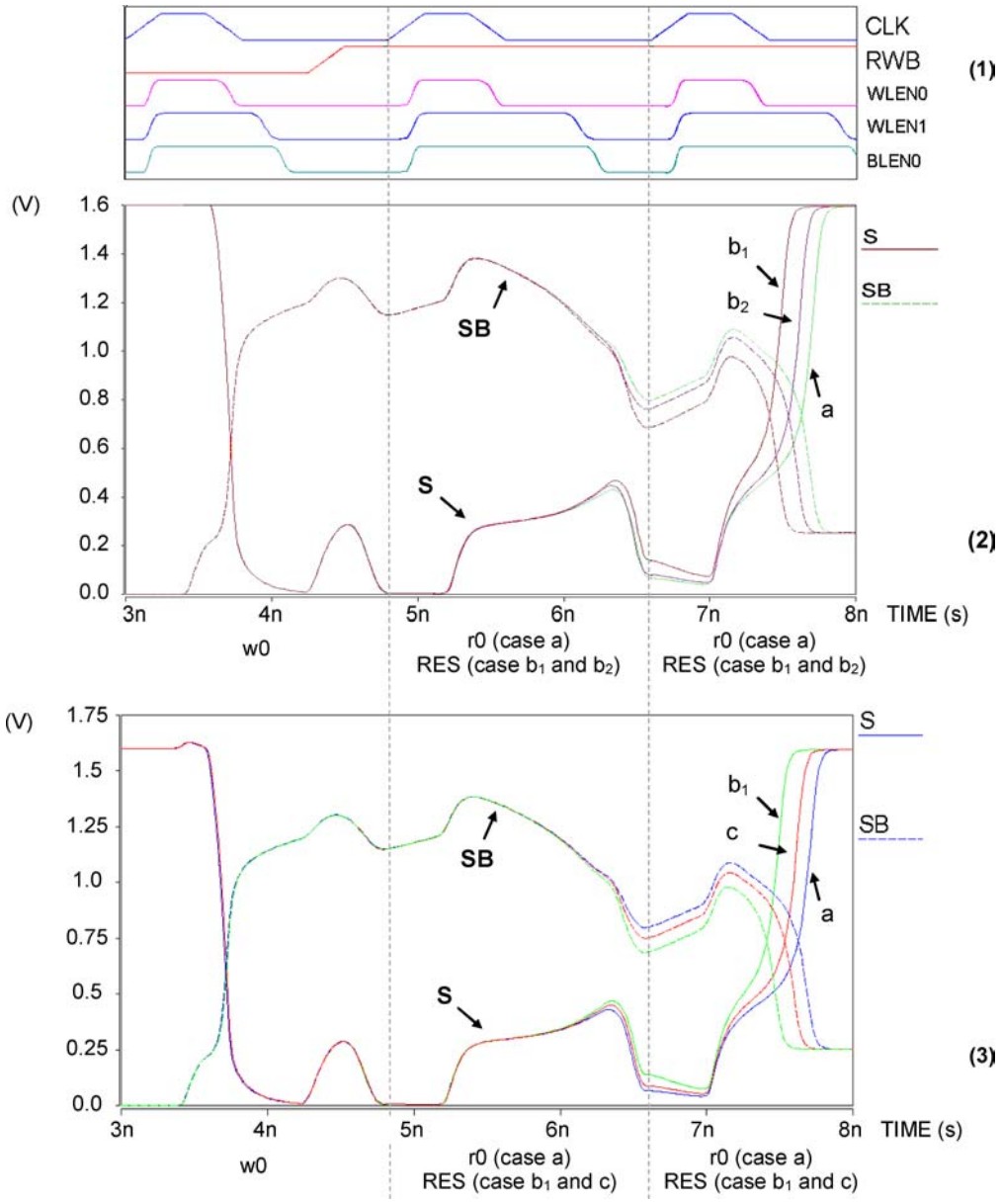

Fig. 6. Electrical simulations of cases *a*, *b* and *c*.

operation. This involves that b_1 produces a more prolonged stress and the cell swaps before.

Now we evaluate the RES in terms of sensitization performance. For this purpose, parametric simulations have been made with different cycle time and with a reasonable resistive range for the size of the resistive-open defect Df4 on the Infineon SRAM memory structure. The results, summarized on the graph of Fig. 7 are referred only to case *b*1. These results are clearly very similar to those, shown in Fig. 3, which refer to the read after write method. The analysis of the two graphs of Fig. 3 and Fig. 7 also confirms that the sensitization effect of the RESs is higher than that produced by read operations on the faulty cell, with the same working condition: typical process, temperature 125°C and supply voltage 1.6 V.

In order to highlight the higher efficiency of RESs for the sensitization of dRDFs, we propose in Table 2

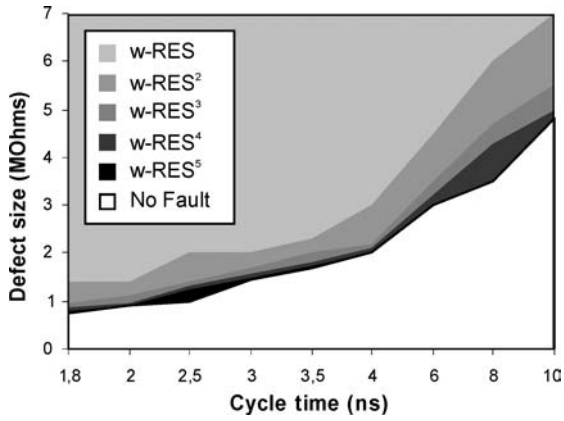

Fig. 7. Fault detection as a function of the cycle time, defect size and RES (typical process, $T = 125°C$, $V = 1.6$ V).

the results of read after write operations and RESs. In this table, the values represent the size of defects that lead to dRDFs. These values are the minimal ones sensitized by read after write operations (w-r^M) or RESs (w-RES^M) for different cycle times. For example, for a cycle time of 4 ns, the sequence w-r^3 sensitizes a dRDF, consequent to a minimal defect size of 2.5 MΩ, while in same conditions, w-RES^3 allows to sensitize dRDF involved by a 2.1 MΩ defect. In other words, RESs are more effective than actual read operations because they can sensitize dRDFs due to smaller resistive defects.

4. March Test Solutions for dRDF Testing

In this section we use the results presented above in order to produce an efficient March test procedure for dRDF detection. A March test has to have some requirements to be able to test dRDFs. In the following we set these requirements that can be also applied for whatever test procedure.

Table 2. Comparison between read after write and RES.

Cycle time (ns)	1.8	2	2.5	3	3.5	4	6	8	10
	Minimal resistance size, Mohm								
w-r	1.7	2	2	3	3.5	4	5.5	8	9.5
w-RES	1.4	1.4	2	2	2.3	3	4.5	6	7
w-r^2	1.2	1.2	1.7	2	2.5	3	4	6	7
w-RES^2	0.95	1.1	1.4	1.7	2	2.2	3.5	4.7	5.5
w-r^3	0.95	1.1	1.4	1.7	2	2.5	3.5	5	6
w-RES^3	0.85	0.95	1.3	1.55	1.8	2.1	3.2	4.3	5
w-r^4	0.9	1	1.3	1.55	1.9	2.2	3.3	4.4	5.5
w-RES^4	0.8	0.9	1.22	1.5	1.75	2	3	3.5	4.8
w-r^5	0.85	1	1.25	1.5	1.9	2.2	3.3	4.3	5.5
w-RES^5	0.8	0.9	1.22	1.5	1.75	2	3	3.5	4.8

i. It is necessary that the read/write operations are performed with a particular addressing order with the purpose to execute the March elements on the memory array by acting on word line after word line. This is necessary because the RESs are produced only by operating on the cells of the same word line. For example, let us consider again the Infineon 0.13μm embedded-SRAM architecture. The read and write operations of the March elements have to be operated firstly on all the 512 cells of the first word line, then on the 512 cells of the second word line, and so on.

The address sequence word line after word line can be operated by exploiting the first of the six Degrees of Freedom (DOF) of March tests [9]:

DOF I: Any arbitrary address sequence can be defined as an $\Uparrow$ sequence, as long as all addresses occur exactly once ($\Downarrow$ is the reverse of $\Uparrow$). The fault detection properties are independent of the utilized address sequence.

ii. The elements of our March test have to include w0 operations, necessary for sensitization, and r0 necessary for observation.
iii. Additional elements with $w1$ and $r1$ are needed in order to detect similar faults generated by resistive-open defects placed symmetrically in reference to Df4 (see Fig. 1).
iv. All the elements, in particular the sensitization ones, need to be performed in $\Uparrow$ and $\Downarrow$ sequence.

The last statement is based on some considerations. For example we still use the same Infineon SRAM architecture. If the faulty cell is C_{i0}, the first cell of the ith word line, an element like $\Uparrow\ w0$ operates a w0 on this cell and is immediately followed by w0 operations performed on the following 511 cells of the same word line. These $w0$ operations imply 511 RESs on the faulty cell. If the faulty cell is the second one, C_{i1}, the same March element $\Uparrow\ w0$ involves 510 RESs on the faulty cell. In case the defective cell is the last of its word line the element $\Uparrow\ w0$ does not involve any RES on it. The introduction of $\Downarrow$ elements allows that the sensitization phase is performed with the opposite addressing sense

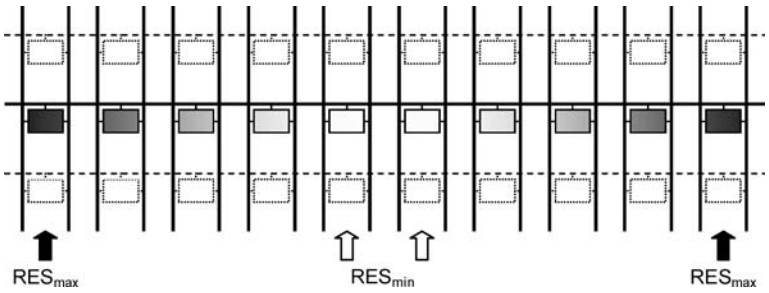

Fig. 8. Distribution of RESs on a word line with the modified March C-.

of the word line. In these conditions the cells that endure the maximum number of RESs are those placed in the extremes of the word line, while those placed in the middle of the word line undergo the smallest number of RESs, i.e. 512/2 = 256 of RESs. In general if *nb_cell* is the number of cells of each word line and *nb_op* the number of operations (read/write) of the March element ($\Uparrow w0 \rightarrow nb\_op = 1; \Uparrow r1w0 \rightarrow nb\_op = 2$), the maximum number of RESs that a cell undergoes is:

$$RES_{\max} = (nb\_cell - 1) \times nb\_op$$

and the minimum one is:

$$RES_{\min} = (nb\_cell \times nb\_op)/2$$

This is illustrated in Fig. 8, where the color of cells is darker if they endure a higher number of RESs.

Among the existing March tests, March C- respects already three (ii, iii and iv) of the four requirements exposed above. This is a 10 N linear test, which is effective to detect stuck-at, transition and 2-coupling faults and that normally cover 0% of dRDFs [6]. March C- has the structure shown in Fig. 9.

We propose a modification of March C- with the objective to detect dRDFs. We can observe that the first five elements (M_0 up to M_4) could be effective for dRDF sensitization because they contain the $w0$ or $w1$ operation. In these elements the read operations are useful for the observation, but they also contribute to the sensitization. Both $\Uparrow$ and $\Downarrow$ sequences are operated allowing a good distribution of RESs for all the cells. The simple modification, which makes March C- able to detect dRDFs, consists in the use of the particular address sequence word line after word line (requirement i). Thus, the modified March C- has the same structure as the original March C- presented in Fig. 9.

$$\left\{ \Updownarrow(w0)\ \ \Uparrow(r0,w1)\ \ \Uparrow(r1,w0)\ \ \Downarrow(r0,w1)\ \ \Downarrow(r1,w0)\ \ \Updownarrow(r0) \right\}$$
$$M_0 \quad M_1 \quad M_2 \quad M_3 \quad M_4 \quad M_5$$

Fig. 9. March C- structure.

Now we evaluate the modified March C- in reference to the Infineon SRAM structure. If the faulty cell is C_{i0}, the first cell of the word line i, the element M_2 operates a $w0$ on this cell followed by the sequence $r1w0$ performed on the following 511 cells of the same word line. This means $2 \times 511 = 1022$ RESs on the faulty cell. The same happens if the faulty cell is C_{i511}, the last cell of word line i, and the element M_4, that is M_2 with inversed address order, operates a $w0$ and 1022 RESs on C_{i511}. So, C_{i0} and C_{i511} endure the maximum number of RESs because they placed in the extremes of the word line. Those placed in the middle of the word line are the less stressed with $2 \times (512/2) = 512$ RESs. Moreover, the elements M_1, as its homologue M_3, allows the test of similar faults due to resistive-open defects symmetrically placed in reference to Df4.

It is important to note that the complexity of the proposed March solution is 10 N and it is invariable. The modified March C- capability to produce RESs, useful for the dRDF sensitization, changes with the SRAM architecture under test but in any case it is always very high. In the mentioned case, the modified March C- allows a minimum of 512 RESs in sequence, while in the same conditions, a RAW test should include a very large number of read operations increasing dramatically its complexity (more than 1000 N). The proposed test presents another advantage: due to the first of the six degrees of freedom [9] of March tests, the modification that we have proposed does not change the capability of March C- to detect the former target faults.

5. Conclusions

The present study has focused on dynamic faults that may occur in core-cells of SRAM memories, in particular on dynamic Read Destructive Faults. In presence of certain resistive-open defects in the refreshing loop of SRAM core-cell, multiple read operations may cause the faulty swap of the cell. In case of low resistive value, the complexity of read after write algorithm may increase dramatically. In order to produce more efficient test solutions, we have explored a different way to sensitize dRDF.

In this direction, we have shown that a cell undergoes a stress equivalent to a read operation, when a read/write operation is performed on a cell of the same word line. We have called this phenomenon Read Equivalent Stress (RES) and we have shown that RESs are more efficient than read after write for the sensitization of dRDFs. On these bases, we have modified the March C- to make it able to detect efficiently dRDFs, without changing its former complexity and capabilities.

The proposed March test solution presents many advantages as its linear complexity and the reutilization of an already existing March test. The main benefit is the high efficiency to detect dRDFs in comparison with read after write test. In fact, in order to reach the same effectiveness, a RAW test should have a prohibitive complexity.

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