Data Retention Fault in SRAM Memories: Analysis and Detection Procedures

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Abstract

In this paper, we present a novel study on Data Retention Faults (DRFs) in SRAM memories. We analyze in detail the electrical origins of these faults, starting from the most common till those that lead to what we have called ***hard to detect*** *DRFs. In general, DRFs are supposed to be produced by very high resistive-open defects that affect the refreshment loop of the core-cell. We demonstrate that lower values of resistance may produce hard to detect DRFs. Moreover, each resistive-open defect produces a particular faulty behavior of the core-cell that changes for different ranges of the resistive value. We analyze different cases and we propose for each one an efficient test procedure based on March tests. In particular, we propose to stimulate the defective cells in some cases by indirect accesses and in some other cases by emphasizing natural noise phenomenon of SRAM memories (such as the ground bounce).*

1. Introduction

In modern integrated circuits such as System-on-Chip (SoC) the importance of memories is growing. Actually, the ITRS roadmap [1] forecast that in 2013 over 90% of the SoC area will be taken by memories, in particular embedded-SRAMs. The SRAMs are more and more dense, and their capacity grows at the same time. Consequently, these devices are more prone to faults and testing them efficiently becomes very important for the yield of SoCs.

The functional fault models traditionally employed in SRAM testing are nowadays insufficient to test the effects produced by some defects that may occur in VDSM technologies. Improvements in manufacturing process quality and memory architecture have lead to the development of new fault models, which are tightly linked to the internal memory structure. These faults need specific test solutions. Moreover, the presence of resistive-open defects is becoming more and more important, due to the ever-growing number of interconnections between the layers. In particular, it is reported in [Need98] that open/resistive vias are the most common root cause of test escapes in deep-submicron technologies.

Several studies on the influence of resistive-open defects on the correct operation of SRAM core-cells have been published recently [2,3,4]. In this paper, we consider resistive-open defects that, occurring in the refreshment loop, may cause data retention faults (DRFs). The proposed analyses concern the different forms of DRF in correlation with the location of the defect and its resistive value.

The rest of the paper is organized as follows. In Section 2, we describe in detail the state of the art of the electrical origins and the test solutions for the DRF. In Section 3, we expose the analyses of *the hard to detect* DRFs and we propose algorithmic procedures useful for their test. In particular we identify two sub-cases of *hard*

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to detect DRFs and we propose to produce their sensitization by stimulating the defective cells by indirect accesses and by emphasizing a natural noise phenomenon of SRAM memories such as the ground bounce. Conclusions and perspectives are given in Section 4.

2. Data Retention Faults: the state of the art

The definition of Data Retention Fault (DRF) is the following:

> *A DRF occurs when a memory cell loses its previously stored logic value after a certain period of time during which it has not been accessed* [5].

In general this kind of fault is the consequence of resistive-open defects in SRAM core-cells, in particular in the self-refreshment loop circuit. Figure 1 depicts the scheme of a standard six transistors core cell in which we have inserted three resistive-open defects in locations where they are commonly the cause of DRFs [5, 6]. These defects are denoted as Df1, Df2 and Df3.

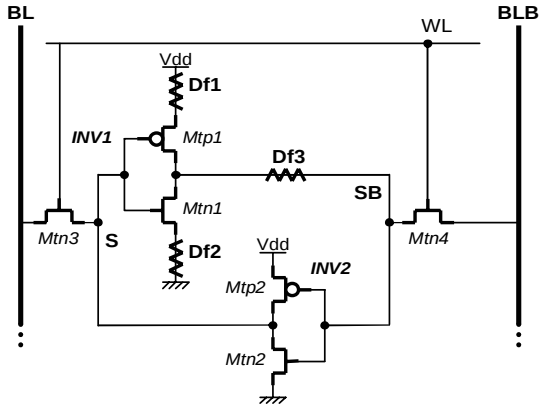

Figure 1: Resistive-open defects injected into the memory core-cell as cause of DRFs.

In order to explain the mechanism of DRFs we consider a core-cell with a resistive-open defect in the pull-up of the inverter INV1; this defect corresponds to Df1 that restrains the current flow between Vdd and node SB. In [2] we have demonstrated that this defect may cause Read Destructive Faults (RDFs), or dynamic Read Destructive Faults (dRDFs), in certain range of resistive value. When Df1 has a very high resistive value, larger than 100 MΩ, it behaves like a quite pure open circuit and involves DRFs.

When a '0' is stored in the cell, bit line BL discharges node S to '0', while BLB charges node SB to '1'. At the end of the w0 operation the two pass-transistor Mtn3 and Mtn4 are off and the cell is isolated from the bit lines. At this moment node S is active low due to the pull-down of the inverter INV2 (see Figure 1), while node SB is floating high, because the pull-up of INV2 does not work correctly due to defect Df1. In this conditions, if the natural leakage currents that discharge node SB (especially through Mtn1 and Mtn4) are higher than the current that passes through the faulty pull-up of INV1 the voltage value of node SB slowly decreases from Vdd to Vdd/2. When node SB is under the threshold value of Vdd/2, INV2 switches, immediately followed by the switch of INV1, so that a faulty swap of the cell occurs with the loss of the stored information.

We have simulated this phenomenon on the Infineon 0.13 µm embedded SRAM, in particular on a cell in which we have inserted the resistive-open defect Df1 with the following parameters:

- Process: *fast*
- Supply voltage: *1.6 V*
- Temperature: *120°C*
- Resistive-open defect: Df1 = 100 MΩ

The evolution of the phenomenon of DRF, described above, is clearly reproduced on the waveforms in Figure 2.

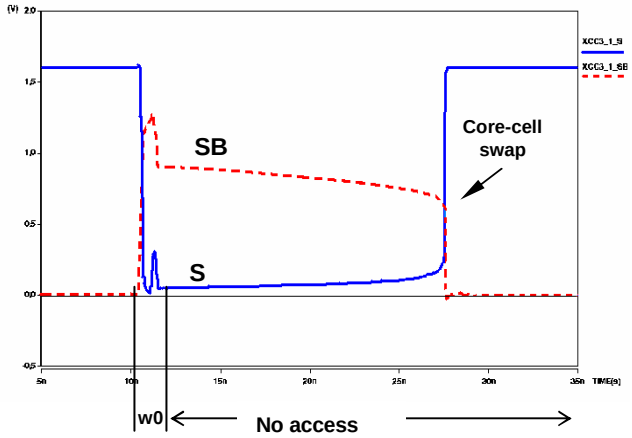

Figure 2: Data retention fault caused by high resistive defect Df1

We can observe that just after the w0 operation node S is at '0', while node SB is at '1', but with a level lower than Vdd due to the faulty pull-up of INV1. For the same reason node SB slowly loses the stored charge because of the leakage currents. With the decrease of the voltage of node SB also INV2 begins to work not perfectly, in particular Mtn2 conducts less than normal and Mtp2 starts to conduct. Consequently the voltage of node S grows slowly. When node SB reaches the threshold of Vdd/2, INV2 switches and the cell swaps.

In this experiment, the resistive value of defect Df1 (100 MΩ) is enough to produce a DRF. Generally the value of Df1 has to be much higher. Here, the particular experimental conditions (temperature 125°C and the fast process corner) maximize the faulty behaviour, producing DRFs.

In order to detect this kind of fault some algorithms have been proposed. In particular in [5, pp.279-283] we find two solutions, named IFA-9 and IFA-13, which are shown in Figure 3.

$$\{\Uparrow(w0);\Uparrow(r0;w1);\ \Uparrow(r1;w0);\Downarrow(r0;w1);$$
$$\Downarrow(r1;w0);\mathrm{Del};\Uparrow(r0;w1);\mathrm{Del};\Uparrow(r1)\}$$

IFA-9

$$\{\Uparrow(w0);\Uparrow(r0;w1,r1);\ \Uparrow(r1;w0,r0);\Downarrow(r0;w1,r1);\Downarrow(r1;w0,r0);$$
$$\mathrm{Del};\Uparrow(r0;w1);\mathrm{Del};\Uparrow(r1)\}$$

IFA-13

Figure 3: IFA-9 and IFA-13 test procedure

These two algorithms are able to cover many fault models such as stuck at faults, unlinked coupling faults, transition faults and others. Their capability to cover DRFs is the consequence of the fact that they have a delay 'Del' inserted after an element that leaves '0' stored in all the cells and also after an element that leaves '1' stored in all the cells (for symmetrically placed resistive-open defect). The duration of the delay is strictly related to the architecture of the memory and the employed technology. It can be in the order of some 100 ns up to 10 ms.

Another way to cover this kind of DRFs can be done indirectly. In fact, the same high resistive-open defects that are the cause of DRFs are also the source of Read Destructive Faults (RDFs), or Deceptive Read Destructive Faults (DRDFs) [7]. For this reason, for the detection of DRFs we can use the read after write algorithm (March RAW [8]) that does not need the use of delays. In practice, just after a write operation, for example w0, a read operation is acted, as r0. After the w0, in presence of defect Df1, the information is stored correctly, but while node S is active low, node SB is floating at '1'. The following read operation connects the two nodes, S and SB, to the two bit lines charged at Vdd. Consequently node S undergoes an external pull-up that, by partially activating transistor Mtn1, that discharge node SB, causing the swap of the cell.

3. Hard to detect DRFs

In the case the current that pass through the resistive-open defects is larger than the leakage currents, *i.e.* in presence of smaller resistive-values, DRFs may still appear, but the behavior of the faulty cell is more complex. In these circumstances the DRFs are ***hard to detect.*** This case is discussed in detail in the next two sub-sections. In sub-section 3.1 we study the case of defect Df1 that does not behave like a quite pure open circuit, *i.e.* for Df1 < 100 MΩ. In sub-section 3.2 we study the case of defects Df2 and Df3 that are far from the condition of pure open circuits, *i.e.* for resistive values close to some kΩ.

3.1 DRF caused by low resistive defect Df1

When an SRAM core cell is affected by defect Df1 for resistive values lower than 100 MΩ, it can show a faulty behavior corresponding to a DRF. In this case the sensitization of such DRF is very different from what we have exposed in the previous section.

As example let us consider an Infineon 0.13 µm SRAM core-cell affected by the resistive-open defect Df1 with a resistance lower than 100 MΩ. After a w0 operation the data is stored in the cell correctly, node S at '0' and node SB at '1'. If no operation is performed on the cell, it continues to remain stable along the time because in this case the leakage currents of node SB are too weak in comparison with the current provided by the pull-up of INV1, even in presence of defect Df1. However, the cell can present also in this case a DRF. In fact, even if no operation is performed directly on the cell, it can undergo an external stimulation. Actually, when a cell is accessed for a read/write operation, the word line signal actives the pass-transistors of all the cells belonging to the word line. While the operation is done on a selected cell, all the other cells of the same word line are connected with their bit lines charged at Vdd by a precharge circuit. The stimulation on the non-selected cells is very similar to the stimulus produced by an actual read operation and we call it Read Equivalent Stress (RES), [3]. Normally the RES is not destructive, but, applied on a cell affected by Df1, it produces a degradation of the stored value. In fact, node SB of the defective cell loses its charge and its voltage drops. Figure 4 shows the waveforms of a concrete example of what exposed above, with a cell where we have inserted Df1 with the following parameters:

- Process: *normal*
- Supply voltage: *1.6 V*
- Temperature: *27°C*
- Resistive-open defect: Df1 = 15 MΩ

This value of resistance may appear large, but is very little in comparison to the values that involve classical DRFs with this process corner condition and temperature.

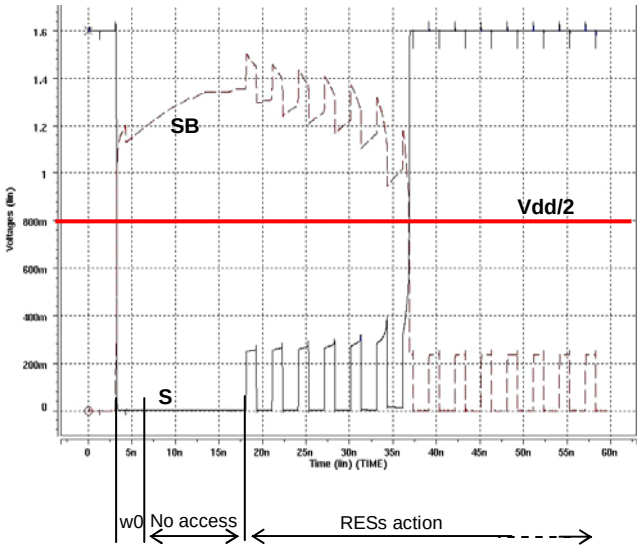

Figure 4: DRF caused by low resistive Df1

The waveforms of Figure 4 show that after a w0, the logic value is correctly stored in the cell: node S is at '0' and node SB is at '1'. However, we can also observe that, due to the faulty pull-up of INV1, node SB has not reached perfectly the Vdd. This voltage level is reached during the following four clock cycles, in which the cell is accessed neither directly with read/write operations nor indirectly by RESs. At this time, the voltage levels of S and SB have not undergone the effect of leakage currents as in the case of large resistive value of Df1 (as shown in section 2). After this no-operation period, the defective cell has been stimulated indirectly by RESs, *i.e.* by acting read/write operations on other cells placed on the same word line. The consecutive RESs produce the progressive degradation of the voltage of node SB. This node, after seven RESs, reaches the threshold of Vdd/2 and the cell swaps. Consequently, the cell presents a DRF because with the normal use of the memory, it loses its stored value, even if there has been no access to the cell, with read/write operations.

The algorithms proposed in the previous section (Figure 3) are valid in case of high resistive value of Df1. In the case of lower resistive value, they are not sufficient because the delays, which were useful for the sensitization, conversely contribute to stabilize the cell. This fact can observed on Figure 4, where in the '*no access*' region the voltage level of node SB grows to reach Vdd.

In order to detect this kind of DRF, it is useful to produce the highest number of consecutive RESs. In fact a sequence of consecutive RESs produces a good sensitization of the fault by degrading progressively the voltage of one of two cell nodes. An easy way to produce long sequence of RESs is the application of a common March test with the particular addressing order "word line after word line". For example, let us consider an Infineon 0.13 µm 8kx32 embedded-SRAM memory, organized as an array of 512 word lines x 512 bit lines. The read and write operations of the March elements have to be operated firstly on all the 512 cells of the first word line, then on the 512 cells of the second word line, and so on.

The modified March C-, which we have proposed in [3], can be used to produce long sequences of RESs. This algorithm is the well-known March C-, see Figure 5, that has to be applied word line after word line. This particular application guarantees a large number of consecutive RESs that is useful to detect DRFs, but it is also useful to sensitize dynamic Read Destructive Faults (dRDFs), [3].

$$\left\{ \Updownarrow (w0)\ \ \Uparrow (r0, w1)\ \ \Uparrow (r1, w0)\ \ \Downarrow (r0, w1)\ \ \Downarrow (r1, w0)\ \ \Updownarrow (r0) \right\}$$
$$M_0 \qquad M_1 \qquad M_2 \qquad M_3 \qquad M_4 \qquad M_5$$

Figure 5: March C- structure

3.2 DRF caused by low resistive defects Df2 and Df3

In certain conditions the solution that we have exposed in the previous sub-section may not be sufficient to detect certain DRFs. In particular we can observe a peculiar behavior of the defective cell in some ranges of resistive value of defects Df2 and Df3.

- **Df2** < 5.3 kΩ
- **Df3** < 11.8 kΩ

In order to explain this case, as done before, we use a concrete example: the simulation of an Infineon 0.13 µm core-cell, in which we have inserted the resistive-open defect Df3 with the following parameters:

- Process: *normal*
- Supply voltage: *1.6 V*
- Temperature: *27°C*
- Resistive-open defect: Df3 = 11.7 kΩ

We can observe the results of the simulation in Figure 6. During this simulation we have operated on the defective cell stimuli similar to those of sub-section 3.1. At first we have performed a w1 operation that is acted correctly: node S is a '1' (Vdd), and node SB is at '0' (GND). A period of four cycles follows, and there is no degradation of the voltage level of the two cell nodes (no access region in Figure 6). In the following clock cycles the cell undergoes the stress of RESs in sequence, *i.e.* as said before the stress of the precharge circuit on the cell due to the normal action of read/write operations on other cells of the same word line. In the previous example this stress was sufficient to produce the progressive

degradation of SB voltage level and, after a certain number of RESs, the swap of the cell. In this case during the action of the RESs on the cell there is only a temporary approach of nodes S and SB voltages to the threshold voltage Vdd/2. This phenomenon appears at each cycle, but there is not an actual faulty swap of the cell, whatever the number of RESs in the sequence. The same considerations and analysis are valid not only for defect Df3 but also for defect Df2.

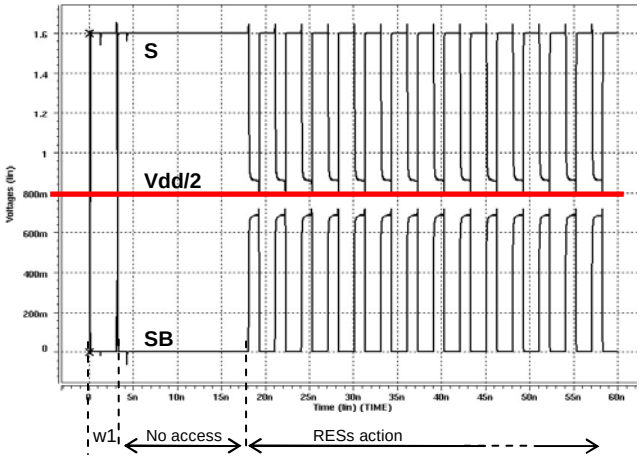

Figure 6: Cell instability that may produce data retention faults. Df3 = 11.7kΩ

Despite the fact that the cell does not swap in our experiment, the detection of defects Df2 and Df3 is important for two reasons. The voltage level reached by node S and node SB are very close to the commutation threshold: about 10 mV in the example of Figure 6. An SRAM memory is expected to retain data for a long time, sometimes for years [5], and a cell that presents the behavior shown in Figure 6 is very weak during the common operations that involve the action of the RESs. If this weakness is coupled with noise phenomena, like the ground bounce, the cell that may have passed the common tests for DRF, can swap losing its logic state during the normal operation of the memory. Moreover, even if during the RESs action the voltage levels of node S and SB are not enough close to the Vdd/2 threshold to induce the swap, the device may incur a premature aging. In fact, the presence of a resistive-open defect may induce a local increment of the heat due to the Joule effect and consequently it leads to an increase of the temperature. In this condition the phenomenon of electromigration takes place, and the resistive-open defect grows till to produce the malfunction of the cell. The cycle of the acceleration of the electromigration is shown in Figure 7.

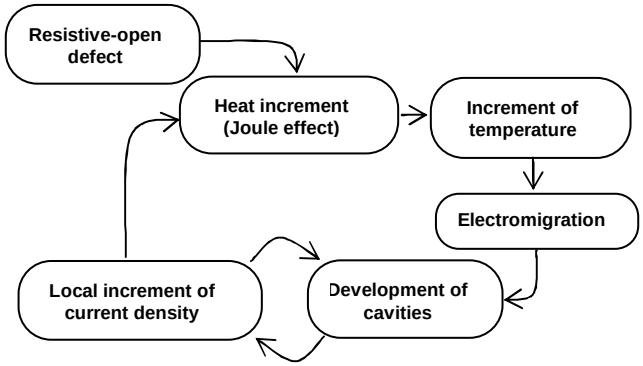

Figure 7: The acceleration electromigration cycle

In order to detect the presence of defects Df2 and Df3, an algorithm has to have the following requirements:

i. Maximizing the productions of RESs in sequence
ii. Maximize at same time the noise conditions.

The first requirement is satisfied by the solution that we have given in sub-section 3.1: the application of a common March tests with the particular addressing order ‘word line after word line’. For the second requirement, we can introduce a dedicated source of noise during the application of the algorithm. Another way is the application of the algorithm in conditions that cause the natural source of noise in SRAM memories.

Among the possible noise sources in SRAM memories there is the ground bounce [9, 10]. The ground bounce is caused by large instant current, due to the switching of multiple devices, through parasitic inductance at the ground node. Ground bounce is especially a serious problem in semiconductor memories because of the simultaneous switching of a large number of memory cells and sense amplifiers. In presence of ground bounce, the commutation threshold of the core-cell inverters may more easily be passed in presence of defects Df2 and Df3 than in normal condition. In fact the voltage of the storage node at ‘0’ (node SB) can shift of some 100 mV [10], due to ground bounce. Consequently, defective cells, which have not faulty behavior in normal conditions, may swap in presence of ground bounce.

As mentioned above, the ground bounce appears when there is a multiple device switching. In memories the devices that may switch are the core-cells, the output circuits and the addressing circuits, especially those used for the column addressing that commonly employ some levels of multiplexers. After these considerations we can formulate an algorithmic procedure that highly increases the detection of the presence of defects Df2 and Df3. As done for the case studied in sub-section 3.1, we can still use a March test with the addressing order ‘word line after word line’ for the production of RESs in sequence.

But in order to maximize the ground bounce phenomenon, the March test has to have also the following requirements:

a. The part of the address concerning the bit line selection has to present the highest possible Hamming distance between each couple of addresses. In other words, this part of the address has to produce the highest possible number of bit commutations. For example, on an 8 bit column address the change between the two addresses 01001110→10110001 leads to 8 commutations, the maximal possible.

b. The stored logic value has to change for each write operation, and so for each read operation. This requirement is allowed by the fourth of the six Degree of Freedom of March tests [11].

In bit-oriented memories it is easier to operate a large number of switching on the column addressing circuits. In the case of a word-oriented SRAM memory we can maximize the ground bounce phenomenon especially by provoking the switching of all the output bits.

As final remarks we can say that the solution proposed in this section does not assure 100% coverage, because many factors, as the value of the resistive-open defect, are concerned. The proposed solution assures the conditions that maximize the testability.

4. Conclusions and perspectives

In this paper we have presented a detailed analysis of data retention faults, with a complete study on the electrical phenomena that cause the fault. At the base of DRFs there is the presence of resistive-open defects in the refreshment loop of the core-cell. We have identified three possible locations for these defects. For each defect, different ranges of resistive value produce different effects on the cell. Consequently, the DRFs that appear need specific conditions for their sensitization. In particular, we have described in detail what we have called *hard to detect* DRFs. We have found two different situations that may cause DRFs. We have proposed for both of them an efficient test procedure. In particular we have proposed to stimulate the defective cells by indirect accesses and by applying the test algorithms so as to emphasizing the natural phenomenon of ground bounce.

We intend to continue the study of the fault model connected to the presence of resistive-open defects in SRAM memories. Moreover we want also continue to investigate the conditions that maximize the fault detection in presence of noise phenomena.

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