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Temperature Dependency in UDSM Process

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Abstract. In low power UDSM process the use of reduced supply voltage with high threshold voltages may reverse the temperature dependence of designs. In this paper we propose a model to define the true worst Process, Voltage and Temperature conditions to be used to verify a design. This model will provide an accurate worst case definition for high performance designs where standard design margins are not applicable. This model is validated at either cell level or path level on two different 130nm process.

I Introduction

With the scaling of technologies, the leakage current contribution to the power consumption has dramatically increased. One solution to reduce the static to dynamic power ratio is to use higher threshold voltage (V_T) devices. However due to the opposite temperature sensitivities of the mobility and the threshold voltage, the current delivered by the devices exhibits, for such biasing conditions, a complex behavior with temperature [1, 2] that may completely modify the temperature at which a design reaches its critical corner. This temperature effect, called temperature inversion phenomenon, becomes particularly critical when the threshold voltage value approaches half V_{DD}. Unfortunately this configuration may occur in some variants of low power UDSM processes (130nm and 90nm), in particular for high V_T process options.

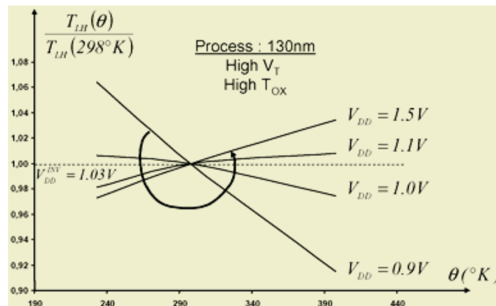

Fig. 1. Temperature evolution of the simulated inverter delay for different V_{DD} values

To validate most digital synchronous designs, it is usually sufficient to verify the design behavior for the worst and the best case timing conditions. In actual low power design, due to the combined use of high threshold voltage devices and reduced supply voltages, the worst case timing conditions becomes less predictable and can occur at different temperatures. In the majority of cases this effect is accounted for through design margins however for high performance designs where more accurate timing

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validation is required, it may be necessary to perform validations in more than 2 PVT conditions in order to guarantee the correct behavior of the design.

Even if the sensitivity of design performances to V_{DD} and V_T values has already been identified as one of the major limitations in V_{DD} scaling [11], little attention has been given to characterize their temperature sensitivity in the low voltage domain. To illustrate the problem we give in Fig.1 the evolution of the normalized propagation delay of a simple inverter. As shown, for high values of the V_{DD} the critical case appears, at high temperature, while for low V_{DD} values the temperature sensitivity is completely reversed. For this reason, this temperature effect is often called the temperature inversion phenomenon.

The main contribution of this paper is to propose a representation of the timing performance of a CMOS structure [4] that facilitates in finding the true worst case condition during the STA. It is organized as follows. In section II, we characterize the transistor current temperature inversion phenomenon. Section III introduces the analytical model from which the timing performance representation is deduced. In section IV we apply these models to characterize the temperature sensitivity of the process, the cell and a data path of a circuit in two different 130nm technologies to demonstrate the influence of the process conditions to the temperature inversion phenomenon. Section IV concludes this work.

II Temperature Inversion: Process Characterization

The threshold voltage and the carrier mobility values are temperature dependent [1, 2]. If both threshold voltage and carrier mobility values monotonically decrease when the temperature increases, the resulting impact on the gate switching current and thus on its timing performance depends on the considered range of V_{DD} values. To analyze this impact let us consider the Sakurai's drain source current (I_{DS}) representation [6]:

$$I_{N,P}^{Fast} = K_{N,P} \cdot W_{N,P} \cdot \left(V_{DD} - V_{TN,P}\right)^{\alpha_{N/P}} \tag{1}$$

where $K_{N/P}$ is a conduction coefficient, and α the velocity saturation index. From (1), it is obvious that a decrease of the $V_{TN/P}$ values results in an increase of the saturation transistor currents while a decrease of the carrier mobility induces an opposite variation of the timing performances. As a result the temperature coefficient of the transistor current and the associated performance parameters may exhibit supply voltage and temperature dependent behaviours. As an example, it has been experimentally observed [8] that for a specific range of V_{DD} value the temperature coefficient of the transition time becomes V_{DD} dependent and may have negative values for $V_{DD}<2 \cdot V_T$. This is a direct illustration of the temperature inversion phenomenon that could appear in nowadays processes with high V_T values and either regular or reduced V_{DD} values.

To characterize the temperature inversion phenomenon, we analyzed the I_{DS} temperature sensitivity of a transistor designed with two 130nm processes A and B, differing one from the other by their threshold value. More precisely, we extracted from eldo simulations, the evolution with temperature of the maximum drain source courant ($V_{GS}=V_{DD}$) delivered by NMOS transistors for different values of V_{DD}. As Fig.2

reports the obtained I_{DS} evolution of an NMOS transistor designed with the process B for three different temperature values.

As shown, for the process B the I_{DS} evolution is non monotonic. Indeed considering the crossing point of the three I_{DS} curves (V_{DD}=V_{GS}=1.08V), it is possible to distinguish two different V_{DD} domains. In the domain I, the NMOS current has a greater value at low temperature. In the domain II, the situation is reversed, the current value is smaller at 233°K. This gives evidence that depending on the V_{DD} value the worst case configuration can be obtained for a completely different temperature value. We can thus conclude that the temperature coefficient of the I_{DS} current is V_{DD} dependent and is equal to zero for the crossing point value V_{DD}=1.05V.

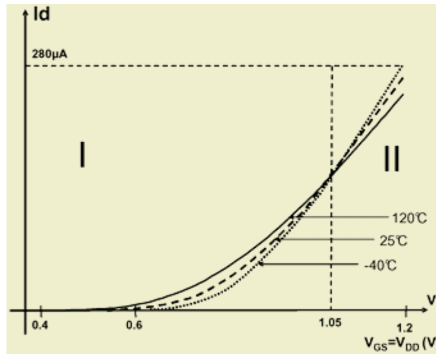

Fig. 2. Temperature evolution of the NMOS transistor current for the Process B

As discussed in [1,2] the evolution of the worst case PVT condition from high to low temperatures can be justified considering the relative variation of the V_{TN} and K_N values with temperature. Although V_T and K have both a negative temperature coefficient, depending on the supply voltage value they have opposite influence on the timing performance. At high V_{DD} value, the temperature induced variations of V_T are small with respect to V_{DD}. As a consequence the temperature induced variations of I_{DS} are mainly due to the K term. At the contrary, at low V_{DD} value, the relative variation of V_T, with respect to V_{DD}, becomes significant enough to counterbalance and even reverse the temperature sensitivity of the I_{DS} courant. In others words, at high V_{DD} values the K term dominates while for lower V_{DD} values the variation of the V_{DD}-V_T term becomes preponderant, reversing the I_{DS} temperature sensitivity.

Table 1. Inversion voltage and nominal threshold voltages for A and B processes

	Process A		Process B	
	NMOS	**PMOS**	**NMOS**	**PMOS**
Inversion point	0.92 V	1.08 V	1.05 V	1.38 V
Vtnom.	0.56 V	0.47 V	0.64 V	0.56 V

One interesting point is that at a V_{DD} value equal to the crossing point value the effect of the V_T variation on the current is exactly balanced by the effect of the K one. Thus imposing this operating point may results in quasi temperature insensitive circuit. Therefore the inversion voltage value of N and P transistors are key metrics to characterize the temperature sensitivity of a design, or to predict unexpected tempera-

ture inversion. Table 1 gives the inversion voltage values extracted from the simulations of the transistor current sensitivity for both A and B processes.

Considering the V_{DD} corners (1.08V and 1.32V) of these processes, we can deduce for the process A that both N and P transistors are never subject to temperature inversion, but for the process B, if the NMOS device is not subject to T inversion, the PMOS is always in inversion. To characterize a process with respect to the temperature inversion phenomenon, two coefficients have to be considered δ and Xk [9, 10] that give respectively the sensitivities of V_T and K to the temperature

$$Vt = Vtnom - \delta \cdot (\theta - \theta nom) \qquad K = Knom \cdot \left(\theta_{nom} / \theta \right)^{Xk} \tag{2}$$

where the nominal values are defined at 298°K and 1.20V. Including these parameters into the current expression (1), we define a derating coefficient Der_I(V_{DD},θ) which allows estimating the performances of any cell operating at any PVT condition.

$$Der_I(V_{DD},\theta) = \frac{I(V_{DD},\theta)}{I_{nom}(V_{DD}^{nom},\theta_{nom})} = \left(\frac{\theta_{nom}}{\theta} \right)^{Xk} \cdot \left(\frac{V_{DD} - V_{Tnom} + \delta \cdot (\theta - \theta_{nom})}{V_{DD}^{nom} - V_{Tnom}} \right)^{\alpha} \tag{3}$$

This coefficient will be used later in an analytical model of timing performances to characterize the temperature sensitivity of CMOS structures.

III Physical Timing Model

It has been shown in [4, 5] that the delay performance of CMOS circuits can be modeled with an analytical representation of the cell output transition time with an explicit identification of the design and process parameters. We summarize in this part the main points of this model considering only the case of falling output edges.

A. Transition Time Modeling

Considering the transistor as a current generator [5], the output transition time of CMOS cell can be directly obtained from the modelling of the (dis)charging current that flows during the switching process of the structure and from the amount of charge ($C_L \cdot V_{DD}$) to be exchanged with the output node as

$$\tau_{outHL} = C_L \cdot V_{DD} / I_{NMax} \tag{4}$$

where C_L represents the total output load, I_{NMax} is the maximum current available in the structure. The key point here is to evaluate this maximum current which depends on the input controlling condition. For that, two domains have to be considered: the fast input and the slow input range. In the fast input range, the driving condition imposes a constant and maximum current value in the structure. The current expression can then be directly obtained from eq.1 [6]. Combining equations 1 and 4 finally leads to the output transition time expression in the fast input range

$$\tau_{outHL}^{Fast} = \tau_{N/P} \cdot DW_{HL/LH} \cdot \frac{Cl}{C_{N/P}} = \frac{DW_{HL/LH} \cdot Cl}{K_{N/P} \cdot W_{N/P} \cdot (V_{DD} - V_{TN/P})^{\alpha_{N/P}}} \tag{5}$$

where $DW_{HL/LH}$ are the logical effort of the considered CMOS structure, $C_{N/P}$ are N/P gate capacitance and finally

$$\tau_N = \frac{Cox \cdot L \cdot V_{DD}}{K_N \cdot (V_{DD} - V_{TN})^{\alpha_N}} \quad \tau_P = \frac{Cox \cdot L \cdot V_{DD}}{K_P \cdot (V_{DD} - V_{TP})^{\alpha_P}} \tag{6}$$

are process metrics since these parameters capture the sensitivity of the output transition time to both the V_{DD} and the V_T values. In the slow input range, the maximum switching current decreases with the input ramp duration. Extending the results of [5] to general value of the velocity saturation index, the maximum switching current flowing in a CMOS structure is

$$I_{N/PMax}^{Slow} = \left\{ \frac{(\alpha_{N/P} \cdot K_{N/P} \cdot W_{N/P})^{1/\alpha_{N/P}} \cdot Cl \cdot V_{DD}^2}{\tau_{in}} \right\}^{\frac{\alpha_{N/P}}{\alpha_{N/P}+1}} \tag{7}$$

Combining (4) and (5) with (7), we finally obtain a manageable transition time expression for a falling output edge

$$\tau_{outHL}^{Slow} = \left(\frac{V_{DD} - V_{TN}}{\alpha^{1/\alpha_N} \cdot V_{DD}} \right)^{\frac{\alpha_N}{1+\alpha_N}} \cdot \left(\tau_{outHL}^{Fast} \cdot \tau_{IN} \right)^{1/\alpha_N + 1} = \left(\frac{Cl \cdot \tau_{IN} \cdot V_{DD}^{1-\alpha_N}}{\alpha^{1/\alpha_N} \cdot K_N \cdot W_N} \right)^{\frac{1}{1+\alpha_N}} \tag{8}$$

with an equivalent expression for the rising edge. To conclude with the modeling of the output transition time, one can observe that in the fast input range the transition time only depends on the output load while in the slow input range, it also depends on the input transition time duration but is threshold voltage independent.

B. Propagation Delay Modeling

The delay of a CMOS gate is load, gate size and input slew dependent. Following [7], the input slope and the I/O coupling can be introduced in the propagation delay as

$$t_{HL/LH} = \frac{\tau_{in}}{\alpha_{N/P} + 1} \left(\frac{\alpha_{N/P} - 1}{2} + v_{TN/P} \right) + \left(1 + \frac{2C_M}{C_M + C_L} \right) \frac{\tau_{outHL/LH}}{2} \tag{9}$$

This demonstrates the full delay sensitivity to the switching environment (τ_{IN}, τ_{out}). Considering the transition time dependency to the current (4), eq.9 will be of great importance in characterizing the temperature sensitivity of designs.

IV Temperature Inversion: Cell Characterization

This section details how it is possible to include the temperature derating coefficient, defined in section II, in the timing performance representation summarized below. In the section III, we show that the τ parameter is a direct representation of the process performance, and that the transition time and the delay expressions directly characterize the cell and circuit level with respect to τ parameter. Thus the modeling of the τ parameter temperature sensitivity must allow characterizing the temperature sensitivities of the timing performances of CMOS structures. This section highlights this point.

A. Process Level

First, we study the impact of the temperature inversion phenomenon on the performance metric. As shown in (4) the temperature dependency of the τ parameter is completely defined from that of the current. From (3) we can also easily define a derating factor $Der_\tau(V_{DD},\theta)$ of the process parameter τ as

$$\frac{\tau(V_{DD},\theta)}{\tau_{nom}\left(V_{DD}^{nom},\theta_{nom}\right)} = Der_\tau(V_{DD},\theta) = \left(\frac{\theta}{\theta_{nom}}\right)^{Xk}\left(\frac{V_{DD}}{V_{DD}^{nom}}\right)\cdot\left(\frac{V_{DD}^{nom}-V_{Tnom}}{V_{DD}-V_{Tnom}+\delta\cdot(\theta-\theta_{nom})}\right)^{\alpha} \quad (10)$$

To characterize the temperature sensitivity of the process it is just necessary to apply this coefficient to the τ metric of each transistor, since this parameter captures the output transition time and propagation delay sensitivity to both the supply and threshold voltage values.

Table 2. Simulated and calculated $\tau_{N/P}$ values for each PVT corner

Process B	τ_P (ps) Simulation			Error (%) Model vs. Sim.			τ_N (ps) Simulation			Error (%) Model vs. Sim.		
V_{DD} (V)	1.08	1.20	1.32	1.08	1.20	1.32	1.08	1.20	1.32	1.08	1.20	1.32
θ=233K	36.6	26.9	21.9	-0.7	-2.2	-6.1	13.9	9.6	7.4	0.1	-4.4	-7.2
θ=298K	33.2	26.2	21.8	0.3	0	-1.1	14.2	10.2	8.0	-1.0	0	0.1
θ=398K	31.2	25.6	21.9	-3.2	-0.7	0.9	14.5	11.1	9.1	-2.5	1.4	3.1

To validate this approach, we applied the derating coefficient (10) to the PMOS and NMOS transistors of the process B that exhibits (Fig.1) a temperature inversion point above the operating V_{DD} value. This has been done in three steps. First step has been devoted to the extraction of the $\tau_{N/P}$ values from simulations for all PVT corners. In a second step, we calibrated the model on the nominal V_{DD} and θ values to obtain the values of $\delta_{N/P}$ $Xk_{N/P}$ coefficients. Finally, we applied the derating coefficient (10) to the nominal $\tau_{N/P}$ values to obtain the $\tau_{N/P}$ values for all others PVT conditions. Results are reported in Table 2. As expected, the PMOS transistor of the process B is inverted on the whole V_{DD} range and is temperature independent at V_{DD}=1.32V. On the other hand, Table 2 shows that the NMOS transistor is not impacted by the temperature inversion phenomenon. This could be guessed from Table 1 hat shows that the inversion voltage (1.05V) is smaller than the worst case supply voltage. Finally, according to the expressions (5, 8, 9), we may conclude that the timing performance parameters (rising edge only) will be impacted by the temperature inversion. The worst case PVT occurs at the worst case process defined by small V_{DD} and low temperature values. For this process the main result obtained on the τ sensitivity is that the falling edge is not impacted by the temperature inversion. At 1.08V the sensitivity to the temperature is very small but the worst case operating mode corresponds to the standard definition with high temperature and low V_{DD} values. As a summary, for the B process, both edges vary in an opposite ways. The temperature coefficient of the transition time is negative (-0.15ps/°K) for the rising edges, while the falling edges exhibit a small but positive temperature coefficient (+0.04ps/°K). In that condition the critical operating mode will be defined by the rising edge.

The conclusion of this paragraph is that the $\tau_{N/P}$ coefficients are usefull to characterize the I_{DS} variations with respect to all the PVT parameters. We have shown that

the model differentiates both edges to account of the N/P transistor dissymmetry. With respect to the V_{DD}, the threshold voltage appears to be the most temperature sensitive parameter, a 5% variation of V_T, can completely reverse the I_{DS} sensitivity.

B. Cell Level

At cell level we must consider the evolution of the transition time and the propagation delay values. As explain in [5] and sum up in part 3, the output transition time can exhibit two different evolutions depending on the controlling input conditions. Thus two different expressions have been developed: one for the fast input range (5) and the other for the slow input range (8). Considering the transition time, a brief analysis of these equations shows that, depending on the input controlling conditions, the temperature variation may affect differently the output transition time. Indeed an analysis of the switching current shows that (5) does depend on the V_T value while (8) does not. This means that in the slow input range the effect of temperature variations can affect the output transition time only through the parameter K. Consequently, the temperature coefficient of the output transition time can never be negative in the slow input range while it may be reversed in the fast input range. This result can be verified in Fig.3 and Fig. 4 that illustrates the evolution of the output transition of an inverter with the input ramp duration. As shown the output transition time exhibits a positive temperature coefficient in the slow input range, while in the fast input range, this coefficient is positive for the A process, and negative for the B process.

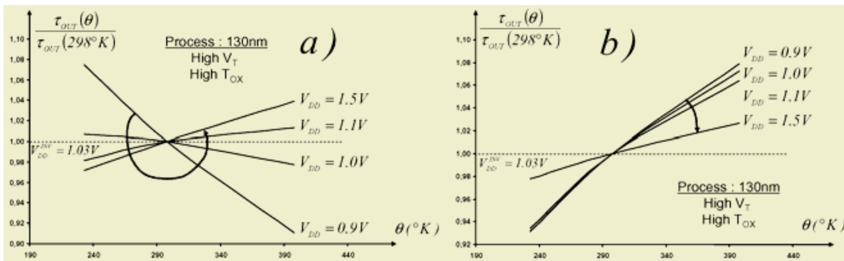

Fig. 3. Inverter output transition time (process B) vs temperature for different V_{DD} and input ramp duration a) a fast input ramp (τ_{IN}=10ps) and b) a slow input ramp (τ_{IN} =1780ps)

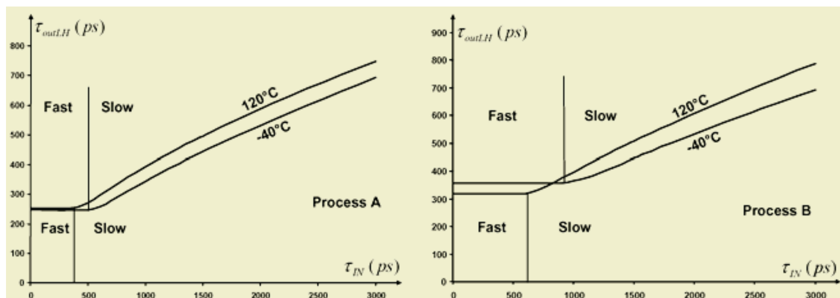

Fig. 4. Inverter output transition time vs input ramp duration for two different θ values

As for the output transition time, the analysis of temperature variation effects on the propagation delay must also distinguish between the fast and slow input ramp domains. As shown by eq.9, the propagation delay is the sum of two terms. Since the second term of the propagation delay is a fraction of the output transition time, all the results obtained in the preceding paragraph remain true for this fraction of the propagation delay. However these results are not sufficient to capture all the temperature variation effects on the propagation delay. Indeed, the first term of the propagation delay, which models the input slope effect, is directly proportional to the input ramp duration and to the threshold voltage value as

$$\frac{1}{\alpha_N + 1} \cdot \left(\frac{(\alpha_N - 1)}{2} + v_{TN} \right) \cdot \tau_{IN} \tag{11}$$

Thus the evolution of the propagation delay with the temperature is strongly influenced by the decrease of v_T value with the increase of temperature. More precisely for any structure there is always an input ramp value, $\tau_{IN}^{Inversion}$, after which the temperature coefficient of the propagation delay is necessarily negative. This limit value can either occur in the fast or the slow input design range. In order to evaluate, the value of $\tau_{IN}^{Inversion}$, we compute in the fast input range the partial derivative of the propagation delay expression with respect to the temperature and cancelled it to obtain the input ramp limit:

$$\tau_{IN}^{Inversion} = \frac{\alpha_N + 1}{\delta_N} \cdot \left(1 + \frac{2C_M}{C_M + C_L} \right) \cdot \tau_{outHL}^{Fast}(\theta_{nom}, V_{DD}) \cdot \left[\frac{X_{kN}}{\theta} - \frac{\alpha_N \cdot \delta_N}{V_{DD} - V_{Tnom} + \delta(\theta - \theta_{nom})} \right] \tag{12}$$

As shown the input transition time value controlling the temperature inversion of the delay is load dependent. One can note that this limit can be negative. This means that the temperature coefficient of the propagation delay is negative on all the fast input range. In the slow input range, the preceding procedure leads to the following input ramp duration limit:

$$\tau_{IN}^{Inversion} = \left(\frac{\alpha_N + 1}{\delta_N} \cdot \frac{\chi_{kN}}{\theta} \right)^{\frac{\alpha_N + 1}{\alpha_N}} \cdot \left(1 + \frac{2C_M}{C_M + C_L} \right) \left(\frac{V_{DD} - V_{Tnom}}{\alpha^{\frac{1}{\alpha}} \cdot V_{DD}} \right) \cdot \left(\tau_{outHL}^{Fast}(\theta_{nom}, V_{DD}) \right)^{\frac{1}{\alpha_N}} \tag{13}$$

As previously mentioned expressions (12) and (13) predict that there is always an input ramp value after which the temperature coefficient of the propagation delay is necessarily negative due to the reduction of the V_T value with the temperature increase. However in all the studied processes, the reduction with increasing temperature of the term (11) was enough important to place the input ramp limit value in the fast input range. This can be understood since the only process subjected to temperature inversion phenomenon is a high threshold voltage process used to limit the leakage currents.

Moreover, as shown in (9), the temperature coefficient of the delay may be less or more imposed by the input ramp duration dependency, that is proportional to the threshold voltage value. As an illustration of this temperature effect, we give in Fig.5 the normalized propagation delay evolutions with θ for a fast input and a slow input ramp. Fig.6 gives respectively the evolution of the propagation delay with the input ramp duration for two different temperature and output load values. As shown for the process B, the temperature dependency of the delay is as expected: the critical con-

figuration is observed at low temperature. On the contrary for process A, a strong input ramp duration dependency of the delay temperature coefficient is obtained. For quite slow input ramps the temperature coefficient is reversed and the critical case is observed at the lowest temperature.

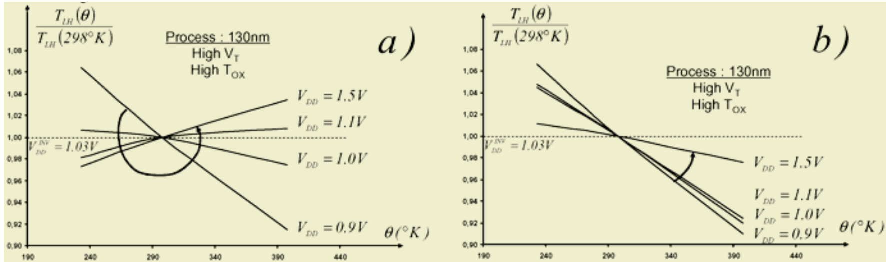

Fig. 5. Inverter propagation delay (process A) vs θ: a) for a fast input ramp (τ_{IN}= 10ps), b) for a slow input ramp (τ_{IN} = 1780ps)

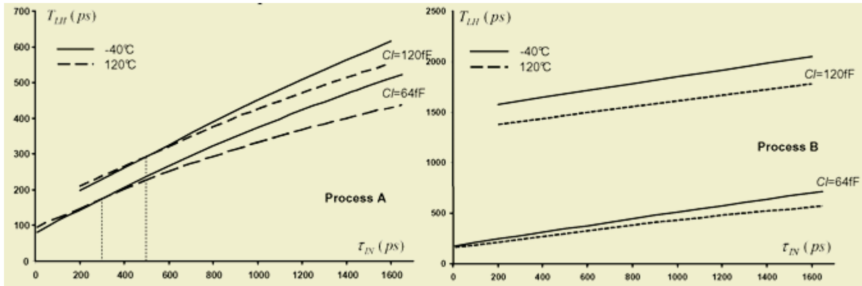

Fig. 6. Inverter propagation delay vs input ramp duration for different θ and C_L conditions

In Table 3, we validate (12). For each loading condition (process A) we impose an input ramp corresponding to the limit defined in (12), and simulate the delay of an inverter for the corresponding load and different temperature conditions. As shown we obtain a quasi temperature insensitivity of the delay, as predicted by (12).

Table 3. Delay for several temperature and C_L values for the input slope calculated with (12)

Load / Temp.	Delay (ps) at $\tau_{IN} = \tau_{IN}$ limit			
	4 fF	**64fF**	**120fF**	**640fF**
-40 C	42.8	176.5	301.5	1474.6
25 C	42.3	175.3	299.6	1466.2
125 C	42.2	175.2	299.8	1467.9

Independently of the considered input range, expressions (12) and (13) allow to conclude that the $\tau_{IN}^{Inversion}$ value depends on design parameters such as the load and the transistor widths. It thus appears difficult to characterize the temperature effects on performances using few and constant derating factors, since the temperature effects are radically different and depending on the operating design conditions.

C. Path / Circuit Level

For a real design both edges have to be taken into account during the STA and the timing behavior with respect to the temperature is not easy to predict. To illustrate this situation let us consider the four critical paths extracted from a real design.

We have simulated these paths for 4 different temperature values and a given supply voltage and a process condition. The results are given on figure 7a. As shown the worst case delays are obtained at either high or low temperature depending on the considered path. This confirms that the temperature effect on the timing is design dependent.

To definitively validate the proposed model, we compared the delay values obtained successively with Eldo and the model for several logic paths extracted from the same design operating under several PVT conditions. Typical results are given in fig. 7b. As shown, the accuracy of the proposed model is good, but the most interesting result is that the model predicts accurately the evolution of the propagation delays with temperature.

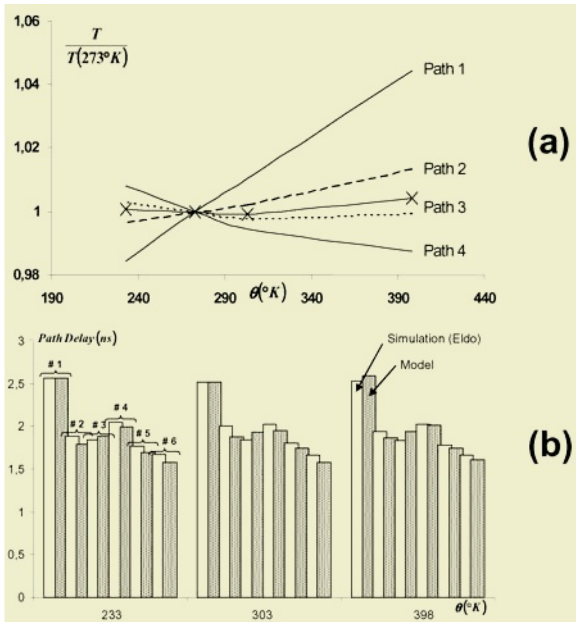

Fig. 7. (a) Temperature dependence for 4 critical paths for one PV condition, (b) Simulated and calculated Paths delay evolution with the temperature for the process B

V Conclusion

Considering the physical parameters that affect the temperature sensitivity of transistor currents, we have defined a model allowing capturing the non linear effects of temperature variations on performances. We have demonstrated the possibility to predict the occurrence of the temperature inversion phenomenon on design performance. It has been shown that critical corner for design characterization may evolve

from high to low temperature. Then, with the model properties, design guidelines and methodologies have been defined to take into account the temperature inversion phenomenon for design validation of real circuits.

References

1. S.M. Sze,"Physics of semiconductor devices", Wiley ed. 1983.
2. Changhae Park et al, "Reversal of temperature dependence of integrated circuits operating at very low voltages", Proc. IEDM conference, pp.71-74, 1995.
3. Synopsys Inc.,"Scalable Polynomial Delay And Power Model", Rev 5, October 2002.
4. P. Maurine and al, "Transition time modeling in deep submicron CMOS" IEEE Trans. on Computer Aided Design, vol.21, n11, pp.1352-1363, nov.2002.
5. B. Lasbouygues and al "Continuous representation of the performance of a CMOS library", European Solid-State Circuits, ESSIRC'03 Conf. pp.595-598, 16-18 Sept 2003.
6. T. Sakurai and A.R. Newton,"Alpha-power model, and its application to CMOS inverter delay and other formulas", J. Solid State Circuits vol. 25,pp. 584-594, April 1990.
7. K.O. Jeppson, “Modeling the Influence of the Transistor Gain Ratio and the Input-to-Output Coupling Capacitance on the CMOS Inverter Delay”, IEEE JSSC, Vol. 29, pp. 646-654, 1994.
8. J.M. Daga, E. Ottaviano, D. Auvergne, “Temperature effect on delay for low voltage applications”, Design Automation and Test in Europe, pp 680-685, 23-26 Feb. 1998, Paris.
9. J.A. Power and all, “An Investigation of MOSFET Statistical and Temperature Effects”, IEEE Int. Conf. on Microelectronic & Test Structures, Vol. 5, pp.202-207, March 1992.
10. A. Osman and al, “An Extended Tanh Law MOSFET Model for High Temperature Circuit Simulation”, IEEE JSSC, Vol. 30, No2, pp.147-150, Feb. 1995.
11. Shih-Wei Sun, P.G.Y.Tsui, "Limitations of CMOS Supply- Voltage scaling by MOSFET threshold voltage variation", IEEE J. of Solid State Circuits, Vol.30, N°8, pp.947-949, August 1995.