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Abstract. Scan architectures, though widely used in modern designs for testing purpose, are expensive in power consumption. In this paper, we first discuss the issues of excessive peak power consumption during scan testing. We next show that taking care of high current levels during the test cycle is highly relevant so as to avoid noise phenomena such as IR-drop or Ground Bounce. Next, we discuss a set of possible solutions to minimize peak power during all test cycles of a scan testing process. These solutions cover power-aware design solutions, scan chain stitching techniques and pattern modification heuristics.

1 Introduction

While many techniques have evolved to address power minimization during the functional mode of operation, it is now mandatory to manage power during the test mode. Circuit activity is substantially higher during test than during functional mode, and the resulting excessive power consumption can cause structural damage or severe decrease in reliability of the circuit under test (CUT) [1-4].

The problem of excessive power during test is much more severe during scan testing as each test pattern requires a large number of shift operations that contribute to unnecessarily increase the switching activity [2]. As today's low-power designs adopt the approach of "just-enough" energy to keep the system working to deliver the required functions, the difference in power consumption between test and normal mode may be of several orders of magnitude [3].

In this paper, we first discuss the issues of excessive peak power consumption during scan testing. As explained in the next section, peak power consumption is much more difficult to control than average test power and is therefore the topic of interest in this paper. We present the results of an analysis performed on scan version of benchmark circuits, showing that peak power during the test cycle (i.e. between launch and capture) is in the same order of magnitude than peak power during the load/unload cycles. Considering that i) logic values (i.e. test responses) have to be captured/latched during the *test cycle* (TC) while no value has to be captured/stored during the load/unload cycles, and ii) TC is generally operated at-speed, we highlight the importance of reducing peak power during TC so as to avoid phenomena such as IR-drop or ground bounce that may lead to yield loss during manufacturing test.

Next, we present a set of possible solutions to reduce peak power during TC. We first discuss straightforward power-aware design solutions that consist in over sizing

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power and ground rails. Then, we discuss two other classes of solutions: those based on some modifications of the scan chain and its associated clock scheme (scan chain stitching) and those based on power-aware assignment of don't care bits in patterns of the deterministic test sequence (X filling techniques). All these solutions can achieve significant reductions in peak power consumption during TC. Selecting one of them depends on its impact on some parameters such as additional DfT features, circuit design modifications, design flow adjustments, test application time and pattern volume increase, at-speed testing capabilities, etc.

The rest of the paper is organized as follows. In the next section, we discuss peak power issues during scan testing. In Section 3, we analyze peak power during the test cycles of scan testing and we highlight the importance of reducing this component of the power. In Section 4, we discuss possible solutions to reduce peak power during all test cycles of scan testing. Section 5 concludes this paper.

2 Peak Power Issues

Power consumption must be analyzed from two different perspectives. Average test power consumption is, as the name implies, the average power utilized over a long period of operation or a large number of clock cycles. Instantaneous power or peak power (which is the maximum value of the instantaneous power) is the amount of power required during a small instant of time such as the portion of a clock cycle immediately following the system clock rising or falling edge. In [4], it is reported that test power consumption tends to exceed functional power consumption in both of these measures.

Average power consumption during scan testing can be controlled by reducing the scan clock frequency – a well known solution used in industry. In contrast, peak power consumption during scan testing is independent of the clock frequency and hence is much more difficult to control. Among the power-aware scan testing techniques proposed recently (a survey of these techniques is given in [5] and [6]), only a few of them relates directly to peak power. As reported in recent industrial experiences [3], scan patterns in some designs may consume much more peak power over the normal mode and can result in failures during manufacturing test. For example, if the instantaneous power is really high, the temperature in some part of the die can exceed the limit of thermal capacity and then causes instant damage to the chip. In practice, destruction really occurs when the instantaneous power exceeds the maximum power allowance during several successive clock cycles and not simply during one single clock cycle [3]. Therefore, these temperature-related or heat dissipation problems relate more to elevated average power than peak power. The main problem with excessive peak power concerns yield reduction and is explained in the sequel.

With high speed, excessive peak power during test causes high rates of current (di/dt) in the power and ground rails and hence leads to excessive power and ground noise (V_{DD} or Ground bounce). This can erroneously change the logic state of some circuit nodes and cause some good dies to fail the test, thus leading to unnecessary loss of yield. Similarly, IR-drop and crosstalk effects are phenomena that may show up an error in test mode but not in functional mode. IR-drop refers to the amount of decrease (increase) in the power (ground) rail voltage due to the resistance of the devices between the rail and a node of interest in the CUT. Crosstalk relates to ca-

pacitive coupling between neighboring nets within an IC. With high peak current demands during test, the voltages at some gates in the circuit are reduced. This causes these gates to exhibit higher delays, possibly leading to test fails and yield loss [7]. This phenomenon is reported in reports from a variety of companies, in particular when at-speed transition delay testing is done [3]. Typical example of voltage drop and ground bounce sensitive applications is Gigabit switches containing millions of logic gates.

3 Analysis of Peak Power During Scan

During scan testing, each test vector is first scanned into the scan chain(s). After a number of load/unload clock cycles, a last shift in the scan chain launches the test vector. The scan enable (SE) signal is switched to zero, thus allowing the test response to be captured/latched in the scan chain(s) at the next clock pulse (see Figure 1). After that, SE switches to one, and the test response is scanned out as the next test vector is scanned in.

There can be a peak power violation (the peak power exceeding a specified limit) during either the load/unload cycles or during TC. In both cases, a peak power violation can occur because the number of flip-flops that change value in each clock cycle can be really higher than that during functional operation. In [7], it is reported that only 10-20 % of the flip-flops in an ASIC change value during one clock cycle in functional mode, while 35-40 % of these flip-flops commutate during scan testing.

In order to analyze when peak power violation can occur during scan testing, we conducted a set of experiments on benchmark circuits. Considering a single scan chain composed of n scan cells and a deterministic test sequence for each design, we measured the current consumed by the combinational logic during each clock cycle of the scan process. We pointed out the maximum value of current during the n load/unload cycles of the scan process and during TC (which last during a single clock cycle). Note that current during TC is due to transitions generated in the circuit by the launch of the deterministic test vector V_n (see Figure 1).

Identification of peak power violation cannot be done without direct comparison with current (or power) measurement made during functional mode. However, this would require knowledge of functional data for each benchmark circuit. As these data are not available, the highest values of current we pointed out are not necessarily peak power (current) violations. There are simply power (current) values that can lead to peak power (current) violation during scan testing. Reports made from industrial experiences have shown that such violations can really occur during scan testing [3] [4].

The benchmarking process was performed on circuits of the ISCAS'89 and ITC'99 benchmark suites. We report in Table 1 the main features for some of these circuits. We give the number of scan cells, the number of gates, the number of test patterns and the fault coverage (FC). All experiments are based on deterministic testing from the ATPG tool "TetraMAX™" of Synopsys [8]. The missing faults in the FC column are the redundant or aborted faults. Primary inputs and primary outputs were not included in the scan chain, but were assumed to be held constant during scan-in and scan-out operations. Random initial logic values were assumed for the scan flip-flops.

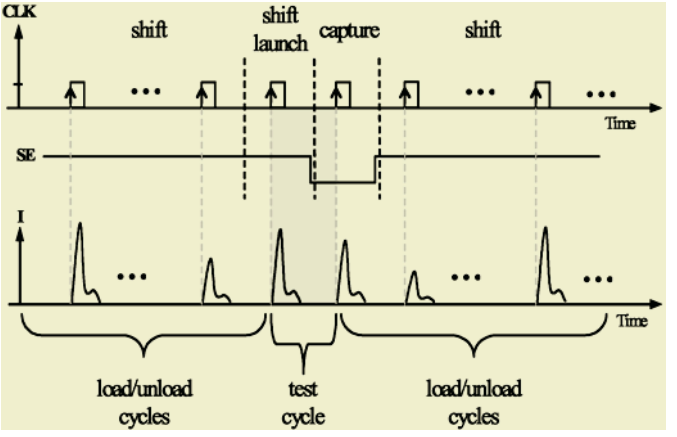

Fig. 1. Scan testing and current waveform

Table 1. Features of experimented circuits

Circuit	# cells	# gates	# patterns	FC (%)
b14s	245	4444	419	99.52
b17s	1415	22645	752	98.99
s9234	228	5597	161	99.76
s13207	669	7951	255	99.99
s38417	1636	22179	145	100

Results concerning peak power consumption are given in Table 2. We have reported the peak power consumed during the load/unload cycles and that consumed during TC. These values are a maximum over the entire test sequence. Power consumption in each circuit was estimated by using PowerMill® of Synopsys [9], assuming a power supply voltage of 2.5 Volts and technology parameters extracted from a 0.25µm digital CMOS standard cell library. These results show that peak power consumption is always higher during the load/unload cycles than during TC. This result was quite predictable as the number of clock cycles during the load/unload phase is much more than one. More importantly, these results show that even if peak power is higher during the load/unload cycles, peak power during TC is in the same order of magnitude. This may lead to problematic noise phenomena during TC whereas these phenomena do not impact the load/unload process. Let us consider again the IR-drop phenomenon. As discussed earlier, it is due to a high peak current demand that reduces the voltages at some gates in the CUT and hence causes these gates to exhibit higher delays. The gate delays do not affect the load/unload process as no value has to be captured/stored during this phase. Conversely, the gate delays can really affect TC because the values of output nodes in the combinational logic have to be captured in the scan flip-flops. As this operation is generally performed at-speed, this phenomenon is therefore likely to occur during this phase and negatively impact test results and thus yield. We can therefore conclude that taking care of peak power during TC and trying to minimize the switching density of the circuit during this phase are really relevant and requires new development of dedicated techniques.

Table 2. Peak power consumption during scan testing

Circuit	Peak during load/unload	Peak during test cycle
b14s	395.55 mW	319.83 mW
b17s	1038.35 mW	1118.68 mW
s9234	358.68 mW	339.88 mW
s13207	499.68 mW	483.30 mW
s38417	1121.80 mW	1074.33 mW

4 Possible Solutions to Reduce Peak Power During the Test Cycle

Considering the fact that minimizing peak power during TC is needed, we present in this section a set of possible solutions to reduce peak power during TC. We first discuss straightforward power-aware design solutions. Then, we discuss two classes of solutions: those based on modifications of the scan chain and its associated clock scheme (scan chain stitching) and those based on power-aware assignment of don't care bits in patterns of the deterministic test sequence (X filling techniques).

4.1 Power-Aware Design Solution

In order to reduce peak power during the test cycles, a straightforward approach would consist in reducing the resistance of the power/ground nets by over sizing power and ground rails. This solution has the advantage to be simple to implement and has limited side effect, i.e. low area overhead. However, this solution requires early in the design flow an estimation of the increase in power consumption during test with respect to power consumption during functional mode. As test data are generally not available at the early phases of the design process, this solution may not be satisfactory in all cases.

4.2 Scan Chain Stitching

A possible solution to reduce peak power during TC consists in partitioning the scan chain into multiple sub scan chains, called "scan segments", and acting on clock signals accordingly. Each scan segment is activated alternately, thus allowing a reduction of the CUT activity during both load/unload cycles and the test cycle. From this basic mode of operation, two types of solutions have already been imagined.

The low power scan architectures proposed in [10] and [11] are based on a gated clock scheme for the scan chain and the clock tree feeding the scan chain. The idea is to reduce the clock rate on the scan cells during shift operations without increasing the test time. For this purpose, a clock whose speed is half of the normal speed is used to activate one half (first scan segment) of the scan cells during one clock cycle of the scan operation. During the next clock cycle, the second half of the scan cells (second scan segment) in the scan chain is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with the system clock and have the same but shifted in time (non-overlapping) period during scan operations. During capture operations, the two clocks operate as the system clock so that a unique clock signal is used. Capture operations are operated using a single clock

cycle. In case more than two segments are defined during scan chain partitioning, the process is modified accordingly. Experiments performed on benchmark circuits have shown that this technique can reduce peak power during TC by approximately a factor of two, without affecting the test time and the performance of the circuit.

Another technique has been presented in [12] that achieve power reduction during both shift and capture operations with no impact on the performance of the design and with a minimal impact on area and testing time. This technique consists in splitting the scan chain into a given number of length-balanced segments and in enabling only one scan segment during each test clock cycle. The difference with the previous proposed techniques [10,11] is that in this case, each test response is captured using more than one clock cycle, e.g. two clock cycles for a two-segment scan chain. Peak power during TC is reduced by a factor which is roughly equal to the number of scan segments. Such a solution requires each scan segment to be structurally independent from the others so as to insure no capture violation.

These two types of solutions can reduce peak power during TC because in both cases, test launch is operated in more than one clock cycle. However, the main disadvantage is that they do not allow at-speed testing, due to multiple scan shifting and/or capture phases, and hence prevent detection of timing defects.

Another possible solution to reduce peak power during TC is to use scan cell reordering. Scan cell reordering consists in determining the order in which the scan cells of a scan chain have to be connected to minimize the occurrence of transitions during all test cycles. It can be demonstrated that this combinatorial optimization problem is NP-hard - the number of possible solutions is n! where n is the number of scan cells in the scan chain. Due to its exponential nature, this problem cannot be solved by an exact method. Heuristics have therefore to be used.

In [13], we have proposed such a scan cell reordering solution that this time allows at-speed testing. From the set of scan cells and a pre-computed sequence of deterministic test vectors, a heuristic process provides a scan chain order that minimizes the occurrence of transitions and hence the peak power during TC. The problem has been formulated as a global optimization problem (we try to minimize peak power during TC for all vectors of the test sequence) and a polynomial-time approximation solution based on a greedy algorithm has been implemented.

Experiments performed on ISCAS'89 and ITC'99 benchmark circuits have been done to measure the reduction in peak power obtained during TC. A sample of these results is shown in Table 3. For each circuit, we report the peak power during TC obtained first from an ordering provided by an industrial tool and next with the ordering technique proposed in [13]. For the evaluation in both cases, the deterministic test sequences presented in Table 1 were used assuming random initial logic values for the scan flip-flops. The industrial ordering has been performed by using the layout synthesis tool Silicon Ensemble® of Cadence Design System [14]. This synthesis tool allows first to perform scan insertion in the design corresponding to the experimented circuit and next the placement and routing of flip-flops in the design with respect to delay and area constraints. For each circuit, the design and the ordering of the scan chain have been carried out with a random placement of the scan-in and scan-out pins. Peak power is expressed in milliWatts and the values reported for each circuit are a mean of peak power (or instantaneous power) consumed during each test cycle of the scan process. Note that these values differ from those in Table 2 which

represent a maximum over the entire test sequence. The last column in Table 3 shows the reduction in peak power dissipation expressed in percentages. Complete results on benchmark circuits have shown that peak power reduction up to 30% can be achieved with the ordering technique proposed in [13]. Note that many other algorithms can be used to perform low power scan cell ordering. We are currently working on a constrained global optimization problem (minimizing peak power during TC for all vectors of the test sequence while maintaining each vector under a "violation" limit) by developing and implementing a heuristic solution based on Simulated Annealing.

Table 3. Peak power savings in the CUT by scan cell reordering

Circuit	Peak – Industrial solution	Peak - Proposed solution	Reduction
b14s	197.17 mW	172.87 mW	12.3 %
b17s	949.47 mW	837.70 mW	11.8 %
s9234	247.32 mW	200.74 mW	18.8 %
s13207	405.56 mW	337.03 mW	16.9 %
s38417	993.22 mW	746.08 mW	24.9 %

Compared with other low power scan techniques, this solution offers numerous advantages. It works for any conventional scan design - no extra DfT logic is required – and both the fault coverage and the overall test time are left unchanged. However, several practical implications of this solution have to be discussed.

First, the heuristic procedure does not explicitly consider constraints such as the placement of scan in and scan out pins or the existence of multiple scan chains with multiple clock domains in the CUT. In this case, the proposed technique has to be modified to allow these constraints to be satisfied. For example, scan chain heads and tails may be predefined and pre-assigned in the case of constraints on scan in and scan out pin position. This kind of pre-assignment may be important to avoid long wires between external scan/out pins and scan chain heads/tails.

In the case of circuits with multiple scan chains and multiple clock domains, which are common in industrial designs, almost no modification of the proposed technique is required. Actually, each scan chain can be considered separately and the heuristic procedure has to be applied successively on each scan chain.

The main drawback of this scan ordering technique is that power-driven chaining of scan cells cannot guarantee short scan connections and prevent congestion problems during scan routing. To avoid this problem, several solutions can be proposed depending on the DfT level at which the peak power problem is considered. First, if scan reordering can be performed before scan synthesis (in this case, flip-flop placement is not already done), the solution is to consider a DfT synthesis tool that can accept a fixed scan cell order (produced by our heuristic) and from which it can optimally place and route the scan resources. Now, if scan reordering cannot be done before scan synthesis (in this case, flip-flop placement is known and fixed), a solution to consider routing is to apply a clustering process as the one developed in [15] that allows to design power-optimized scan chains under a given routing constraint. In this case, the routing constraint is defined as the maximum length accepted for scan connections. Results given in [15] have shown very good tradeoff between test power reduction and impact on scan routing. Note that in all situations, ATPG is done earlier in the design flow.

4.3 X Filling Techniques

In conventional ATPG, don't care bits (Xs) are filled in randomly, and then the resulting completely specified pattern is simulated to confirm detection of all targeted faults and to measure the amount of "fortuitous detection" – faults which where not explicitly targeted during pattern generation but were detected anyway. It is interesting to note that the fraction of don't care bits in a given pattern is nearly always a very large fraction of the total available bits [16]. This observation remains true despite the application of state-of-the-art dynamic and static test pattern compaction techniques. The presence of significant fraction of don't care bits presents an opportunity that can be exploited for power minimization.

In order to avoid congestion problems inherent to scan chain modification techniques and to allow at-speed testing, pattern modification techniques can be used to reduce peak power during TC. Here, the idea is to use a test generation process during which non-random filling is used to assign values to don't care bits (Xs) of each test pattern of the deterministic test sequence. For example, it is possible to apply the following non-random filling heuristics:

- Don't care '0': all don't care bits in a test pattern are set to '0'
- Don't care '1': all don't care bits in a test pattern are set to '1'
- Adjacent filling: all don't care bits in a test pattern are set to the value of the last encountered care bit (working from left to right).When applying adjacent filling, the most recent care bit value is used to replace each `X' value. When a new care bit is encountered, its value is used for the adjacent X's

For example, consider a single test pattern that looks like the following: 0XXX1XX0XX0XX. If we apply each one of the three non-random filling heuristics, the resulting pattern will be:

- 0000100000000 with '0' filling
- 0111111011011 with '1' filling
- 0000111000000 with adjacent filling.

These non-random filling heuristics (among few others) have been evaluated in [7] to measure the reduction in average power consumption during scan shifting (load/unload cycles). Results reported in [7] indicate that the adjacent filling technique does an excellent job of lowering overall switching activity while still maintaining a reasonably increase in pattern volume.

From our side, we have evaluated these heuristics to measure the reduction in peak power consumption during TC with respect to a random filling of don't care bits. Results obtained with the adjacent filling heuristic are reported in Table 4. As for results in Table 3, the values reported for each circuit are a mean of peak power (or instantaneous power) consumed during each test cycle of the scan process. These results show significant reduction in peak power during TC (up to 89%) with an increase of the overall pattern volume ranging from 0 to 15% (3.9% on average for the complete set of experimented circuits).

Pattern modification techniques are therefore promising solutions to reduce peak power during TC. In addition, these techniques require no modification of the basic design of the circuit and no additional DfT features are required to implement these solutions. Finally, at-speed testing is possible so that the defect coverage of the initial

test sequence can be maintained. Our future work will consist in investigating much more on this type of solutions.

Table 4. Peak power savings in the CUT with adjacent filling

Circuit	Peak – Random filling	Peak – Adjacent filling	Reduction
b14s	178.00 mW	131.23 mW	26.3 %
b17s	961.86 mW	191.07 mW	80.1 %
s9234	240.02 mW	80.39 mW	66.5 %
s13207	402.62 mW	42.33 mW	89.5 %
s38417	978.10 mW	275.80 mW	71.8 %

5 Conclusion

In this paper, we have shown that excessive peak power consumption during all test cycles of scan testing has to be controlled to avoid noise phenomena such as IR-drop or ground bounce. Without caution, these phenomena may lead to yield loss during manufacturing test as test cycles are generally operated at-speed.

The reduction of peak power during TC can be addressed from different perspectives. First, we can perform circuit design implementation considering test power constraints. Next, modifications applied on the scan chain, the scan clock scheme or the test patterns can also be used.

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