Test Engineering Education in Europe: The EuNICE Test Project

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TEST ENGINEERING EDUCATION IN EUROPE

The CRTC experience through the EuNICE-Test project

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Abstract: The present paper describes the CRTC and EuNICE-Test project actions and outcomes. The original idea was to build a long-lasting European Network for test engineering education using both test resource mutualisation and remote experiments. This objective is fully fulfilled and we have now, in Europe, five centers of competence able to deliver high-level and high-specialized training courses in the field of test engineering using a high-performing industrial ATE. All the centers propose training courses on digital testing, three of them propose mixed-signal trainings and three of them propose memory trainings. Taking into account the demand in test engineering, the network is planned to continue in a stand alone mode.

Key words: Test Engineering, Education, Distant learning, ATE, Remote testing

1. THE CRTC PLATFORM

1.1 Economical context

The cost of the production test for mixed-signal circuits is a very strategic challenge for the competitiveness of the microelectronics industry. Such circuits are mixed-signal devices that contain both digital and analogue blocks. They may be:

- high added-value ASICs (Application Specific Integrated Circuits)
- composite MCMs (Multi-Chip Modules) with mixed technologies

- New-age SoCs (Systems-on-Chip) designed from IP (Intellectual Property) modules.

These mixed-signal circuits constitute the major part of modern communication devices and their fabrication is strongly boosted by the tremendous growth of the multimedia/telecom market.

Nowadays, testing mixed-signal circuits (the so-called mixed-signal testing) is a very critical economical challenge. In some cases, the test of a multimedia/telecom circuit may constitute up to 50% of its total cost [1]. Moreover, due to the growing complexity of IP-based SoC devices, this high percentage is planned to increase significantly in the years to come. The global test cost for a given circuit mainly includes the cost for test development, the cost for implementing the full characterization test on high-tech engineering testers and the cost for using highly efficient production testers. To give an idea of the economical importance of testing problems, we have to keep in mind that the production test floor of a circuit founder typically consists of about one hundred 1M€ testers. Such testers are used in three eight-hour shifts per day and all year round.

1.2 The CNFM Test Resources Center (CRTC)

CRTC ("Centre de Ressources de Test du CNFM") has been created in France by CNFM ("Comité National de Formation en Microélectronique") to respond to the industrial demand in engineers with a double Design & Test competence. The CNFM is the French institution which coordinates initial training and continuous education in microelectronics. For more than 15 years, the CNFM has been in charge of the coordination between universities, microelectronics industries and French authorities. This is a consortium that groups the 11 French universities and academic centers involved in microelectronics education. This consortium aims at bringing together heavy soft (CAD tools) and hard resources (clean rooms, ATEs,…) for a common use, at a lower price.

In 1997, the CNFM decided to create a common test resources center (the so-called CRTC) which concentrates up-to-date and high-tech test resources in a single CNFM center, the so-called PCM ("Pôle CNFM de Montpellier"). A mixed approach has been chosen for test education implementation that combines both distributed and centralized test resources. Indeed, considering the huge cost of high-tech IC testers, the policy of CNFM was to develop one and one only test center for all the French academic centers. So in 1998, the LIRMM was chosen to implement the CRTC. In addition, to avoid any excessive travel expense for students from their university to CRTC in

Montpellier, the implementation has been thought to make the CRTC testers reachable by net from any remote center.

CRTC is mainly equipped with an up-to-date/high-tech ATE Agilent 83000-F330t (Figure 1). In each of the 11 CNFM centers, a server with test software facilities is implemented to allow the local development of test programs.

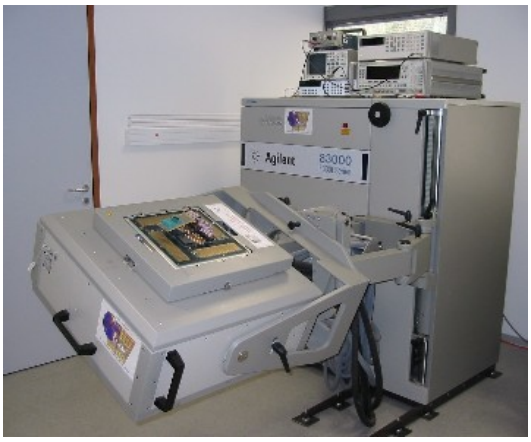

Figure 1. Agilent 83000-F330t

1.3 Test Resource Sharing and Remote Testing

The network is articulated around CRTC common test resources. The advantage of having a one and only one resource centre for all the project partners is obvious. Mutualisation allows putting very performing up-to-date testers at partner's disposal. This saves money by avoiding the replica of clearly underused test resources in several scattered centers. On the other hand, in a context of a "mass education", the price to pay for having centralized resources is the traveling and lodging costs for trainees. So, the original idea of the CRTC project was to permit a network connection on the common tester to implement a remote test of the circuit. Using this configuration, up to 16 students may be locally trained in parallel using the 8 workstations connected on a server equipped with software test development resources. Only at the very last moment of the physical test they have to be connected to the tester through the network (Figure 2).

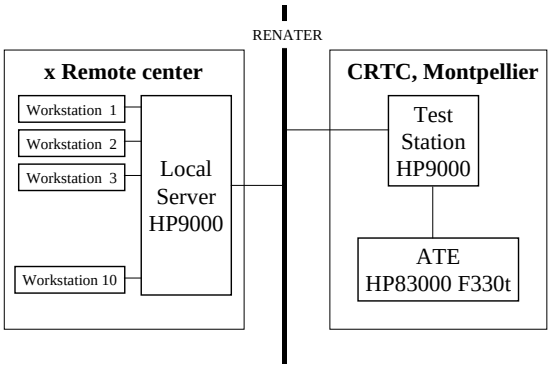

Figure 2. Network implementation for remote testing

Training courses are open for pre- and post-doctoral students from universities or engineering schools. The training contents are issued from those developed by Agilent for the 83000 tester [2-4].

Digital training courses aim to initiate students and engineers to digital IC test. After completing level 1 training, each trainee will be able to (i) make competent use of any digital ATE to test a device for its performance parameters and specifications, (ii) build up a test flow to automate the test execution and (iii) create a test program to be executed on the production test floor. After completing level 2 training, he will have gained the know-how to (i) test complex devices, (ii) convert simulation data and (iii) make optimum use of tester resources. Both training courses use a standard digital circuit as DUT (Device Under Test) to simply illustrate all the test functions. Each training course is built up on lessons and related lab exercises. The network configuration of CRTC allows any trainee in any distant center to prepare lab exercises using the local resources. Also the correctness of both input signal shapes and output strobe locations may be locally verified. Only the test execution itself necessitates a remote connection on the CRTC tester in Montpellier.

Mixed-signal training courses aim to initiate students and engineers to the test of analogue and mixed-signal circuits. After completing the training, students are able to make competent use of the Agilent 83000 F330 to test a mixed-signal device for its performance parameters and specifications. They are prepared to plan appropriate tests by utilizing the SmartDSP instruments. They are able to develop test programs for mixed-signal devices and use the available tools for developing and debugging mixed-signal tests.

Memory training courses aim to initiate students and engineers to the test of various types of memory, including memories embedded in SoC. After completing the training, students have an overview of the common elements of a memory device, and what is involved in testing memories. They know how the memory test software works, and how to set up and execute a memory test using the user interface. Finally, they learn how to use the result tools that enable to characterize the device.

2. THE EuNICE-Test PROJECT

2.1 Project Objectives

EuNICE-Test acronym stands for European Network for Initial and Continuing Education in VLSI/SOC Testing using remote ATE facilities. This is a 2-year long European IST (Information Society Technology) project that was completed in September 2003. The objective of the project was to address the shortage of skills in the microelectronics industry by educating students at pre- and post-doctoral levels in the field of test engineering. The idea was to strengthen leading educational centers in critical disciplines of design and test in microelectronics with the active support and guidance of industry. At the starting point of the project, initial education in that field was too little developed in Europe, just restricted to the French experience with 200 students and engineers trained per year. Taking into account the context described above, there was a strong demand from the microelectronics industry in engineers having knowledge ranging from the simple awareness of test problems (design engineers) to the full skill and competence in IC testing (product engineer, test engineer). It was the objective of the present educational project to respond this demand by implementing a European network for test engineering education both in initial and continuing education perspective.

In this context, EuNICE-Test project aims to be the seed of a European network for initial and continuing education in test engineering in order to respond the industrial demand for microelectronics engineers having a double Design & Test competence. This educational project is based upon the successful experience [5-8] of CRTC. The expansion at European level includes 4 new academic partners (see Figure 4), namely UPC Barcelona (Spain) [UPC], Politecnico di Torino (Italy) [Polito], University of Stuttgart (Germany) [UST] and Institute Jozef Stefan of Ljubljana (Slovenia) [JSI]. Agilent Technologies [Agilent] is the key industrial partner of the project for

providing up-to-date equipment and specific education on clearly identified hot test topics. CRTC [CRTC/LIRMM] is the leader of the project. Because CRTC is hosted by a research laboratory (LIRMM, www.lirmm.fr) internationally renowned in the field of circuit testing, it benefits from the competence of these permanent researchers. The teaching staff of CRTC is composed of researchers and professors fully implicated in various research projects on the design and test of integrated circuits and systems. Such projects include DFT and BIST for digital, analogue and mixed-signal circuits and design and test of fully integrated microsystems. Also, all the other participants in the consortium have a full competence and expertise in the field of IC testing. This ensures both solid theoretical background and up-to-date test knowledge for the trainees. Finally, the project benefits from the Agilent Technologies active support. This partnership allows taking advantage of the very last technological developments for ATEs and ensures the achievement of skill and practical knowledge for the trainees through the use of advanced test equipment.

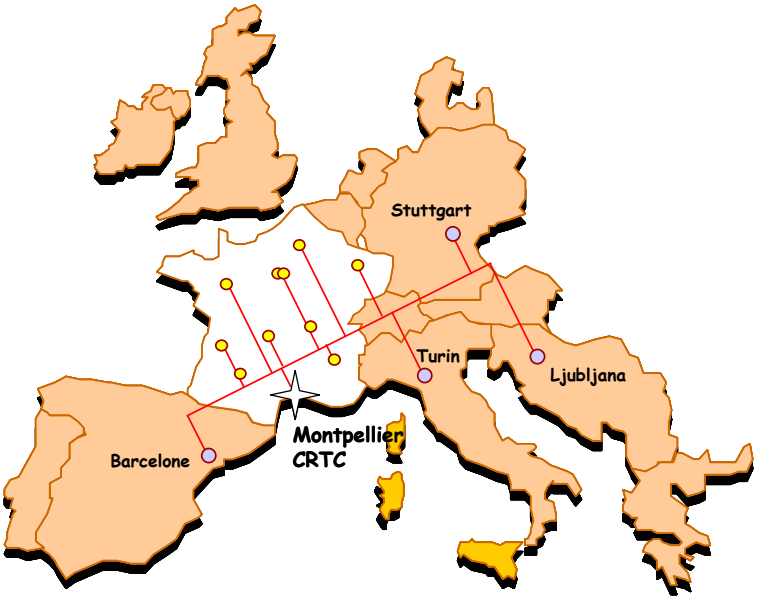

Figure 3. National and European network for test education

2.2 Project work plan

EuNICE-Test project was a two-year long project divided into four interdependent work-packages. The Gann chart of these work-packages is given in Figure 4. The trainers of each academic partner have been first trained to test engineering on the Agilent 83K tester of CRTC in Montpellier (WP1: Digital Training for Trainers). Next, these trainers have performed the same training course to their students, concurrently in each centre [UPS, Polito, UST and JSI] (WP2: Training implementation). Finally, the industrial partner [Agilent] taught academic participants to specific test techniques (WP3: Specialized Test Training for Trainers) and one of the partners [JSI] organized a specialized training to their students (WP4: Mixed-signal Test Training implementation). So at the end of the project, each academic centre is specialized in a given test field: mixed-signal test and/or memory test.

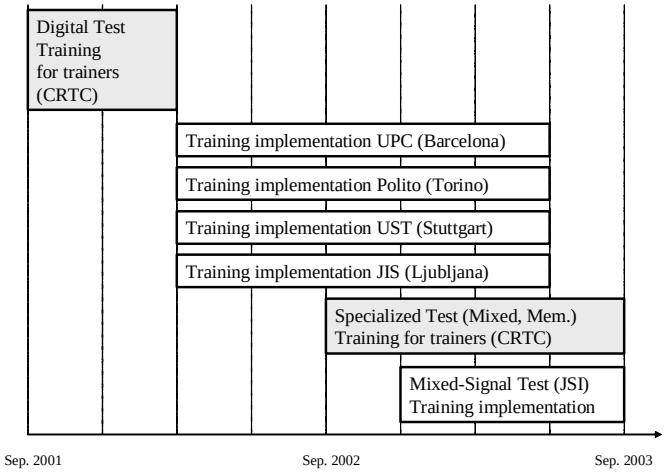

Figure 4. EuNICE-Test project planning

2.3 Training implementation

All the tasks of the Gann chart of Figure 4 have been completed on time according to original schedule. First, all the European trainers (9 people) have been trained in digital test at CRTC during two weeks. Then the set-up

of the four centers has been completed for student local education. This set-up covers:

- Equipment purchase order & installation
- Software installation and running
- Network and Internet connection up and running
- First successful online connection to ATE.

The way each training course for student is implemented depends on the local context. The global organization of syllabus, the initial level of the students and the pedagogical approach of the teaching team make the organization is different in terms of number of students, number of groups and course duration (see Table 1). This demonstrates the good adaptability of the remote system. Once a working time slot is reserved through the Web site of CRTC [9], the tester is fully devoted to the remote centre. Then the teacher is free to dispose of the tester, exactly as if it was located on the local site, and he can implement the training at his own convenience.

The initial objective of training 16 students per academic centre during the project has been globally respected. Of course, depending on local context and need, the figures vary a little bit but the mean value of trained student is around 17. During the EuNICE-Test mid-term meeting in Stuttgart (September 2002) the efficiency of remote test connection for educating student in digital test has been demonstrated by a demo and approved by both the European referee and the European Project Officer.

So, the EuNICE-Test project has permitted training 69 additional students in digital test in Europe (Table 1). This gives an increase of 43% compared to the sole educational program in France (160 trainees).

Table 1. Digital Training Implementation in European Centers

Centre	# Students	# Groups	# Students per group	# Days	# Hours Per student (Lecture + Labs)	# Trainers
UPC	10	5	2	6	18 + 24	3
POLIT	25	6	4 (or 5)	16	22 + 14	2
JSI	21	2 x 5	2 (or 3)	6	6 + 9	2
UST	13	6	2 (or 1)	10	20 + 20	2
Total	69					9
LIRMM	20	10	2	6	18 + 24	3
France	160					24

Also mixed-test and memory training for trainers have been implemented in each of the 4 European centers. All have been completed on time according to original schedule. Specialized test training on Mixed-Signal testing was organized in January 2003 at LIRMM/CRTC. Seven persons involved in the EuNICE-Test project participated to this specialized training: 2 from LIRMM/CRTC, 2 from UPC and 3 from JSI. In order to provide the project with the necessary hardware equipment, Agilent improved the CRTC Agilent 83000 F330t tester configuration. The following cards have been installed:

- SWI (Smart Waveform Instrument) card. This card features two independent but identical instruments called SWI channels. Each SWI channel contents an arbitrary waveform generator, a waveform digitizer, and a DSP.
- SWG (Smart Waveform Generator) card. This card can be used to generate up to four independent analogue signals, including high frequency sinusoid and video waveforms.
- SVS (Smart Video Sampler) card. This hardware is aimed at dynamic measurement of video signals. It contains also two waveform digitizers for general purpose applications.
- SCM (Smart Capture Memory). It can acquire up to 64K of 16 bits words at rate up to 50 MHz.

Specialized test training on Memory testing was organized in April 2003 at the Training Centre of Agilent Technologies (Böblingen, Germany). Seven trainers involved in the EuNICE-Test project participated to this specialized training: 3 from LIRMM/CRTC, 2 from Polito and 2 from UST.

Finally, as scheduled in the EuNICE-Test project, JSI has implemented a Mixed-Signal training course for its students. During the EuNICE-Test final meeting in Ljubljana (September 2003) the efficiency of remote test connection for educating student in mixed-signal testing has been demonstrated by a demo and approved by both the European reviewer and the European Project Officer.

2.4 Assessments

Let us now give the global feeling from the synthesis of the partner feedback (deliverable reports, e-mails, phone contacts, meeting at conferences, etc.).

Positive points:

- Global feedback is good
- To accede an up-to-date, industrial ATE is a very critical opportunity for electrical engineering education
- Training course is globally proved to be effective for student learning
- Technical collaboration with CRTC/LIRMM has been very satisfactory
- Average time for connecting Montpellier ATE is globally practicable even if strongly dependent on network traffic

Negative points:

- Training course is mainly designed to fulfill production test objectives. It is often necessary to add some introductory lectures to give the basics of test.
- The lack of physical contact with ATE is a little bit frustrating for students.

So, the global feedback from European partners about the implementation of these first training courses on digital test engineering is very good. The remote access has been proved to be very compliant and adaptable to local context. The opportunity of acceding to a real industrial test tool is fully appreciated. Depending of the level the training is given (MS, PhD) and taking into account the local educational context it may be necessary to add complementary lectures. The major drawback of the system is the lack of physical contact with the tester. In the future, it will be mandatory to add some video materials to compensate the student frustration of never seeing the tester. Finally, it is of interest to indicate that some European partner have created their own Web page to present the training course to their students.

2.5 Test Education Offer at European Level

Starting from the situation of 2001, we have clearly extended the opportunity for a European student to have high-level education in test engineering. The original French network composed of 10 centres connected on the CRTC resources (Figure 5) is now a European network with 4 new academic centers of excellence.

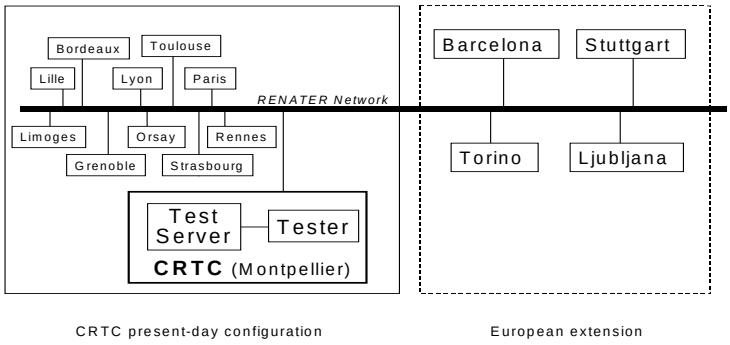

Figure 5. European network for test education

By the end of the project, test engineering knowledge dissemination now results in 3 European centers of competence in digital and mixed-signal testing and 3 European centers of competence in digital and memory testing (Table 2).

This configuration allows the per-year offer in test engineering education in Europe to be:

- 5 training courses in Digital Test
- 3 training courses in Mixed-Signal Test
- 3 training courses in Memory Test

Co-coordinated training scheduling should permit any European student to dispose several time slots for digital and/or specialized test training.

Table 2. Centers of competence in test engineering.

Center	Digital Test	M-S Test	Memory Test	Teaching Language
Montpellier (F)	✓	✓	✓	French / English
Barcelona (E)	✓	✓		Spanish / English
Torino (I)	✓		✓	Italian / English
Stuttgart (D)	✓		✓	German / English
Ljubljana (SI)	✓	✓		Slovenian / English

3. FORTHCOMING ISSUES

Since the end of the project (Sept. 2003), the CRTC platform has been continuously used for students training at both national and European levels. Table 3 shows the reservation status for the last two years.

Table 3. Tester reservation (hours) and number of trained students for 2003-2004.

Center	#Hours	#Students
National		
LIRMM – University of Montpellier	112	40
ENSERG – University of Grenoble	32	16
IXL - ENSEIRB – University of Bordeaux	64	16
LEPSI – University of Strasbourg	68	16
CEGELY - INSA de Lyon	48	16
ESINSA – Université de Nice Sophia Antipolis	56	16
AIME – Université Paul Sabatier - Toulouse	56	16
European		
UPC - Barcelona	168	20
Politecnico – Turino	8	4
UST - Stuttgart	160	26
IJS - Ljubljana	108	42
TOTAL		
	1224	**228**

Although the CRTC platform is still very active, some drop in the remote center activity has been observed recently, especially in the national network. There are two identified reasons for this:

- It is difficult for the remote centers to maintain the required HP-UX workstation, running an old operating system. With the current ATE, is it however the only way to run the test software.
- The Agilent 83000 does not support mixed-signal circuits testing conveniently. As mentioned above, such trainings have been implemented in the framework of the EuNICE-Test project but it was mainly for the purpose of demonstration.

In addition to those issues, the CRTC has to consider the short-term replacement of its testing equipment. This is rushed by the reality that Agilent company will not support the 83000 series after July 2006. A positive point is that it will be an opportunity to develop additional services and then extend the CRTC offer. For this, two options are under consideration:

- The purchase of an Agilent 93000 Soc series tester (figure 6). This solution obviously guaranties the platform continuity. Moreover, it allows extending the CRTC offer to mixed-signal circuits and memory testing. The main drawback of this approach is the difficulty to get academic or national funding to fully cover the cost of such tester. This project can be partially funded by industrial collaborations, for instance by making this equipment available for continuous education and private R&D. Note also that the development software for recently released testers is Linux compatible and thus only requires a basic computer to run.

- The implementation of training modules based on "virtual testing" platforms. Such software can emulate the behavior of real physical testers providing the same outputs by simply running a simulation engine. This option has advantages to rely on software tools that do not require huge amount of support in contrast to hardware. Because the device under test is also virtual (i.e. a model), it is possible to inject faults very simply and then to get trained on diagnosis tools. In terms of flexibility, this solution is ideal because each center can be totally autonomous. The main drawbacks are: (i) it only works for digital circuits so far and (ii) the licensing cost is still expensive compared to the mutualisation of one tester for years.

Figure 6. Agilent 93000 SOC Series tester.

4. CONCLUSION

The paper deals with a European experience of education in test engineering of ICs and SoCs, using remote testing facilities. The project addresses the issue of the shortage in microelectronics engineers aware of the new challenge of testing mixed-signal circuits for multimedia/telecom market. The project aims at providing test training facilities on a European scale, in both initial and continuing education contexts. This will be done by allowing the academic and industrial partners of the consortium to train engineers using the common test resource center (CRTC). CRTC test tools include an up-to-date/high-tech tester (Agilent 83000F330-t) that is fully representative of real industrial testers, as used on production testfloors.

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