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Efficient Test of Dynamic Read Destructive Faults in SRAM Memories*

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Abstract

This paper presents an analysis of the electrical origins of dynamic Read Destructive Faults (dRDFs) that affects the SRAM memories. This fault is the consequence of resistive-open defects in the refreshment loop of the SRAM core-cells. The consequence of this fault is that multiple consecutive read operations on a cell may induce the faulty swap of the stored value. In a recent paper, we have considered only two of the four possible dRDF fault primitives. Here, we complete this study by evaluating the effectiveness of all fault primitives. We also show that read or write operations on a cell involve a stress on the other cells of the same word line. This stress, called Read Equivalent Stress (RES), has the same effect as an actual read operation for the dRDF sensitization. On this basis, we demonstrate that RESs can replace actual read operations in the dRDF fault primitives making them more efficient.

1. Introduction

The System-on-Chip (SoC) paradigm is associated with a trend from logic-dominant chips to memory-dominant ones. From the ITRS documents [1], by 2013 over 90% of the chip will be occupied by different types of memories, e.g. embedded-SRAMs (e-SRAMs). The e-SRAMs are increasingly dense with and present more and more large capacity, thus they are more prone to faults, not only reducing memory and SoC yield but also posing new challenges for their test.

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Static faults such as stuck-at, transition and coupling faults are commonly used to validate SRAM blocks. These faults are sensitized by only one operation (read or write). Recent works show that VDSM (Very Deep Sub-Micron) technologies more frequently involve dynamic faults [2, 3]. To be sensitized these faults need more than one operation in sequence and traditional tests are not made to detect them [4].

Among the known dynamic faults that may affect SRAM memories, we concentrate our attention on those that concern the core-cell. One of these faults is the dynamic Read Destructive Fault (dRDF) [2, 5]. The first definition of this fault was: a write operation immediately followed by a read operation causes the swap of the logic value stored in the cell. So, such a fault requires a specific read/write sequence to be detected.

March RAW [5] (Read After Write) is an efficient solution to detect all single-cell dynamic faults in core-cells. Its complexity is 13N including the initialization. This algorithm detects dRDFs by March elements that perform a write operation followed by a read operation, *e.g.* w0r0. In [6] we have shown that this test can be improved by applying a sequence of read operations instead of a single read. The new sensitization sequences are $w0r0^M$ or $w1r1^M$, where $r0^M$ denotes a sequence of M successive r0 operations, *e.g.* $w0r0^2$ = w0r0r0. The multiple read operations, performed after the write operation, allow a more efficient fault sensitization. However, if a large number of read operations is needed, the test complexity may increase drastically.

In our recent work, we have proposed a more efficient alternative to March RAW [7]. Without increasing its complexity, we have improved the standard March C- algorithm (10N complexity) [8, 9] in order to make it able

to detect also dynamic Read Destructive faults in the core-cell. Our modified March C- detects dRDFs by using a particular addressing sequence. This modification is allowed by the first of the six Degrees of Freedom (DOF) [10] of March tests, and does not alter the capability to detect the former target faults.

The proposed algorithm does not produce directly the multiple read operations, but with the use of a particular addressing order all the memory core-cells undergo to an equivalent stress. During a read or write operation on a certain cell the pre-charge circuit is turned off in the relative column, but all the other columns have the pre-charge left on at Vdd. Consequently, all the cells on the same word line of the selected cell fight against the pre-charge circuit. In [7] we have shown that this event, that we call Read Equivalent Stress (RES), is equivalent to a read operation for the non-selected cells. In fact, during an actual read the cell is connected to its two bit lines that are floating at Vdd, having been previously precharged at voltage level. In other words, a read or write operation on a certain cell involves a stress (RES) on the other cells of the same word line similar to an actual read. This phenomenon can be used for dRDF sensitization.

In [7] we have considered only two of the four possible dRDF fault primitives defined in [2]. In this paper we complete this study by evaluating the effectiveness of all fault primitives. We also prove that RESs can efficiently replace the read operations in the fault primitives.

The rest of the paper is organized as follows. In Section 2 we give an overview of the simulation flow and definitions of fault models. Section 3 provides an analysis of the electrical origins of dRDF and of the effectiveness of the fault primitives useful to sensitize dRDFs. In Section 4 we present an efficient March test solution for dRDF. Concluding remarks are given in Section 5.

2. Simulation flow and definitions

In this section we propose a brief summary of the main results of our previous study on core-cell faulty behavior [6]. This study was oriented to the characterization of some faults induced by the injection of resistive-open defects in the core-cell of Infineon 0.13µm embedded SRAM memory. Figure 1 depicts the scheme of a standard 6-transitors cell where six different resistive-open defects have been inserted. The defects are placed on the interconnections, where they are more likely to appear. We do not consider all possible locations due to the symmetry of the structure. For example defect Df4' is the symmetric of defect Df4. The resistance values have been chosen from few ohm up to several Mohm in order to ensure a range large enough to obtain complete results from simulations.

In Table 1 we show for each resistive-open defect the corresponding fault models. Only defect Df4 induces a dynamic fault, in particular a dynamic Read Destructive Fault. As mentioned before, due to the symmetry of the circuit also defect Df4' produces a dRDF.

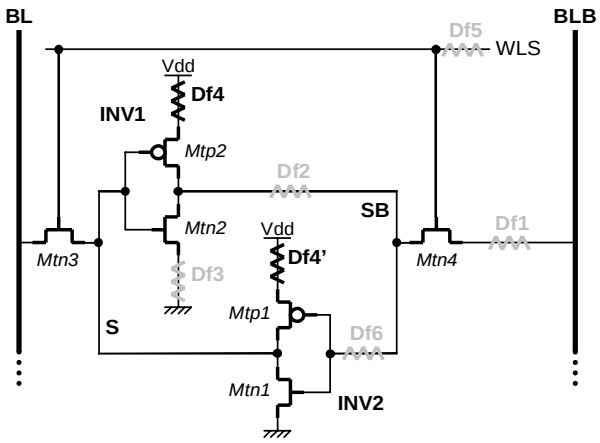

Figure 1: Resistive-open defects injected into the memory core-cell

Defect	*Extracted fault models*
Df 1	**TF**
Df 2	**DRDF-RDF**
Df 3	**DRDF-RDF**
Df 4	**dRDF**
Df 5	**IRF/TF**
Df 6	**TF**

Table 1: Summary of the fault models extracted for each inserted resistive-open defect.

The definitions of all the fault models reported in Table 1 are the following:

- Transition Fault (TF): *A cell is said to have a TF if it fails to undergo a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written.*
- Read Destructive Fault (RDF) [11]: *A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output.*
- dynamic Read Destructive Fault (dRDF) [2, 5]: *A cell is said to have an dRDF if a write operation **immediately** followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output.*
- Deceptive Read Destructive Fault (DRDF) [11]: *A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell.*
- Incorrect Read Fault (IRF): *A cell is said to have an IRF if a read operation performed on the cell*

returns an incorrect logic value, and the correct value is still stored in the cell.

In the rest of the paper we point out only on the dynamic Read Destructive Fault (dRDF) that occurs in presence of Df4 (and also its symmetric Df4'). The detection of the other fault models present in Table 1 is easy, in fact common March test are able to cover them.

3. dRDF Fault Primitives evaluation

Defect Df4 on transistor Mtp2 source induces a dynamic Read Destructive Fault that occurs when a zero is stored in the cell. A '0' stored corresponds to a '0' on node S and a '1' (Vdd) on node SB (see Figure 1). For the read operation, the two bit lines BL and BLB are pre-charged and left floating at Vdd. Then the cell is connected to the bit lines, the word line signal actives transistors Mtn3 and Mtn4, which are switched on. BLB and node SB are at the same potential, while BL and node S have a different potential. As BL has a high capacitance, its discharge is long. So, we can consider that BL and BLB values remain at Vdd at the beginning of the read operation. Moreover, the current in Mtn3 is high due to the voltage difference between BL and S. Node S is thus charged a little (0 + δV). As the value at the inverter INV1 input has slightly increased, the value at its output (SB) decreases because Mtp2 cannot compensate this lack of charge due to the presence of Df4. Consequently, SB voltage decreases a little (Vdd - δV) causing the degradation of the logic '0' on S. If SB value becomes close to Vdd/2, there is a swap of the value stored in the cell. Note that, in normal conditions, when there is not a resistive defect in the pull-up path of INV1, the current in the Mtp2 transistor is sufficient to maintain the SB node close to Vdd. Some times it is necessary to perform multiple read operations in sequence to degrade the voltage level of node SB enough to produce the swap of the cell. The same happens in presence of defect Df4' when '1' is stored and read operations are performed on the cell.

On this basis, for dRDFs we can define four FPs (Fault Primitives) that are the evolution of those proposed in [2, 5]. A FP is denoted as **<S/F/R>**. **S** describes the sensitizing sequence, which sensitizes the fault in the core-cell. **F** describes the value of the faulty cell; **F** ∈ {0, 1, ↑, ↓}, where ↑ (↓) denotes an up (down) transition due to a certain sensitizing operation. Finally, **R** describes the logic value which appears at the output of the memory. With this notation we propose four FPs for dRDF, which can be divided in two groups. The first group corresponds to defect Df4 and uses essentially w0 and r0 operations:

FP1: **<0w0r0^{M}/↑/1>** A '0' is initially stored in the cell. A w0 immediately followed by M r0 operations causes the swap of the cell and we observe a '1' at the memory output.

FP2: **<1w0r0^{M}/↑/1>** A '1' is initially stored on the cell. A w0 immediately followed by M r0 operations causes the swap of the cell and we observe a '1' at the memory output.

The second group of FPs corresponds to defect Df4' and uses essentially w1 and r1 operations:

FP3: **<1w1r1^{M}/↓/0>** A '1' is initially stored on the cell. A w1 immediately followed by M r1 operations causes the swap of the cell and we observe a '0' at the memory output.

FP4: **<0w1r1^{M}/↓/0>** A '0' is initially stored on the cell. A w1 immediately followed by M r1 operations causes the swap of the cell and we observe a '0' at the memory output.

Note that in each FPs M is a certain number of read operations so that M≥1. For example, <0w0r0^{2}/↑/1> means that 0 is stored in the cell and the sequence of operations w0r0^{2} = 0w0r0r0 induces the swap of the cell from '0' to '1'. Due to the symmetry of the core-cell circuit there are the following equivalences:

$$FP1 \equiv FP3 \text{ and } FP2 \equiv FP4$$

Consequently, for our analysis we can consider only FP1 and FP2. For the other FPs, the results are exactly the same.

The two FPs that we analyze are both referred to defect Df4. In Figure 2 and Figure 3 there are the waveforms relative to the hSpice simulations of the core cell with Df4 of 20 MΩ. The simulations have been performed with the following operation parameters: process typical, 1.6 V supply voltage, a temperature of 27 °C and a cycle time of 3 ns.

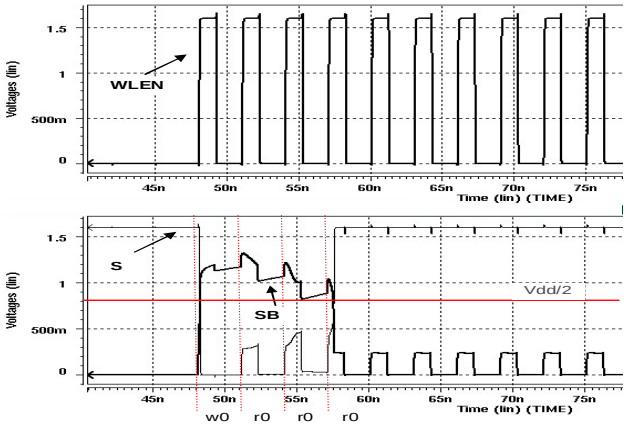

Figure 2: Waveforms of <1w0r0^{M}/↑/1> simulation (Df4)

Figure 2 gives an overview of FP1: <1w0r0^{M}/↑/1>. The logic value '1' is initially stored in the cell. A w0 is operated. SB node commutes from '0' to '1' without reaching the Vdd level due to the presence of the defect. At this point, '0' is stored in the cell but it is not perfectly

stable. Then the following multiple read operations degrade the voltage level of node SB until it reaches the threshold value of Vdd/2 after which the cell swaps. The cell commutes after 3 consecutive read operations.

The <0w0r0^M/↑/1> FP is illustrated by the waveforms of Figure 3. This time, in the cell a '0' is previously stored. This means node S is at '0' and node SB is at level '1'. We have obtained this condition by writing a '0' on the cell and letting it stabilizes until SB reaches the Vdd level. Firstly a w0 operation is performed on the cell that has no impact on the cell content. As previously, a sequence of r0 operations is then operated on the cell, which swaps after 12 reads.

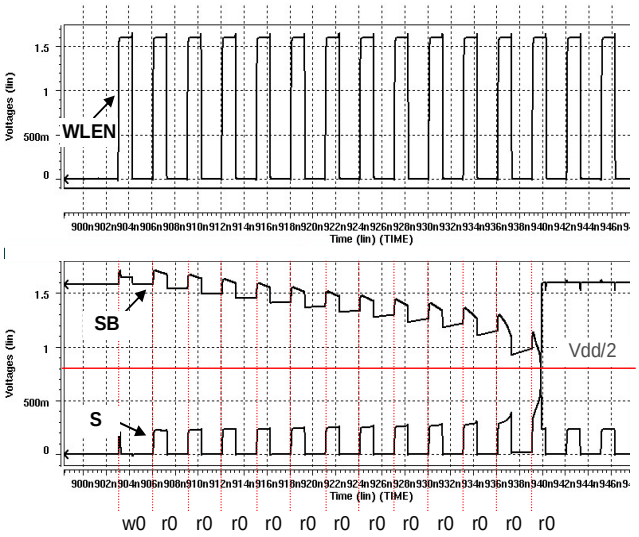

Figure 3: Waveforms of <0w0r0^M/↑/1> simulation (Df4)

With these results we can do a comparison of the two FPs. The first observation is that both FPs have the same electrical origin, *i.e.* a defect in the pull-up referred as Df4. But we can observe that there is a huge difference in the effectiveness of the FPs. In fact the number of operation, useful for the sensitization in the first case is 4 (1 write + 3 reads) while it is 13 (1 write + 12 reads) in the second one. We can explain this difference by the fact that in the first case the cell is not stable after the write operation because node SB has not reached the Vdd level. Consequently a littler number of read operations is necessary to induce the degradation of SB voltage to Vdd/2 and produce the faulty swap of the cell. So, it appears evident that detecting the FP <1w0r0^M/↑/1> is less expensive than <0w0r0^M/↑/1> in terms of test complexity, *i.e.* total number of operations.

What we have stated above is also valid for Df4', symmetrically placed with respect to Df4. This time, for the same reasons, among the two FPs (<1w1r1^M/↓/0> and <0w1r1^M/↓/0>) the most efficient is the second one.

4. Read equivalent stress for dRDFs detection

In the previous section it has been shown that a dRDF can be the consequence of resistive-open defects in the core-cell of SRAMs. In particular it has been empathized that in presence of the resistive-open defect Df4 the action of single or multiple read '0' immediately after a write '0' operation may cause the inversion of the value stored in the cell. Consequently, in order to sensitize this fault it is necessary that the test algorithm has sequences with multiple read operations like w0r0^M and w1r1^M for the symmetrically placed defects (Df4 and Df4'). In [7] we have demonstrated that a cell can undergo a stress equivalent to a read operation (Read Equivalent Stress, RES) when a read/write operation is performed on other cells of the same word line.

It is useful to remember that when a cell is selected for a read or write operation the pre-charge circuit is normally turned off in its bit line. For the bit lines that are not involved in the operation, the pre-charge circuit is commonly left on. With the pre-charge active and the word line being high on the unselected columns, the cells fight against the pre-charge circuit. A consequent deduction is that the stress produced by a read operation on a cell is equivalent to the stress caused by a read or write operation performed on whatever cell on the same word line. During a read action the perturbation of the cell is produced by the charge stored previously on its two bit lines, while in the other case the cell is stressed by the same bit line charge, but with the pre-charge circuit still on. In order to simplify what exposed above we produce the example referred to the scheme in Figure 4.

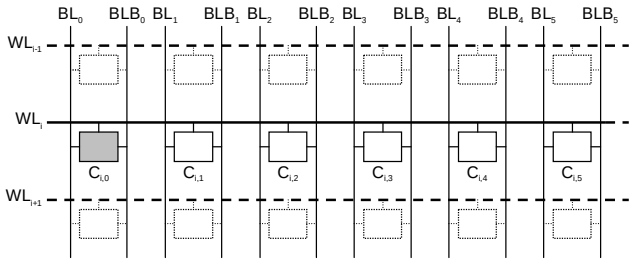

Figure 4: A portion of an SRAM block

This scheme depicts a section of an SRAM block, and in particular in the middle there are the first six cells of the word line WL_i. We assume that on WL_i the first cell on the left $C_{i,0}$ is affected by a resistive-open defect in the pull-up transistor of one of the two inverters (as Df4 in Figure 1). This defect may cause a dRDF. This fault is detectable when, immediately after a write data on cell $C_{i,0}$, one or multiple read operations are performed on the same cell. An equivalent faulty behavior can also occur when the write data in cell $C_{i,0}$ is followed by read or write operations on the other cells of the same world line. This is

possible because, if for example cell $C_{i,1}$ is selected, the pass transistors (Mnt3 and Mnt4 in Figure 1) of all the cells on the same word line, in particular the faulty cell $C_{i,0}$, are saturated. So, $C_{i,0}$ fights against the pre-charge circuit that is active, as for all the non-selected columns. Consequently, the faulty cell $C_{i,0}$ undergoes a stress (RES) similar to a read operation.

In [7] we have produced formal confirmations to the previous statements with electrical simulations that have been performed on Infineon 0.13 µm embedded-SRAM family with the Infineon internal SPICE-like simulator. We have considered a reference 8kx32 memory, organized as an array of 512 word lines x 512 bit lines. The cell array of this memory is split in 128 blocks. When a word line is selected all the 512 cells on this word line are connected to respective bit lines.

At this point we have analyzed the RESs capability to replace the actual read operations in the dRDFs FPs. Spice simulations have been performed with the same parameters of previous simulations and the same resistive value (Df4 = 20 MΩ). The waveforms in Figures 5 presents the results obtained for the new FP2 <1w0RES^M/↑/1> with RESs replacing the actual read operations. These RESs are obtained by acting read operations on others cells of the word line where the defective cell (with Df4) is present.

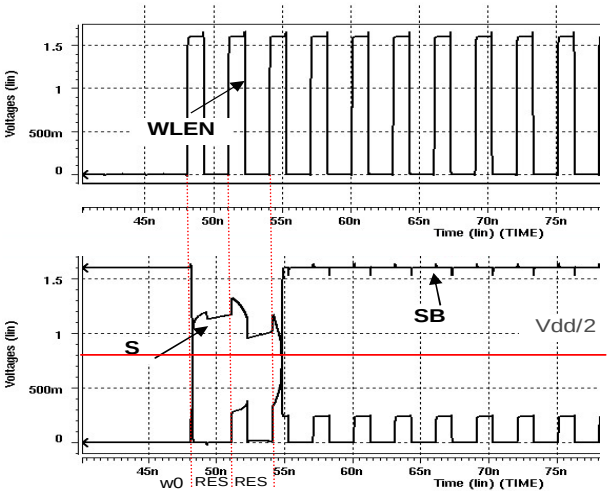

Figure 5: Waveforms of <1w0RES^M/↑/1> simulation (Df4)

After a first analysis we can deduce that RESs have the same effects than actual read operations in the fault sensitization. We can also note that RESs are more efficient. In fact, for the equivalent FP (see Figure 2) three read operations were necessary for the faulty swap while in this case only two RESs are required.

We have performed the same kind of simulation for the other equivalent FP: <0w0RES^M/↑/1>. The results that we have found are very similar to the previous case. The effectiveness of RESs for dRDFs sensitization is one more time demonstrated. In this occasion 11 RESs instead of 12 actual read operations are necessary to induce the faulty swap of the cell, as we can see in Figure 6.

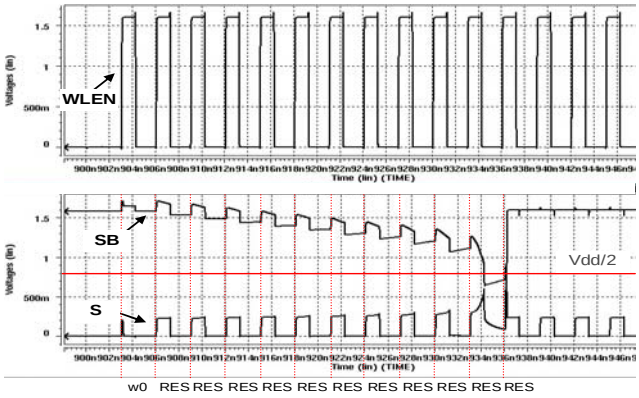

Figure 6: Waveforms of <0w0RES^M/↑/1> simulations (Df4)

What we have state above is also valid for Df4', symmetrically placed respect Df4. In fact, for the same reasons, among the two new FPs (<1w1RES^M/↓/0> and <0w1RES^M/↓/0>) the most efficient is the second one**.**

5. March test procedure

In order to use the RESs for the production of an efficient March test for the detection of the dRDF caused by Df4 the algorithm has to have the following requirements:

i. It is necessary that the read/write operations are performed with a particular addressing order with the purpose to execute the March elements on the memory array by acting on word line after word line. This is necessary because the RESs are produced only by operating on the cells of the same word line.

ii. The elements of the March test have to include w0 operations to sensitize the dynamic faults induced by Df4, w1 operations for those induced by the symmetrical resistive-open defect Df4'.

iii. The presence of r0 and r1 operations is necessary for observation.

iv. All the elements, in particular the sensitization ones, need to be performed in ⇑ and ⇓ sequence.

The last statement is necessary to obtain the best distribution of RESs on all the memory cells.

Considering the previous requirements, let us show how it is possible to produce an efficient test for all the FPs of dRDF. As done in [7] we propose to modify the already existing March C- in order to test dRDFs. March C is presented in Figure 7 and normally covers 0% of dRDF [5]. The modification is the following one: the read/write

operations of the algorithm have to be performed with a particular addressing order with the purpose to execute the March elements on the memory array by acting on word line after word line. The modification makes March C- able to detect dRDFs, though in the mean time, due to the first of the six degrees of freedom [10, 12] of March tests, it does not change the capability of March C- to detect the former target faults.

$$\{\ \Updownarrow(w0)\ \ \Uparrow(r0,w1)\ \ \Uparrow(r1,w0)\ \ \Downarrow(r0,w1)\ \ \Downarrow(r1,w0)\ \ \Updownarrow(r0)\ \}$$
$$M_0 \qquad M_1 \qquad M_2 \qquad M_3 \qquad M_4 \qquad M_5$$

Figure 7: March C- structure

This modified March C- is able to cover all the dRDF. In facts, some elements of March C- include w0 and w1 operations, necessary for sensitization of all the dRDF, and r0 and r1 necessary for their observation. Moreover, the elements, in particular the sensitization ones, are performed in ⇑ and ⇓ sequence. This condition allows that the cells endure a good average distribution of RESs along each entire word line.

The proposed March test solution presents many advantages as its linear complexity and the reutilization of an already existing March test. The main benefit is the high efficiency to detect dynamic faults.

6. Conclusions

With the present work we have studied the conditions for the sensitization of dynamic Read Destructive Faults that may occur in core-cells of SRAM memories in presence of resistive-open defect. In particular, we have analyzed the efficiency of the Fault Primitives useful for the dRDF detection and we have demonstrated that the best one is $<1w0r0^M/\uparrow/1>$ for defect Df4 and consequently its homologue $<0w1r1^M/\downarrow/0>$ for the symmetrical defect Df4'.

Moreover, we have shown that a cell undergoes a stress equivalent to a read operation, when a read/write operation is performed on a cell of the same word line. We have called this phenomenon Read Equivalent Stress (RES), and shown that RESs are more efficient than actual read operation to sensitize dRDFs. On these bases, we have introduced new FPs, with RESs at the place of actual read. We have evaluated the effectiveness of these new FPs and the most performing are $<1w0RES^M/\uparrow/1>$ and consequently its homologue $<0w1RES^M/\downarrow/0>$ for the symmetrical defect Df4'.

In last part of the paper we have shown how a modified March C- is able to produce a high number of RESs. This March procedure is able to detect efficiently dRDFs because it contains the two FPs $<1w0RES^M/\uparrow/1>$ and $<0w1RES^M/\downarrow/0>$. This modified March C- is also able to cover all the former target faults.

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