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OFFSET AND NOISE REJECTION ANALYSIS IN CMOS PIEZORESISTIVE SENSORS

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Abstract: In this paper, the use of piezoresistive CMOS beams is addressed with a particular focus on offset and noise rejection problems in a Wheatstone bridge. Using a test-chip (a magnetometer), the mismatch between resistors (on the substrate) and gauges (suspended) is experimentally studied. Both thermal and mechanical causes are analysed. Finally, mismatch cancellation techniques are reported.

Keywords: CMOS, MEMS, Offset, noise rejection

INTRODUCTION

The design of low-cost mechanical CMOS sensors often rely on the use of piezoresistive structures (basically cantilevers) [1]. Such structures are easily manufactured using a single-step, auto-aligned wet etching of CMOS dies and have demonstrated a high level of reliability. For instance, previous studies have shown that the performances of piezoresistive CMOS magnetometers in terms of sensitivity and resolution allow the measurement of earth magnetic field, making those devices suitable for navigational applications [2]. However, the system performance can only be raised to its optimum level by taking into account parasitic effects during the design of the surrounding circuitry. In this paper, the causes of offset and noise rejection are studied and solutions are proposed and compared.

TEST-CHIP OVERVIEW

The sensor under study is a magnetometer. It is made of an aluminium planar coil embedded into a partially suspended frame depicted in Fig.1. Two polysilicon resistors are located near the frame anchor points and act as strain gauges. Their resistance variations are converted into voltage variations by means of a Wheatstone bridge that requires two reference resistors deposited on the substrate. The best sensitivity to magnetic field is obtained by driving the frame at its resonant frequency (V/T). This sensitivity is quite poor and it must be improved by on-chip amplification. For instance, a compass application would require an amplification of about 20.000. When dealing with such elevated gain, offset must be considered carefully to prevent amplifier from saturation. Furthermore mismatch of the Wheatstone bridge cause a bad PSRR. In the following, the origins and the measurement of mismatch are described.

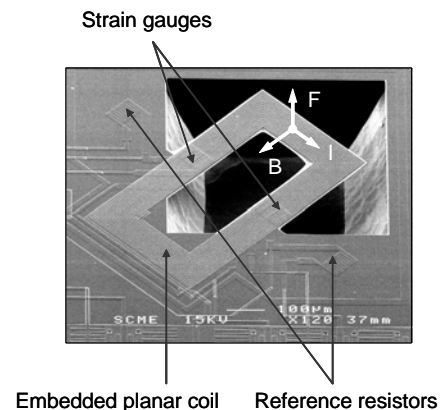


Fig. 1. SEM Picture of the sensor

MISMATCH ANALYSIS

Main offset results from the resistor mismatch on the Wheatstone bridge. In our case this mismatch has three main origins:

- Scatterings of the CMOS polysilicon deposition process;
- After the structure is released by the etching process, a stress relaxation mechanism occurs. This mechanism produces an initial bending of the frame that modifies the nominal value of the gauges resistors. The amplitude of this phenomenon is very difficult to predict since it depends on fabrication conditions;
- The temperature of the frame is higher than the temperature of the substrate due the power dissipated by both the Wheatstone bridge biasing and the driving coil.

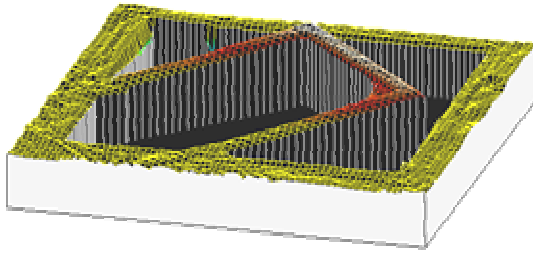
CMOS Process Mismatch

The four resistors are identically sketched on the layout. It usually guaranties a 0.1% matching between all resistors. With simulation tools (Monte-Carlo analysis), the standard deviation of the offset is found around 2mV with a Wheatstone bridge supplied by 5V. The offset is then guaranteed to be

inferior to 6mV for 99.7% of fabricated sensor. However, this precision is only obtained if a special care is given to placement of the resistors with respect to each other (e.g. symmetrical placement and use of dummy structures...). Due to the sensor configuration, the placement of the four resistors is not optimal and the expected mismatch may slightly differ from the specified value.

Residual Stress Mismatch

The second mismatch origin comes from the releasing process that modifies the level of residual stress in the gauges. In Fig. 2, the curvature radius r that appears on the sensing part after release has been measured at various locations.



#	1	2	3	4	5	6
r (mm)	3,32	3,04	2,11	2,52	3,31	2,22

Fig.2. Measurement of the curvature radius

This curvature radius results from an internal equivalent bending torque T given by:

$$\frac{1}{r} = \frac{T}{E_n I_n} \quad (1)$$

where E_n is the equivalent Young's modulus of the suspended beam and I_n the equivalent inertia of the beam cross section. Analytical modelling of E_n and I_n for heterogeneous beams have been addressed previously [3]. Taking into account the sensor dimensions and characterized CMOS material properties [4] we calculate $E_n = 131\text{GPa}$ and $I_n = 806\mu\text{m}^4$. Using an average radius of $r = 2.5\text{mm}$, the resulting bending torque is found to be $T = 42.2 \cdot 10^{-9}\text{N.m}$.

The same torque would be induced at the gauge location by a bending $z = 17.7\mu\text{m}$ of the cantilever end, as expressed by:

$$z = \frac{T \cdot L_c^2}{3 \cdot E_n I_n} \quad (2)$$

where $L_c = 364\mu\text{m}$ is the cantilever length. Given that the bending of the cantilever produces an output voltage of $700\mu\text{V}/\mu\text{m}$, the relative change of the gauge value is calculated as follows:

$$\frac{\Delta R}{R} = 700 \frac{2}{V_{dd}} z \quad (3)$$

Using $V_{dd} = 5\text{V}$, the resistor mismatch due to the residual stress equals 0.5%. The resultant offset at the output of the Wheatstone bridge is in the range of 10mV.

Thermal Mismatch

A qualitative study of thermal effect in the cantilever has been performed by means of infrared images. The temperature elevation is estimated this way for the three cases (Fig 3) :

- Only the gauges are biased (5V on the Wheatstone bridge).
- Only the coil is supplied (2,2mA current)
- Both gauges and coil are supplied.

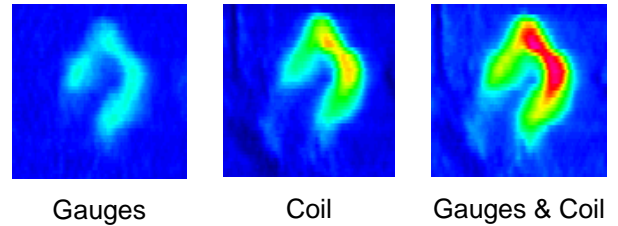


Fig.3. Temperature analysis on the suspended frame

The dissipated power in the gauges is $P_g = 6.25\text{mW}$. The power dissipated in the coil is in the same range $P_c = 6.36\text{mW}$. During sensor operation, the temperature elevation of the gauge depends on the equivalent thermal resistance of the frame R_{th} and R_{th}' as given by:

$$\theta_g = P_g R_{th} + P_c R_{th}' \quad (4)$$

In first approximation, $R_{th} = R_{th}'$. Consequently the contribution on the temperature elevation of the gauge biasing equals the contribution of the coil. In normal operation the temperature difference between the gauge and the reference resistors reaches 26°C . Thanks to the Temperature Coefficient of the Gauges (TCR), we can calculate the relative variation of gauge:

$$\frac{\Delta R}{R} = TCR \cdot \theta_g \quad (5)$$

Using $TCR = 0.9 \cdot 10^{-3}\text{K}^{-1}$ (given by the foundry), the temperature elevation induces a resistor mismatch of 2.34% corresponding to an offset of 58.5mV.

In summary, Fig.4 gives the absolute contribution of each effect on the static mismatch. We observe that 92% of the problem results from the micromachining process.

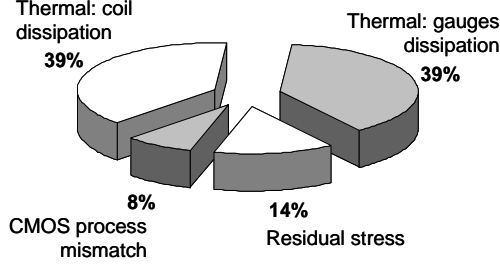


Fig. 4. Offset contributions

ELECTRICAL CHARACTERIZATION

Mismatch between gauges and the reference resistors are studied more in detail in the section thanks to electrical methods.

First, the thermal effect due to the coil is characterized. When no power is dissipated in the coil, the output of the Wheatstone bridge is measured. Then, 5V is applied across the coil, corresponding to a power of $P_c = 6.36\text{mW}$. The change in the output voltage ΔV_{out} is 22.6mV. Thus, the equivalent thermal resistance R_{th}' can be deduced:

$$R_{th}' = \frac{\Delta V_{out}}{(V_{dd}/2) \cdot TCR \cdot P_c} = 1580\text{K/W} \quad (6)$$

Thermal contribution of the gauges cannot be evaluated by the same way so the following method has been used instead. Offset data is collected using a test-chip that is electrically equivalent to the circuit depicted in Fig.5. Equivalent input offset ($V_a - V_b$) is measured for $V_{out} = 0\text{V}$. This offset is studied as a function of the electrical power dissipated in the suspended frame. To do this, the supply voltage V_b varies from 4.25V to 5.25V in order to avoid problem with the pad protection circuitry. Note that no driving current is applied to the coil during this measure. It comes:

$$(V_a - V_b) = 2 \left(\frac{V_b}{2} \times \frac{R_{gauge} - R_{ref}}{R_{ref}} + \varepsilon \right) \quad (7)$$

where ε is the input offset of the amplifier stage.

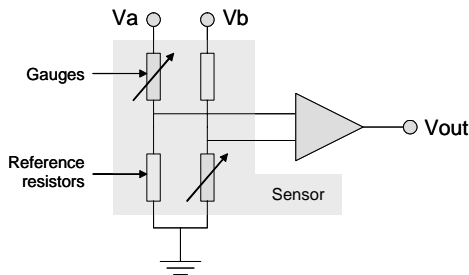


Fig. 5. Test-Chip equivalent circuit

The study has been performed on a set of 20 devices. Fig.6. presents the typical resistor mismatch collected for both a non-etched and a fully released sensor. Very good matching is observed between the four non-released resistors, while important mismatch appears between reference resistors and suspended gauges. The linear dependency to the temperature (i.e. the power dissipated) is also consistent with the polysilicon temperature coefficient TCR. The initial mismatch caused by stress relaxation only (i.e. $P_g = 0$) can be estimated, using the interpolation line to about -0.5%. It confirms the value calculated by measurement of the curvature radius. Note that the sign of this mismatch is the inverse of the one thermally induced. From the slope of the characteristic (Fig.6.), the equivalent thermal resistance related to dissipation of the gauges is:

$$R_{th} = \frac{1}{TCR} \cdot \frac{d(\Delta R / R)}{dP_j} = 2600\text{K/W} \quad (8)$$

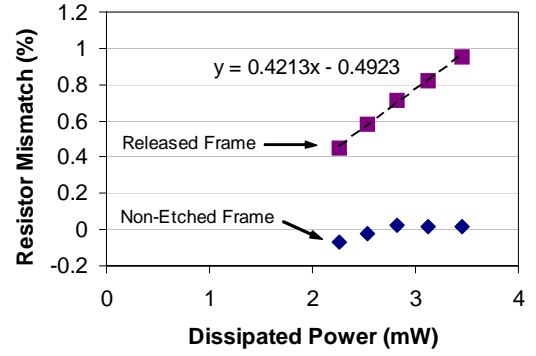


Fig. 6. Mismatch characterization results

Concerning the CMOS process mismatch, the offset has been characterised on 43 non etched frames. The standard deviation found is 6mV. It is three times bigger than the one evaluated by simulation but remains negligible compared to the other effects.

Finally, the overall mismatch causes an offset of 50 mV (in average) and a PSRR of 40dB. It strongly limits the possible gain of the amplifiers and then the resolution of the sensors.

DESIGN ISSUES

The main purpose of mismatch cancellation is to prevent the amplifier stage from saturation and decrease the sensitivity to power supply noise. Two approaches have been investigated and compared.

Dummy Frame

The first approach is based on the use of a dummy frame, insensitive to the magnetic field, with same thermal, mechanical and electrical properties than

the sensor. The coil is then replaced by a metal path going back and forth instead of making turns (Fig. 5). A similar design has been already successfully used in a bolometer [x].

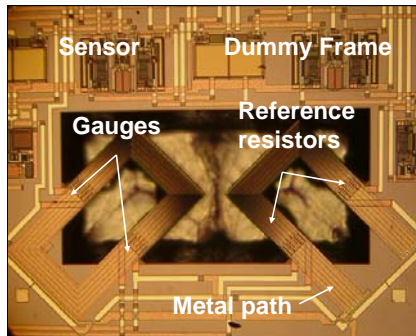


Fig. 7. The reference resistors are embedded in the dummy frame to cancel both thermal and mechanical offsets.

This sensor with its dummy frame has been characterized by electrical tests. The influence of power dissipated in the coil dissipation is reduced by 98%. No thermal influence of the gauges has been measured using the previous extraction method. It therefore becomes negligible in the overall mismatch. Finally, on 3 samples the remaining offset is found to be mainly caused by the CMOS process uncertainties on polysilicon resistors (90% at least). Table 1 gives a comparison of the sensor performances with and without dummy frame.

Table 1. Results summary (Dummy Frame)

	Surface	Power	Offset	PSRR
Without dummy	A	P	50 mV	-40 dB
With dummy	2×A	2×P	7,33 mV	-57,5 dB

Feedback circuit

The dummy structure dramatically improves the offset and power supply rejection ratio but is not practical in terms of surface and power costs. That is why a second solution is investigated. It makes use of a feedback circuit including a low-pass filter to bias the Wheatstone bridge through V_a and V_b (fig.8). By cancelling the offset, the supply noise is also rejected.

The main source of mismatch, using this closed-loop architecture, is caused by the equivalent input offset of the amplifier itself. Nevertheless, solutions exist to drop the offset down to 1mV. Thus, the cancellation of the mismatch can be improved. From simulation results, a PSRR of -73 dB can be expected.

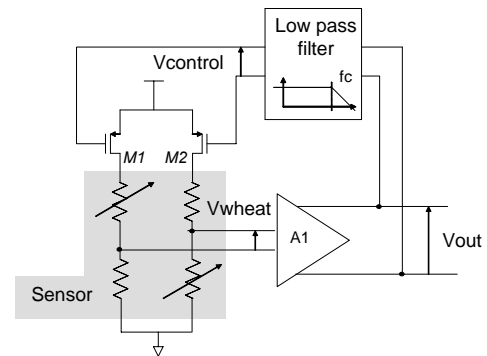


Fig. 8. Offset feedback to balance the Wheatstone bridge

CONCLUSION

The design of low-cost CMOS mechanical sensors usually involves piezoresistive suspended structures. Transduction is then realized using polysilicon resistors as gauges. In this paper, the mismatch between suspended resistors (i.e. gauges) and reference resistors is studied. Since this resistor mismatch causes both offset and poor noise rejection, design solutions are proposed to overcome those effects. The first solution, based on the use of a dummy frame, has been implemented. It cancels the mismatch due to micromachining but show limited performances because classical method for matching polysilicon resistance on a CMOS substrate cannot be used. A second method, based on feedback electronics, has been analysed. It offers better performances in terms of area but also in terms of efficiency. The offset can be reduced to the one of an amplifier stage.

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