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Automated Diagnosis and Probing Flow for Fast Fault Localization in IC

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Abstract

The continually increasing complexity of integrated circuits has made fault localization progressively more difficult. Despite significant improvements in test and diagnosis tools, probing is still required for acquiring new information and for confirming test results. For this reason, we have developed an optimized diagnosis-to-probing flow which significantly reduces the number of nodes to be probed and which dramatically cuts the cost of fault localization. With this approach, probing can be integrated in test and diagnosis operations to reach nodes which are known to be untestable.

1. Introduction

Fault localization is started at the test level. When testing is insufficient, diagnosis techniques are used to refine and extend the localization of potential candidates for fault origin(s). Finally, probing at the die level of one or more nodes may be required to remove remaining uncertainties. Probing can be very time consuming and requires a high level of knowledge of the die. This is why it is often used as a last resort.

To limit probing to only a few nodes and to benefit from this ability to reach otherwise unreachable nodes, we have developed a diagnosis flow (see Fig.1). From an initial Automatic Test Pattern Generation (ATPG) and datalog tester resulting from EWS (Electrical Wafer Sort), a first diagnosis is performed to create a list of potential failing nodes. To reduce this list of suspects, we specifically rerun ATPG to generate new patterns and to individually test each node of the list. The result (PASS/FAIL) is correlated with the sensitivity of the pattern on each net to eliminate certain candidates. If several candidates remain after the list has been maximally reduced with tester emulation and result comparisons, internal probing is used. Probing is used as an internal capability to bring new information back to the diagnosis flow. It makes it possible to converge faster with a higher degree of confidence on the researched fault. The result is compared to the correct value - obtained from simulations and the acquisition of new data is reused with diagnosis tools to generate a reduced new fault list. Probing can then be conducted on the final nets to discriminate equivalent faults in the netlist, such as the input and output of an inverter, which produce the same tester datalog. We will present the application of this diagnosis flow through a case study to highlight how probing can be coupled efficiently with ATPG to

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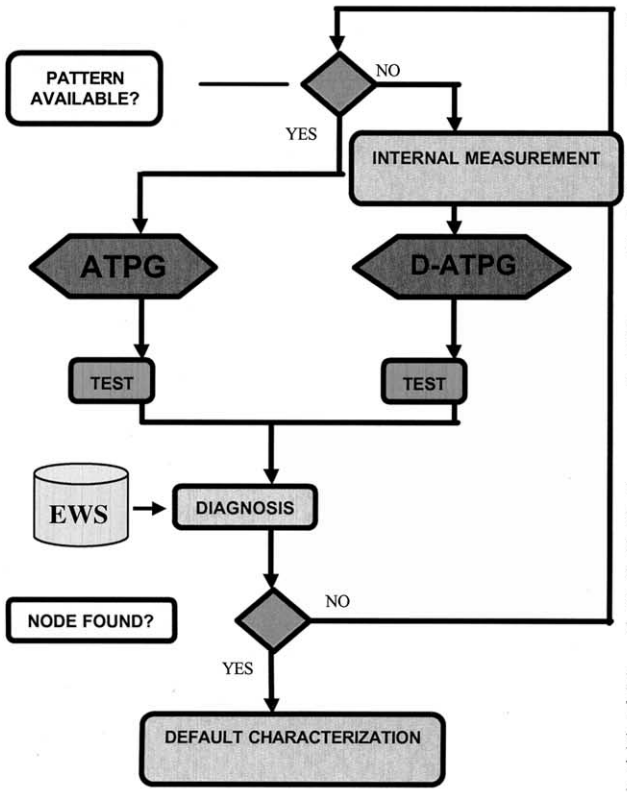

Fig. 1: The diagnosis flow: we generate patterns to localise the failing node with external test and internal measurement. D-ATPG stands for Diagnosis Automatic Test Pattern Generation

bring added testing and capabilities to specific nodes.

A second part of our paper will be focused on probing technique optimisation. The goal is to take into account the probing technique, the duration involved and node accessibility in order to reduce the time and cost of our diagnosis flow. To check signals from the front side on metal layers, frequently used techniques include mechanical and e-beam probing for node logic levels. Both techniques are fast. However, access to buried metal layers is more challenging and requires some preparation. The choice we have automated involves either probing a top metal layer which is a few gates after the node of interest or preparing the device (added time and cost) and probing the node directly if it is just to confirm that it is not the root cause of the failure.

2. Methodology

To optimise design modifications for probing, our strategy uses fault propagation in order to acquire equivalent signals on easier probing nodes. To do this, we convert signals to probes and generate new patterns to emulate a node and propagate its value.

The FIB (Focused Ion Beam) is put into the equation to create probe points on buried metal layers. To optimize FIB work we define the following approach:

Optimal FIB probe placement calculation

The goal is to predict the duration and difficulty of FIB probe points. A grade is calculated to assess the success rate and the cycle time. Questions that must be resolved before starting are: Is the FIB operation do-able, are the metal lines accessible (front side or backside), where is the optimal location, and what are the risk, time and cost involved?

Using the layout information, the equipotential line of each electrical node to be probe is extracted. The equipotential correspond to the series of polygons (e.g., rectangles of metal line) connected together between an output of a gate and the next input.

The next step is to extract the "accessible part", i.e., the part of a metal line which is not covered by above layers. At this point, if there is "accessible" metal, it means that the FIB probe point is possible.

To calculate the optimal placement, three parameters are used:

- Minimum separation α: The visible part of the buried metal line is reduced by a factor α due to the cone shaped ion beam and beam shift.
- Minimal line width β: A line is accessible if it size is larger than its factor β.
- Minimal distance between two lines λ: The proximity coefficient λ is used to filter out parts of the equipotential that are too close to other lines.

In addition to these parameters, the FIB time is calculated for the optimal probe point [REF 3].

When we add this optimized probing to our diagnosis flow, we can jump to the generated list of potential failed nodes. To measure signals by internal probing we follow our algorithm whose input is the

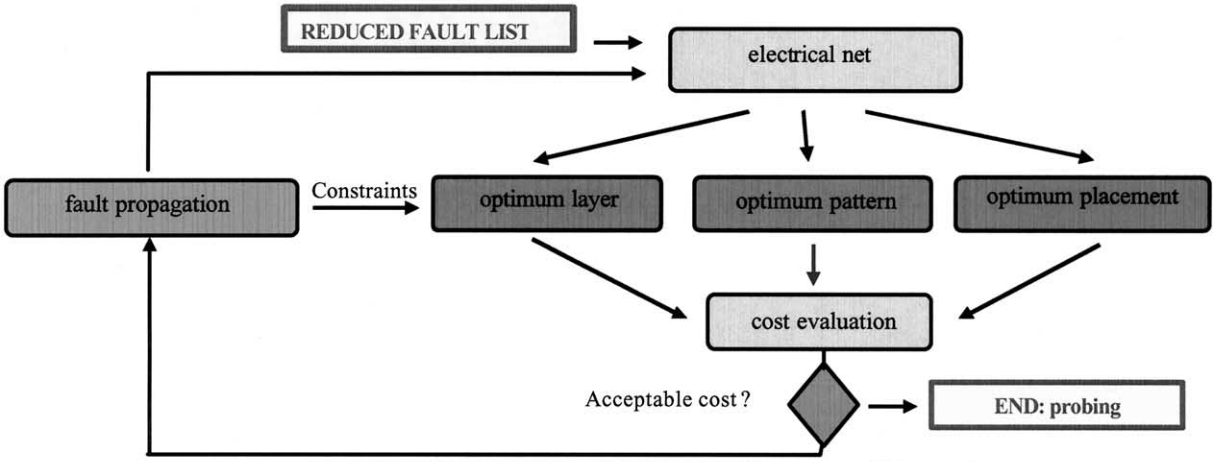

Fig.2: Proposed flow to define the best node to probe

node to be probed, extracted from the list, and whose output is the right or wrong status of the node. If the measured net has a different value from the simulation, we have identified the guilty net; otherwise, we reduce the fault list.

If the node to be probed is an upper metal level, the cycle time and the success rate are good. The design modification (by FIB) required for acquiring new information is quite cheap (in terms of time vs. success rate cost value). However, a node on a lower metal level is more difficult to reach because of its depth. This measurement is expensive because of a long cycle time and a low success rate in comparison with the first node. In this case, fault propagation is taken into account to measure the input value of a gate on the output of this gate.

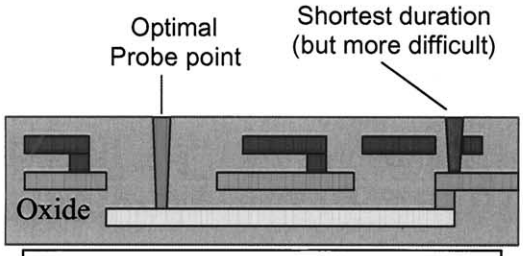

Fig.3: Optimal FIB probe point calculation. Proximity of nearby metal lines is taken into account to increase success rate of FIB operation while minimizing cycle time.

The algorithm proposed in Fig.2 takes the cost of a design modification, probing and pattern generation for extracting the optimised node to be probed into account (propagation can be performed through one or more logical gates).

This automated diagnosis and probing flow is made up with four major parts:

- The fault propagation: considering the schematic/netlist, we look for the logical gates involved by the electrical net we will propagate. We define the outputs relatives to these logical gates and the constraints to add and others inputs to correctly propagate the fault.
- The optimum layer: a script, which allows extracting the upper metal level of an electrical net: we enter the name of the net we want to analyse (during the design stage, this net is in fact several polygons) and thanks to navigation tools, we can determined the metal level of each polygon. By treatment, we define the upper metal level polygons.
- The optimum pattern: before the probing stage and for net emulation, we generate Diagnosis-ATPG patterns. We use commercial ATPG tools, but we just add in the fault list, the suspect net we want to probe; one pattern is generated ("0" forced on the net to check a "stuck-at 1" for example). In term of time, no difference between one pattern generation and an other one and for the success rate, it is binary: we succeeded (100%) or not (0%) to generate the pattern.

- The optimum placement: we define the best place to do the probe point taking into account the neighbourhood metal lines of the interesting electrical net

Mechanical and e-beam probing vs TRE probing

The approached we have presented in the above paragraph was first meant for front side IC investigation with mechanical and e-beam probing. With the increasing complexity of devices, Time Resolved Photon Emission (TRE) has open new capabilities. TRE can detect the faint emission coming from switching transistors, through the silicon backside. The advantage of TRE is to suppress any FIB work since transistors are probed instead of metal line.

With TRE, the cycle time can be very long for small technologies. With TRE acquisition, the device test pattern is looped in order to increase the chances of detecting photons from transistor commutations. Cycle time is calculated as a function of the number of commutation, the test pattern length and power supply V_{DD}. The success rate is more difficult to access. The two main factors are VDD and the minimal distance between two switching transistors λ for optimal probing. More detail on IC debug with TRE and circuit simulation can be found in [REF 5].

3. Experimental Results

The experiences have been done with a fully scanned design, a 0.18 micron technology with 6 metal levels. Two examples will be detailed to understand the benefit of this methodology.

3.1. Multiplexer

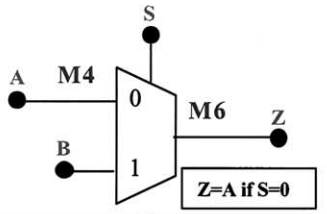

Fig.4: Fault propagation from "A" net to "Z" net with a constraint on "S" net.

From the ATPG and the datalog tester generated during EWS, a first result of diagnosis is obtained with a diagnosis tool: it gives us 4 candidates. To reduce this list of suspects, we generate new specifics patterns to retest individually each net; we succeeded to eliminate 2 suspects. The more probable suspect is the "A" net of a multiplexer. This net is in Metal4 and

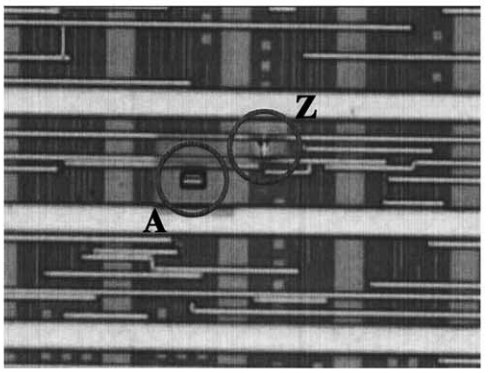

Fig 5: Optical view of FIB modifications in Metal4 / Metal6

considering the gate involved by this net, it is possible to propagate the "A" signal on the "Z" net; we just need to add a constraint on the Select input (to force his value to "0" in this case). The schematic Fig.4 shows the fault propagation.

The two probe points (see the optical view of the "A" and "Z" FIB modifications in Fig.5) have been done to compare the time requested for each one. The results are described in the table (Tab.1): to realize the probe point on "A" net, it takes 15minutes; the Metal4 was not covered by Metal5 and Metal6. For the output of the multiplexer, only 5minutes are needed with a higher success rate.

Following the proposed flow, from the reduced suspects list, the net we need to measure is the "A" input of a multiplexer. To do the probing, a pattern is available for emulation, the time requested is 15minutes with a quite good accessibility and a middle success rate. Starting from this data, we are propagating the signal on "Z" output of the multiplexer and we define the cost associated to this other possibility of probing: a pattern with a constraint on "S" can be generated, the time for this

FIB modification is 5minutes with a high accessibility and a high success rate. As the probing conditions are acceptable (Metal6, good accessibility), we go outside the loop and we can start the probing phase. In case of non-acceptable conditions, it is possible to propagate an other time the fault to find the best net to probe.

	Net A	*Net Z*
time	FIB 15min + ATPG	FIB 5min + ATPG
success	middle	high

Tab.1: Time and success rate of FIB modifications in Metal4 / Metal6

As a result of the algorithm, it is more profitable to probe the "Z" net instead of the "A". It allows to spare time and to have a higher success rate.

The probing of this net revealed a stuck-at 0 of the "A" net due to a particle, creating a short between this net and a ground line (Fig.6).

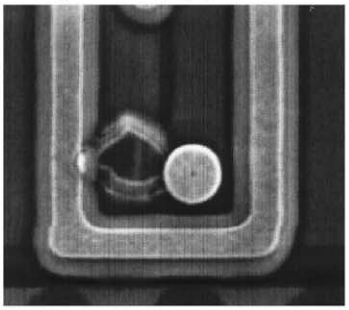

Fig.6: Scanning Electron Microscope image of the defect: a particle between two metal lines.

3.2. Inverter

For this second chip analysed, after the diagnosis tool and the fault list reduction three suspects needs to be probed to find the guilty net. One net of the reduced fault list is the input of an inverter. Considering the algorithm, the result of the optimum layer script is a Metal1 polygon as the higher metal level we can access. Although, the pattern generation is successful, the net is very difficult to reach (Metal1 covered by other layers, see Fig.8), it means the time to do the FIB modification is high and the success rate low.

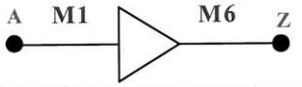

Fig.7: Fault propagation from "A" net to "Z" net of the inverter.

The fault propagation will help us because of the output inverter in Metal6 (schematic on Fig.7). The pattern generation is not requested: therefore the output signal is exactly the reverse as the input signal, the two patterns to emulate "A" and "Z" are identical. The probing on "Z" net is very benefit in this case.

	Net A	*Net Z*
time	FIB 90min + ATPG	FIB 5min + ATPG
success	low	high

Tab.2: Time and success rate of FIB modifications in Metal1 / Metal6

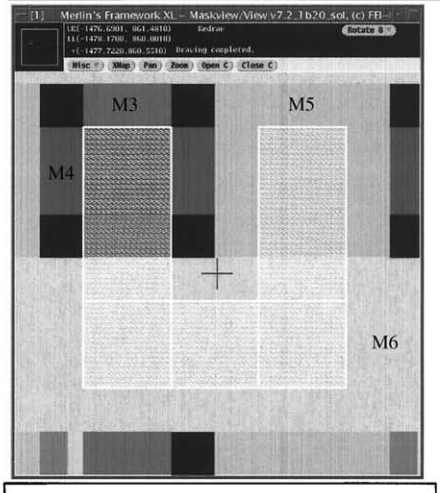

Fig.8: Layout view of the inverter input (net highlighted in Metal1)

The probing confirms the right value of this net. This suspect can be removed of the fault list. The guilty net is one of the two other nets, due to a defectivity problem.

Conclusion

We have presented an algorithm to optimize the probing. This algorithm determines the best net and the best place to probe and to check the logical value of an electrical net. To define it, the algorithm takes into account the pattern generation possibility, the higher metal level of the net and his accessibility (neighbourhood of the other nets). We can dramatically reduce the cost of probing, thanks to the signal propagation from one net to an other net, playing with logical gates and constraints.

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