March Tests Improvements for Address Decoder Open and Resistive Open Fault Detection

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Abstract

This paper presents a complete analysis of the ability of March tests to detect ADOFs (Address Decoder Open Faults) and resistive-ADOFs in address decoders of embedded-SRAMs. Such faults are the primary target of this study because they are notoriously hard-to-detect. With this study, we show that standard March tests without modifications are not able to detect them and we propose to translate the algorithm presented in [1, 2] into March elements. These new March elements involve a particular address sequence and data to be written.

1. Introduction

Embedded memories will continue to dominate the System-on-Chip silicon area in the next years. This is confirmed by the SIA Roadmap which forecasts a memory density of 94% in about ten years [3]. Consequently, memories will be the main responsible of the overall SoC yield. So, it is evident that efficient test solutions and repair schemes for memories need to be developed.

Generally, memory test algorithms such as March tests [4, 5] are employed to test the faults in memories. March algorithms are the most used because of their linear complexity and, among them, MATS++ and March C- [4, 6] are the most used in industry.

However, March tests are constructed essentially for static faults. In recent memory designs, a new class of faults appears to be more and more problematic to be detected. These faults are called dynamic faults [7, 8]. These are faults that can only be sensitized by performing more than one operation sequentially.

Among the known dynamic faults, we focus our study on those caused by open and resistive open defects which may occur in address decoders. So, we consider open defects that appear at transistor level and especially in the parallel plane of NAND/NOR gates. In presence of these defects two bit lines or word lines may be erroneously selected at the same time. This fault, also called ADOF (Address Decoder Open Fault), has been considered in [1, 2], where an algorithmic test solution is proposed. Other works have been proposed to study this type of fault [9, 10, 11] with March test solutions.

Recently, the ADOF problem has been considered from another point of view. In fact, in VDSM (Very Deep SubMicron) technologies, resistive open defects appear more and more common than pure open defects [12, 13]. In the following, we will consider resistive open defects in the parallel plane of transistors that involves what we call resistive-ADOFs. The presence of a resistive-ADOF produces a delay in the selection and deselection phases of word lines or bit lines.

In this paper, we analyze March tests ability for ADOFs and resistive-ADOFs detection in address decoders of

[*] This work has been partially funded by the French government under the framework of the MEDEA+ A503 "ASSOCIATE" European program.

embedded-SRAMs and we prove that standard March tests are not able to detect such faults. Test decomposition in sensitization and observation phases allows us to define required address sequence and data to be written in order to create new effective March elements based on the algorithm proposed in [1, 2]. These new March elements are able to detect all ADOFs and resistive-ADOFs without sensitization and observation problems and its complexity is much lower than the solution proposed in [1, 2].

The rest of the paper is organized as follows. Section 2 gives details about a classical address decoder implementation. Section 3 presents the ADOF and resistive-ADOF behavior. Section 4 provides the test conditions and electrical simulations for such fault models. New March elements allowing the detection of ADOFs and resistive-ADOFs are proposed in Section 5. Concluding remarks and future work are discussed in Section 6.

2. Basics and background

In the whole memory structure, we focus our attention on address decoders. Figure 1 depicts the scheme of a 2-bit wordline decoder. It is based on NOR-gates. NAND and inverter gates are present for synchronization and buffering respectively. A similar address decoder is used for bitline selection. Such a structure is used in the Infineon 0.13µm synchronous embedded-SRAM architecture.

We consider open and resistive open defects in this address decoder. When one of these defects appears between gates (inter-gate defect), a certain wordline is not selectable. This defect can be detected by March tests, like March C-, since it is equivalent to AF (Address decoder Fault) [9]. Thus, these kinds of open defects will not be considered in the following.

When the open defect is located inside the gate (intra-gate defect) and especially in the serial plane of the NOR-gates between the connections of the PMOS transistors (TP1 and TP2 in Figure 1), there is no pull-up of the NOR-gate output. When WLS0 (WordLine Selection 0) is addressed its activation does not occur. This effect is similar with the inter-gate defect. Thus, standard March tests are able to sensitize and detect this fault. In presence of a resistive open defect, there is a delay in the pull-up of the NOR-gate output and a consequent delay of the wordline selection. The test conditions are the same as before, but with additional timing constraints.

In the case of open defects placed in the parallel plane of NOR-gate transistors, dynamic faults appear. Referring to the NOR-gate of Figure 1, such a defect may be located at the drain, source or gate nodes of TN1 or TN2 transistors. As example, in Figure 1 we have inserted an open defect at the source node of TN2 transistor. This is an ADOF. In this architecture, the fault may produce an irregular behavior of the pull-down of the NOR-gate, thus preventing the correct deactivation of WLS0 due to a memory effect. In this case, two wordlines can be selected at the same time. So two memory cells are addressed during the same read or write operation. In presence of a resistive open defect, the NOR-gate pull-down presents a certain delay. We call this fault resistive-ADOF.

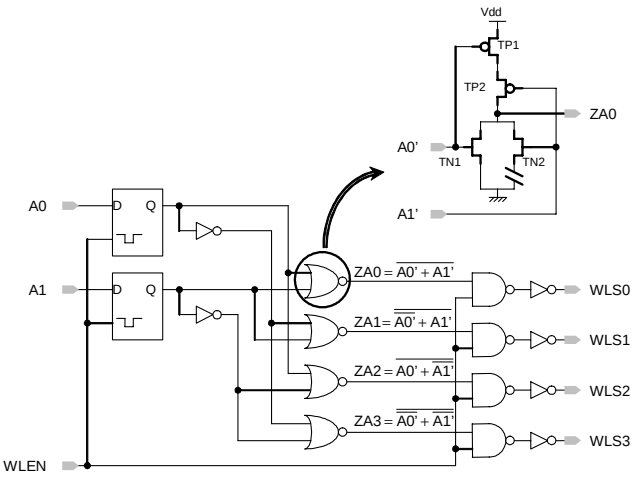

Figure 1: A NOR-based wordline address decoder

What stated above for NOR-based address decoders has the same validity for the complementary NAND-based architecture. In this case the parallel plane is placed in the pull-up path and the serial plane in the pull-down path. As for the NOR-based architecture, intra-gate faults show a sequential behavior when they are located in the parallel plane.

3. ADOFs and resistive-ADOFs behaviors

When it is fault free, the address decoder given in Figure 1, driven by signals A0 and A1, activates only one wordline at a time. For example:

1. <A0, A1> = <0, 0> ⇒ WLS0 is activated;
2. rising transition on A1: <A0, A1> = <0, 1> ⇒ WLS2 is activated and WLS0 is deactivated.

Now let us describe the sequential behavior of an ADOF. Consider the address decoder of Figure 1 with the open defect in TN2. The corresponding waveforms are shown in Figure 2. As already mentioned, the presence of an ADOF induces a wrong selection of two wordlines:

1. <A0, A1> = <0, 0> ⇒ WLS0 is activated;
2. rising transition on A1: <A0, A1> = <0, 1> ⇒ WLS2 is activated and WLS0 remains activated.

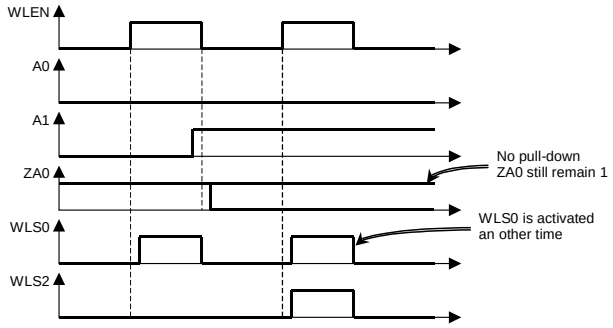

Figure 2: Waveforms of NOR-based address decoder with an ADOF

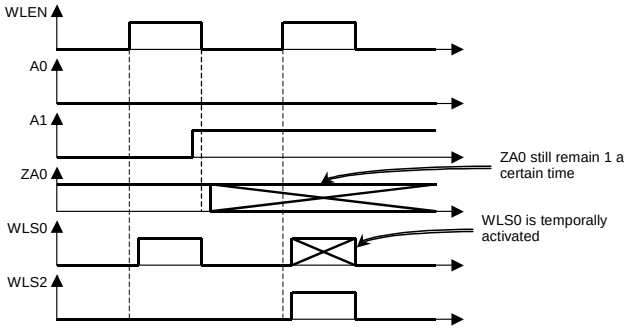

Figure 3: Waveforms of NOR-based address decoder with a resistive-ADOF

In this case, the open defect in TN2 prevents the pull-down of the ZA0 node, which remains at logic level high because of the memory effect (node and NAND input capacitances). In this example, we have first activated WLS0, (address <0, 0>) and then WLS2 (address <0, 1>). Between the two addresses only one-bit changes. This is required to sensitize the fault because a two-bit transition from <0, 0> to <1, 1> would activate both TN1 and TN2, thus discharging the node ZA0. So, WLS0 would be correctly deactivated in presence of the open defect because transistor TN1 would also be active, thus masking the faulty behavior of TN2. This shows that, in general, a test condition for this fault is to provide an address sequence with a Hamming distance of 1 (Hd = 1), *i.e.* each address has to present only a single-bit transition in comparison with the previous one.

The consequences on the entire address decoder structure are observable in Figure 3. After the input transition <A0, A1> = <0, 0> $\rightarrow$ <A0, A1> = <0, 1>, WLS2 is correctly activated, while WLS0 remains activated erroneously for a certain time due to the delay of the pull-down operation.

For resistive-ADOFs, three cases are possible:

1. **Large resistive open defect:** The circuit behaves as in presence of an ADOF. The delay in the deactivation of WLS0 is longer than the clock period, thus the two word lines are selected during the whole read or write phases.
2. **Intermediate resistive open defect:** The delay produced during the WLS0 deactivation is partial. So we have the correct activation of WLS2 and for a certain time the concomitant activation of WLS0. This time, there is a high probability that a dynamic fault occurs, with the same effects of an ADOF.
3. **Very small resistive open defect:** The delay perturbation introduced in the circuit is irrelevant and not pathological.

4. ADOFs and resistive-ADOFs detection

In this section, we analyze the ability of March tests to detect these faults. Standard March tests are not efficient for ADOFs and resistive-ADOFs testing. In order to improve March tests detection capability, it is required to use an address sequence with a Hamming distance of 1 [9]. This modification allows fault sensitization, but the fault effect cannot be observed because an undefined value is read on the memory output as illustrated beneath.

ADOFs have been considered in [1, 2], where an algorithmic solution is proposed that allows the correct sensitization and observation of all faults. This algorithm (Sachdev's algorithm) performs the following three phases:

a. "0" is written in a certain cell X;
b. "1" is written in a cell Y, whose address has Hd = 1 from cell X;
c. cell X is read; a "0" is expected.

The phases b and c are iterated n times, *i.e.* for all the cells whose address has Hd = 1 from cell X; n is the number of decoder inputs. In presence of an ADOF, during phase b, a "1" is written in cell Y, but cell X is selected at the same time and the stored "0" is overwritten with the opposite value. Phase c allows the fault observation. Thus, Sachdev's algorithm is effective for both sensitization and observation and its complexity is $(2n+1)x2^n$.

Moreover, in [14], it is shown that this algorithm can also be used for resistive-ADOFs detection. However, Sachdev's algorithm structure is very different from classic March tests and, when the objective is at-speed testing, a dedicated BIST implementation is required. As March tests are commonly used due to their linear complexity and effectiveness for detection of a large number of faults, it is advisable to use this technique for ADOFs and resistive-ADOFs detection. For this purpose, some modifications are required.

Some test conditions have been proposed in [16] in order to detect ADOFs and resistive-ADOFs by March tests. These conditions are the following ones:

> *For any open or resistive open defect in the parallel path of address decoder gates, all two-pattern sequences with Hd = 1 have to be applied. With this prerequisite, any March test effective to cover address decoder faults (AFs) will detect this fault [16].*

The condition on the address sequence (Hd = 1) can be satisfied by exploiting the first of the six Degrees of Freedom (DOF) [15]:

> **DOF I:** *Any arbitrary address sequence can be defined as a $\Uparrow$ sequence, as long as all addresses occur exactly once ($\Downarrow$ is the reverse of $\Uparrow$). The fault detection properties are independent of the utilized address sequence [15].*

The second condition, address decoder faults detection, is achieved by many March tests and among these, we consider March C- [6] as a case study. It has a 10N complexity, including the six March elements presented in Figure 4. Independently of the address sequence, March C- is also effective for SAFs (Stuck-At Faults), TFs (Transition Faults), CFins (Inversion Coupling Faults), CFids (Idempotent Coupling Faults) and SCFs (Static Coupling faults) detection [4].

$$\{\Updownarrow(w0)\ \Uparrow(r0,w1)\ \Uparrow(r1,w0)\ \Downarrow(r0,w1)\ \Downarrow(r1,w0)\ \Updownarrow(r0)\}$$
$$M_0 \quad M_1 \quad M_2 \quad M_3 \quad M_4 \quad M_5$$

Figure 4: March C- scheme

Now, we propose an analysis of the precedent statement with the NOR-based architecture (Figure 1) and we show that during the observation phase some problems appear. The observation phase is exploited during the second March element (M_1), when the ADOF involves a double addressing during the read operation as shown in Figure 5.

During M_1, for the first address, Ad0 <A0, A1> = <0, 0>, we have a correct behavior. A "0" is read and a "1" is written. For the following address, Ad1 <A0, A1> = <0, 1>, with only one bit transition, the r0 operation is performed and in presence of the defect (open or resistive open) the previous cell is also selected. Consequently, two different logic values, the "1" stored at Ad0 and the "0" stored at Ad1, are read on the same bitline (BL).

	Ad0	Ad1	Ad3	…
M_0	*w0*	*w0*	*w0*	…
M_1	*r0, w1*	*r0, w1*	*r0, w1*	…

Two opposite values are read at the same time

Figure 5: ADOFs detection with March C- (Address sequence with Hd = 1)

Electrical SPICE-based simulations have been performed on the 0.13 µm Infineon technology in order to evaluate this particular condition. Note that we consider a data detection limit of -/+ 80mV for ΔBL (ΔBL = BL - BLB), *i.e.* the minimal internal voltage difference allowing to perform a correct read operation. BL and BLB signals are the core cell outputs as depicted in Figure 6. Figure 7.a gives the comparison during the read "0" operation between Sachdev's algorithm and March C- test with an Hd = 1 address sequence. It is shown that Sachdev's algorithm (ΔBL(R0)_s), allows to detect the resistive open defect because a "1" is read instead of a "0" for a certain defect size (≈ 27kΩ). On the other hand, March test (ΔBL(R0)_m) presents an uncertain detection because an undefined value is obtained during the read operation for the same defect size. In Figure 7.b similar results are shown for a read "1" operation.

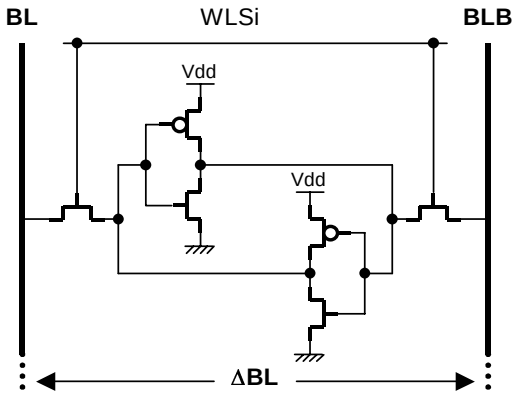

Figure 6: Memory core cell

In conclusion, Sachdev's algorithm is effective for the sensitization of ADOFs and resistive-ADOFs and it is effective for the observation if the delay exceeds the sensing phase of the write operation. With this algorithm the partial double addressing occurs during a write access. The same does not occur for the modified March C- test. This algorithm is effective for the sensitization, but the observation phase is problematic. The double cell access occurs during the read operation causing two opposite values to be driven on the same bit line. Thus, March

elements need to be adapted for ADOFs and resistive-ADOFs detection.

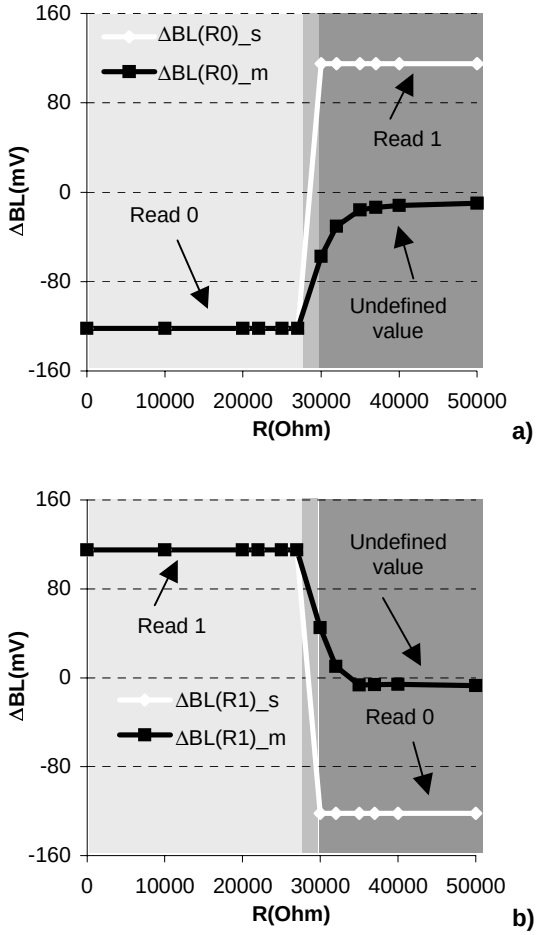

Figure 7: Sachdev's algorithm vs. March C-

5. New March elements for ADOFs and resistive-ADOFs detection

With March C-, in presence of ADOFs or resistive-ADOFs, the double addressing occurs during both write and read operations. As the same logic value "0" is written during the first March element M_0, the double addressing has no effect. On the other hand, the double addressing occurring during the read operation of the second March element M_1 leads to an uncertainty.

Therefore, for a proper detection it is necessary to sensitize the fault during the write operation and observe it during a separate read, as proposed by Sachdev. Thus, the proposed solution consists to translate the Sachdev's algorithm into March elements. The three phases of Sachdev's algorithm can be graphically illustrated as in Figure 8, where between Ad0 and Ad1 Hd = 1, d = data (0 or 1) and $\bar{d}$ its opposite value.

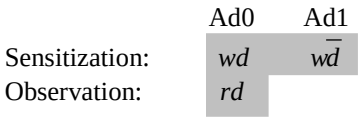

Figure 8: Sachdev's pattern

Now, we show how this pattern can be implemented by a March test. For this purpose, we can reiterate the Sachdev's pattern for all addressable cells, as shown in Figure 9. Instead of performing sensitization and observation for each cell, we can execute a sensitization phase at the same time for all the cells by a serial write operation with alternating data d and $\bar{d}$ followed by a global observation phase by reading the written data.

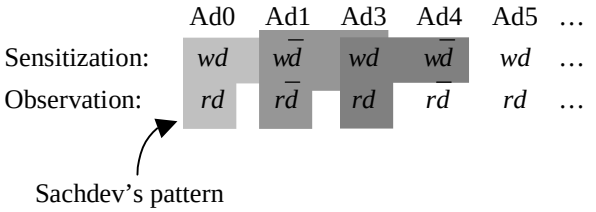

Figure 9: Sachdev's adaptation to March elements

This can be translated in the two March elements of Figure 10, where A is a logic value which starts from "0" or "1" and takes the opposite value for each new address. Moreover, the address sequence must have Hd = 1.

$$\{\Uparrow(wA)\ \Uparrow(rA)\}$$ A alternating logic value

M_A M_B

Figure 10: New March elements for ADOFs and resistive-ADOFs detection

The possibility to change the data value during the execution of a March element is justified by the fourth DOF of March tests [15]:

> **DOF IV:** *The data within a read/write operation does not necessarily has to be equivalent for all memory addresses as long as the detection probabilities of basic faults are not affected [15].*

In order to ensure that the proposed March elements cover all the ADOFs and resistive-ADOFs, it is necessary that the sequence of 2^m produced addresses (where m is the total number of address bits) contains all the $nx2^n$ single-bit transitions (where n is the bit-width of the considered

decoder) [9]. In other words, the necessary condition for complete detection is the following one:

$$2^m \geq n \times 2^n + 1 \quad (1)$$

Remember that we considered a bit oriented SRAM memory which uses two decoders (wordline and bitline decoder). If this condition is not satisfied, it is necessary to add two other similar March elements with the reverse address sequence, that implies the presence of the opposite single-bit transitions. However, this condition (Eq. 1) is most of the time satisfied as for the considered Infineon memory structure.

The validation of the proposed March elements is observable by the waveforms of Figure 7. During the test operation of the new March elements, the electrical behavior of the memory circuit is similar to Sachdev's algorithm simulation. The double addressing, due to the ADOF, occurs during the write operation (sensitization phase). The observation phase is done during the read operation without uncertainty because there is not double addressing with opposite data as before.

Finally, the test complexity obtained with our new March elements is $(2n) \times 2^n$ for an n-cell memory compared to $(2n+1) \times 2^n$ for the Sachdev's algorithm. Moreover, for a BIST implementation, the Sachdev's algorithm requires a dedicated address generator which cannot be used by March tests. Our solution is more attractive because the same address generator can be used for our March elements and an additional March test.

6. Conclusions

The presented study has focused on dynamic faults that may occur in address decoders of memories. In particular, we have proposed a new test solution for ADOFs and their generalization, resistive-ADOFs.

Electrical analysis of March tests has shown that ADOFs and resistive-ADOFs can be detected only when the sensitization phase involves a double addressing during the write operation. For this purpose, we have exploited some Degrees of Freedom of the March tests (DOF I and IV) in order to generate new March elements for ADOFs detection. Compared to the previous March solutions, these new March elements ensure the fault observation.

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