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Abstract: *This paper presents an analysis of dynamic faults in core-cell of SRAM memories. These faults are the consequence of resistive-open defects that appear more frequently in VDSM technologies. In particular, the study concentrates on those defects that generate dynamic Read Destructive Faults, dRDFs. In this paper, we demonstrate that read or write operations on a cell involve a stress on the other cells of the same word line. This stress, called Read Equivalent Stress (RES), has the same effect than a read operation. On this basis, we propose to modify the well known March C-, which does not detect dRDFs, into a new version able to detect them. This is obtained by changing its addressing order with the purpose of producing the maximal number of RES. This modification does not change the complexity of the algorithm and its capability to detect the former target faults.*

Keywords: Memory testing, SRAM core-cell, dynamic faults, resistive-open defects, March test.

Proposed Topic: Memory Test.

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Abstract

This paper presents an analysis of dynamic faults in core-cell of SRAM memories. These faults are the consequence of resistive-open defects that appear more frequently in VDSM technologies. In particular, the study concentrates on those defects that generate dynamic Read Destructive Faults, dRDFs. In this paper, we demonstrate that read or write operations on a cell involve a stress on the other cells of the same word line. This stress, called Read Equivalent Stress (RES), has the same effect than a read operation. On this basis, we propose to modify the well known March C-, which does not detect dRDFs, into a new version able to detect them. This is obtained by changing its addressing order with the purpose of producing the maximal number of RES. This modification does not change the complexity of the algorithm and its capability to detect the former target faults.

1 Introduction

Embedded memories will continue to dominate the System-on-Chip silicon area in the next years. This is confirmed by the SIA Roadmap which forecasts a memory density approaching 94% in about ten years [1]. Consequently, memories will be the main responsible of the overall System-on-Chip yield. It therefore becomes evident that the development of efficient test solutions and repair schemes for memories are essential.

Memory test solutions are mostly oriented to static fault detection. These faults are sensitized by only one operation. Recent works show that VDSM (Very Deep Sub-Micron) technologies more frequently involve dynamic faults [2, 3]. They can be sensitized only by performing more than one operation in sequence and traditional tests are not made to detect them [4].

Among the known dynamic faults that may affect SRAM memories, we concentrate on those that concern the core-cell. One of these faults is the dynamic Read Destructive Fault (dRDF) [2]. It has the following behavior: a write operation immediately followed by a read operation causes the flip of the logic value stored in the cell. So, such a fault requires a specific read/write sequence to be detected.

Recently, a test solution, referred as March RAW (Read After Write) [5], has been proposed to detect all single-cell dynamic faults in core-cells. Its complexity is 13N including the initialization. This algorithm detects dRDFs by March elements that perform a write operation followed by a read operation, *e.g.* 1w0r0. It has been shown in [6] that this test can be improved by applying the sequence of operations $1w0r0^M$, where $r0^M$ denotes a sequence of M successive r0 operations, e.g. $1w0r0^2$ = 1w0r0r0. In this case, multiple read operations are performed after the write operation, allowing a more efficient fault detection. However, if a large number of read operations is needed, the test complexity increases drastically.

In this paper we propose a more efficient alternative to March RAW. Without increasing its complexity, we improve the standard March C- algorithm (10N complexity) [7, 8] in order to make it able to detect also dynamic faults in the core-cell. Our modified March C- detects dRDFs by using a particular addressing sequence.

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This modification is allowed by the first of the six Degrees of Freedom (DOF) [9] of March tests, and does not alter the capability to detect the former target faults.

Multiple read operations after a write operation can be achieved by the March C- (with the address modification) for the following reason: during a read or write operation the pre-charge circuit is turned off in the selected column; the others columns have the pre-charge left on. Consequently, all the cells on the same word line of the selected cell fight against the pre-charge circuit. In this paper we show that this event, that we call Read Equivalent Stress (RES), is equivalent to a read operation for the non-selected cells. In other word, a read or write operation on a certain cell involves a stress (RES) on the other cells of the same row. This phenomenon can be used for dynamic fault sensitization.

The rest of the paper is organized as follows. Section 2 gives an overview of our study presented in [6] with the defect insertion in the core-cell. Section 3 provides explanations and electrical simulations of the RES. In Section 4, a March test solution is presented. Concluding remarks and future works are given in Section 5.

2 Dynamic faults in the core-cell

In this section we synthesize the main results of our previous study in core-cell faulty behavior [6]. This study was oriented to the characterization of some faults induced by the injection of resistive-open defects in the core-cell of an SRAM memory core-cell. Figure 1 depicts the scheme of a standard 6-transitors cell where six different resistive-open defects have been placed. The defects are not injected into all possible locations due to the symmetry of the structure.

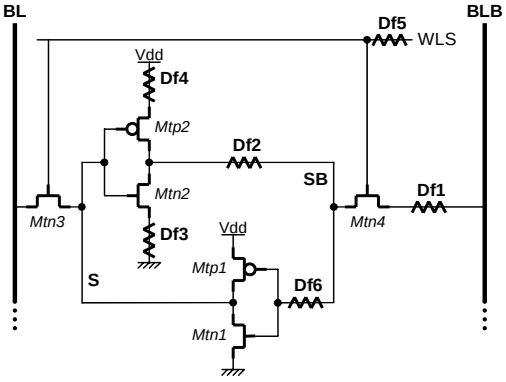

Figure 1: Resistive-open defects injected into the memory core-cell

The whole operating environment range has been selected in order to maximize the fault detection probability. Hence simulations have been performed by the variation of the following parameters:

- Process corner: slow, typical, fast
- Supply voltage: 1.35V, 1.5V, 1.6V
- Temperature: - 40°C, 27°C, 125°C
- Resistance values have been chosen from few Ωs up to several MΩs since a large range of possible values have been reported [10].

In the following, the most significant simulation results are presented, with particular emphasis on dynamic fault models. Table 1 shows a summary of the fault models identified for each injected resistive-open defect, according to the conditions which maximize the fault detection, *i.e.* the minimum detectable resistance value. The faults have been detected by 1w0r0 or 0w1r1 sequences.

Dfi	Process corner	Voltage (V)	Temp (°C)	Min Res (kΩ)	Fault Model
1	Fast	1.6	-40	~25	TF
2	Fast	1.6	-	~8	RDF DRDF
3	Fast	1.6	125	~3	RDF DRDF
4	**Fast**	**1.6**	**125**	**~130**	**dRDF**
5	Fast	1.6	-40	100/140	IRF/TF
6	Fast	1.6	125	~2 M	TF

Table 1: Summary of worst-case PVT corners for the defects of Figure 1 and corresponding minimum detected resistance and fault models [6]

Definitions of the fault models reported in Table 1 are the following ones:

- Transition Fault (TF): *A cell is said to have a TF if it fails to undergo a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written.*
- Read Destructive Fault (RDF) [11]: *A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output.*
- dynamic Read Destructive Fault (dRDF) [2, 5]: *A cell is said to have an dRDF if a write operation **immediately** followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output.*
- Deceptive Read Destructive Fault (DRDF) [11]: *A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell.*
- Incorrect Read Fault (IRF): *A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell.*

On the bases of these results, a dynamic Read Destructive Fault (dRDF) occurs in presence of Df4. This fault is detectable by a read after write operation. However, in case of a little defect size, multiple read operations are needed. This statement is confirmed by the

waveforms presented in Figure 2 which shows that a sequence of five r0 operations, is needed to detect the fault carried by a 1.5 MΩ resistance defect.

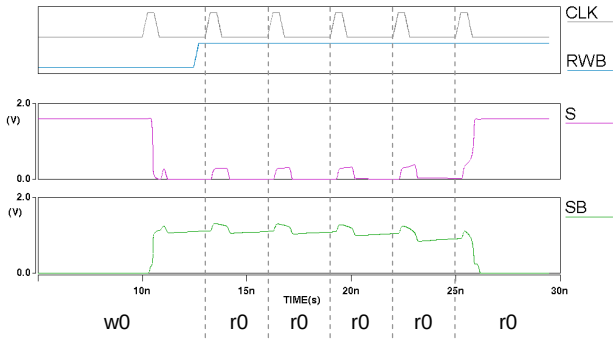

Figure 2: A destructive read occurring after the 5th consecutive r0 operation
(typical process, T=125°C, V=1.6V, T_{cyc}=3ns, R=1.5MΩ)

In general, the dependence of dRDF has been studied in relation to the cycle time and the defect size. The results are presented in the graph of Figure 3 where each point corresponds to a determined couple (cycle time, defect size) and is placed in a certain area corresponding to a sensitization sequence like $1w0(r0)^M$, where M = 1 to 5.

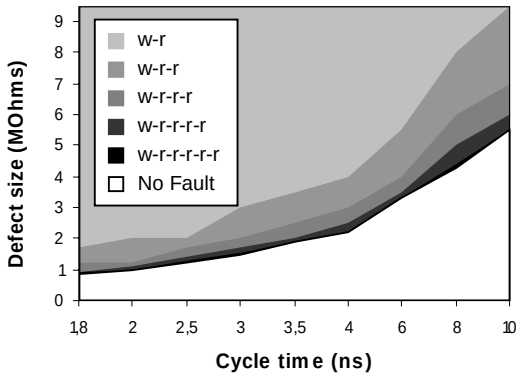

Figure 3: Fault detection as a function of the cycle time and defect size (typical process, T=125°C, V=1.6V)

It should be observed that the minimal detected resistance value depends on the cycle time. The fault detection is two times more effective when we pass from 1w0r0 to $1w0r0^5$.

3 Read Equivalent Stress

In the previous section it has been shown that a dRDF can be the consequence of resistive-open defects in the core cell of SRAMs. In particular it has been empathized that in presence of the resistive-open defect Df4 depicted in Figure 1, the action of single or multiple read immediately after a write operation may cause the inversion of the value stored in the cell. In this section, we show that a cell can undergo a stress equivalent to a read operation (Read Equivalent Stress, RES) when a read/write operation is performed on other cells of the same word line. Moreover, we demonstrate that RESs are more effective to sensitize dRDFs than read operations.

For this purpose, it is useful to remember that when a cell is selected for a read or write operation the pre-charge circuit is normally turned off in its bit line. For the bit lines that are not involved in the operation, the pre-charge circuit is commonly left on. With the pre-charge active and the word line being high on the unselected columns, the cells fight against the pre-charge circuit. A consequent deduction is that the stress produced by a read operation on a cell is equivalent to the stress caused by a read or write operation performed on whatever cell on the same word line. It is also possible that in the latter case the stress is larger. In fact, during a read action the perturbation of the cell is produced by the charge stored previously on its two bit lines, while in the other case the cell is stressed by the same bit line charge, but with the pre-charge circuit still on. In order to simplify what exposed above we produce the example referred to the scheme in Figure 4.

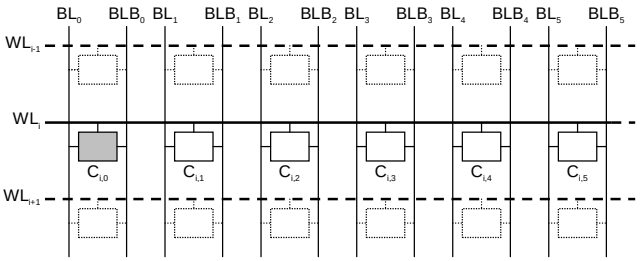

Figure 4: A portion of an SRAM block

This scheme depicts a section of an SRAM block, and in particular in the middle there are the first six cells of the word line WL_i. We assume that on WL_i the first cell on the left $C_{i,0}$ is affected by a resistive-open defect in the pull-up transistor of one of the two inverter (as Df4 in Figure 1). This defect may cause a dRDF. This fault is detectable when, immediately after a write data on cell $C_{i,0}$, one or multiple read operations are performed on the same cell. An equivalent faulty behavior can also occur when the write data in cell $C_{i,0}$ is followed by read or write operations on the other cells of the same world line. This is possible because, if for example cell $C_{i,1}$ is selected, the pass transistors (Mnt3 and Mnt4 in Figure 1) of all the cells on the same word line, in particular the faulty cell $C_{i,0}$, are saturated. So, $C_{i,0}$ fights against the pre-charge circuit that is in on state as for all the non-selected columns. Consequently, the faulty cell $C_{i,0}$ undergoes a stress (RES) similar to a read operation.

In order to give a formal confirmation to the previous assumptions and assertions, electrical simulations have been performed on Infineon 0.13µm embedded-SRAM family with the Infineon internal SPICE-like simulator. It has been considered a reference 8kx32 memory, organized as an array of 512 word lines x 512 bit lines. The cell array of this memory is split in 128 blocks. When a word line is

selected all the 512 cells on this word line are connected to respective bit lines. The bit line selection is performed by a pre-decoder, that selects a column for each block (for example the first column of each block), followed by different lines of multiplexers.

In Figure 5 there is an example of a two-block SRAM with the column decoding made by a pre-decoder and multiplexers. Consequently, when a read operation is done on a cell, it is actually performed on all the correspondent cells for each block, and after, there is a further selection made by multiplexers. Thus in the considered Infineon architecture, when a cell is selected to be read or written, 512 cells are contemporarily selected because they are on the same word line. For 128 of them the pre-charge circuit is off, because they are in the same position of the selected cell in the different blocks. In term of stress for each read or write operation there are128 cells with a actual read stress, because they are selected by word line and bit lines, and 384 (= 512-128) cells that undergo a RES, because they are selected only by the world line signal.

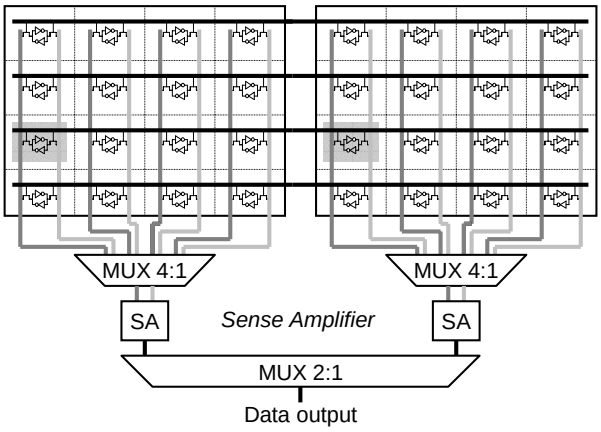

Figure 5: Scheme of a two-block SRAM memory

The simulations have been performed to estimate and confront the stresses produced in the following situations:

a. On the faulty cell a w0 operation is performed, immediately followed by one r0 operation.
b. On the faulty cell a w0 operation is done, immediately followed by read (b_1) or write (b_2) operations on the cells placed on the same word line.
c. On the faulty cell a w0 operation is performed, immediately followed by read or write operations on the cells on the same word line, but placed in other blocks in the same position of the faulty cell (highlighted cells in Figure 5).

The waveforms in Figure 6 refer to the electrical simulations made with the previous conditions in the case of a faulty cell, where the defect Df4 is present and has a size of 1.4 MΩ. The waveforms in Figure 6.a represent the control signals; CLK, RWB which is the read/write selection, and the word line and bit line enable signals (WLEN0, WLEN1 and BLEN0). The voltage values of S and SB nodes (see core cell presented in Figure 1) are reported in Figure 6.b, for the comparison of case a and b (b_1 and b_2) and in Figure 6.c for a comparison between cases a, b_1 and c. These waveforms show that after a w0 operation the fault free inverter of the cell has its output (node S) normally switched to '0' logic, that is an effective electrical 0V. The other inverter has its output switched to '1' logic, that does not correspond to an exact Vdd value, due to the delay effect involved by defect Df4.

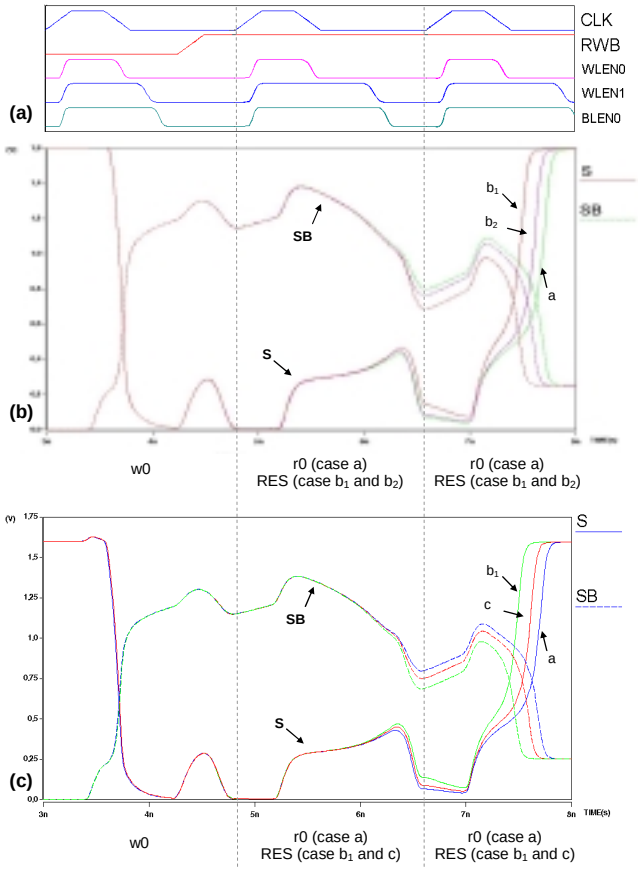

Figure 6: Waveforms of simulations

In all cases a, b and c, the disturb operations performed immediately after the w0 made on the same cell or in other cells of the same word line, produce an abnormal swap of the faulty cell after two cycles. This is a confirmation of the assumptions proposed at the beginning of this section, *i.e.* the effects produced by the read equivalent stress in term of sensitization of dRDF are very similar to actual read stresses. In fact, in both graphs (Figure 6.a and 6.b) the waveforms show different cases of RES (b_1, b_2 and c) which are very similar to a read after write (case a).

Considering Figure 6.b, it can also be observed that in case of read operation the word line enable signal is on for a period a little bit longer than for the write operation. This involves that b_1 produces a more prolonged stress. In fact, the cell swaps before.

Now we evaluate the RES in terms of sensitization performance. For this purpose, parametrical simulations have been made with different cycle time and with a reasonable resistive range for the size of the resistive-open defect Df4 on the Infineon SRAM memory structure. The results, summarized on the graph of Figure 7 are referred only to case b_1. These results are clearly very similar to those shown in Figure 3 that refer to the read after write method. The analysis of the two graphs of Figure 3 and Figure 7 also confirms that the sensitization effect of the RESs is higher than that produced by read operations on the faulty cell.

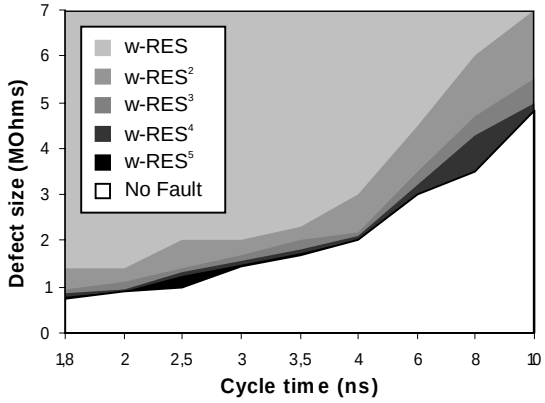

Figure 7: Fault detection as a function of the cycle time, defect size and RES (typical process, T=125°C, V=1.6V)

In order to highlight the higher efficacy of RESs for sensitization of dRDF, we propose in Table 2 the results of read after write operations and RESs.

	cycle time (ns)	1.8	2	2.5	3	3.5	4	6	8	10
Minimal resistance size, MOhm	w-r	1.7	2	2	3	3.5	4	5.5	8	9.5
	w-RES	1.4	1.4	2	2	2.3	3	4.5	6	7
	w-r^2	1.2	1.2	1.7	2	2.5	3	4	6	7
	w-RES^2	0.95	1.1	1.4	1.7	2	2.2	3.5	4.7	5.5
	w-r^3	0.95	1.1	1.4	1.7	2	**2.5**	3.5	5	6
	w-RES^3	0.85	0.95	1.3	1.55	1.8	**2.1**	3.2	4.3	5
	w-r^4	0.9	1	1.3	1.55	1.9	2.2	3.3	4.4	5.5
	w-RES^4	0.8	0.9	1.22	1.5	1.75	2	3	3.5	4.8
	w-r^5	0.85	1	1.25	1.5	1.9	2.2	3.3	4.3	5.5
	w-RES^5	0.8	0.9	1.22	1.5	1.75	2	3	3.5	4.8

Table 2: Comparison between read after write and RES

In Table 2, the values represent the size of defects that lead to dRDFs. These values are the minimal ones sensitized by read after write operations (w-r^M) or RESs (w-RES^M) for different cycle time. For example, for the cycle time 4 ns, the sequence w-r^3 sensitizes a dRDF, consequent to a minimal defect size of 2.5 MΩ, while in same conditions, w-RES^3 allows to sensitize dRDF involved by a 2.1 MΩ defect. In other words, RES is more effective than read after write operation because it can sensitize dRDFs due to a smaller resistive defect.

4 March test solutions for dRDF testing

In this section we use the results presented above in order to produce an efficient test for dRDF detection. Among the various types of algorithm we choose March test that allows to reach a good effectiveness among with of its small complexity. For this purpose, our March test has to have some requirements.

i. It is necessary that the read/write operations are performed with a particular addressing order with the purpose to execute the March elements on the memory array by acting on word line after word line. This is necessary because the RESs are produced only by operating on the cells of the same word line. For example, let us consider again the Infineon 0.13µm embedded-SRAM architecture. The read and write operations of the March elements have to be operated firstly on all the 512 cells of the first word line, then on the 512 cells of the second word line, and so on.

ii. The elements of our March test have to include w0 operations, necessary for sensitization, and r0 necessary for observation.

iii. Additional elements with w1 and r1 are needed in order to detect similar faults generated by resistive-open defects placed symmetrically in reference with Df4 (see Figure 1).

iv. All the elements, in particular the sensitization ones, need to be performed in ⇑ and ⇓ sequence.

The last statement is based on some considerations. For example we still use the same Infineon SRAM architecture. If the faulty cell is $C_{i\,0}$, the first cell of the ith word line, an element like ⇑w0 operates a w0 on this cell and is immediately followed by w0 operations performed on the following 511 cells of the same word line. These w0 operations imply 511 RESs on the faulty cell. If the faulty cell is the second one, $C_{i\,1}$, the same March element ⇑w0 involves 510 RESs on the faulty cell. In case the defective cell is the last of its word line the element ⇑w0 involves any RES on it. The introduction of ⇓ elements allows that the sensitization phase is performed with the opposite addressing sense of the word line. In these conditions the cells that endure the maximum number of RESs are those placed in the extremes of the word line, while those placed in the middle of the word line undergo the smallest number of RESs, *i.e.* 512/2=256 of RESs. In general if *nb_cell* is the number of cells of each word line and *nb_op* the number of operations (read/write) of the March element (⇑w0 → *nb_op*=1; ⇑r1w0 → *nb_op*=2), the maximum number of RESs that a cell undergoes is:

$$RES_{max} = (nb\_cell - 1) \times nb\_op$$

and the minimum one is:

$$RES_{min} = (nb\_cell \times nb\_op) / 2$$

This is illustrated in Figure 9, where the color of cells is darker if they endure a higher number of RESs.

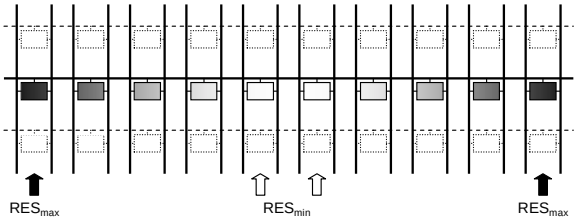

Figure 9: Distribution of RESs on a word line with the modified March C-

Now we propose a modification of known March tests, which have the characteristics exposed above, with the objective to detect dRDFs. For this purpose, we consider the well known March C-. This is a 10N linear test, which is effective to detect stuck-at, transition and 2-coupling faults and that normally cover 0% of dRDFs [5]. March C- has the structure shown in Figure 8.

$$\{\Updownarrow(w0)\ \Uparrow(r0,w1)\ \Uparrow(r1,w0)\ \Downarrow(r0,w1)\ \Downarrow(r1,w0)\ \Updownarrow(r0)\}$$
$$M_0 \quad M_1 \quad M_2 \quad M_3 \quad M_4 \quad M_5$$

Figure 8: March C- structure

We can observe that the first five elements (M_0 up to M_4) could be effective for dRDF sensitization because they contain the w0 or w1 operation. In these elements the read operations are useful for the observation, but they also contribute to sensitization. Both $\Uparrow$ and $\Downarrow$ sequences are operated allowing a good detection for all the cells.

The modification, which makes March C- able to detect dRDFs, consists in the use of the particular address sequence word line after word line. Due to the first of the six degrees of freedom [9] of March tests, this modification does not change the capability of March C- to detect the former target faults.

Now we evaluate the modified March C- in reference to the Infineon SRAM structure. If a faulty cell $C_{i\,0}$ is the first cell of the word line i, the element M_2 operates a w0 on this cell followed by a r1 and a w0 on the following 511 cells of the same word line. This means 2x511=1022 RESs on the faulty cell. The same happens if the faulty cell is $C_{i\,511}$, the last cell of word line i, and the element M_4, that is M_2 with inversed address order, operates a w0 and 1022 RESs on $C_{i\,511}$. So, $C_{i\,0}$ and $C_{i\,511}$ endure the maximum number of RESs because they placed in the extremes of the word line. Those placed in the middle of the word line are the less stressed with 2x(512/2)=512 RESs. Moreover the elements M_1, as its homologue M_3, allows the test of similar faults due to resistive-open defects symmetrically placed in reference with Df4.

The proposed March test solution presents many advantages as its linear complexity and the reutilization of an already existing March test. The main benefit is the high efficiency to detect dRDFs in comparison with read after write test. In fact, in order to reach the same effectiveness, a RAW test should include a very large number of read operations increasing dramatically its complexity.

5 Concluding remarks and future works

The present study has focused on dynamic faults that may occur in core-cells of SRAM memories. In particular, we have focused our attention on dynamic Read Destructive Faults.

We have shown that a cell undergoes a stress equivalent to a read operation, when a read/write operation is performed on a cell of the same word line. We have called this phenomenon Read Equivalent Stress (RES), and shown that they are more efficient than read after write. On these bases, we have modified the March C- to make it able to detect dRDFs, without changing its complexity and capabilities.

We intend to prosecute this study by analyzing the capability of RES to sensitize all the other dynamic faults in core cells.

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