Resistive-Open Defects in Embedded-SRAM Core Cells: Analysis and March Test Solution

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Keywords: SRAM core-cell, resistive-open defects, delay faults, dynamic faults, March test.

Proposed Topic: Memory testing.

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Proposed to
13th Asian Test Symposium
Caesar Park Hotel, Kenting, Taiwan
November 15-17, 2004

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Abstract

In this paper we present an exhaustive analysis of resistive-open defect in core-cell of SRAM memories. These defects that appear more frequently in VDSM technologies induce a modification of the timing within the memory (delay faults). Among the faults induce by such resistive-open defects there are static and dynamic Read Destructive Fault (RDF), Deceptive Read Destructive Fault (DRDF), Incorrect Read Fault (IRF) and Transition Fault (TF). Each of them requires specific test conditions and different kind of March tests are needed to cover all these faults (TF, RDF, DRDF and IRF). In this paper, we show that a unique March test solution can ensure the complete coverage of all the faults induced by the resistive-open defects in the SRAM core-cells. This solution simplifies considerably the problem of delay fault testing in this part of SRAM memories.

1 Introduction

The importance of producing efficient tests for memories is crucial; this fact has been put in evidence by the SIA Roadmap which forecasts a memory density approaching 94% of System on Chip (SoC) silicon area in about ten years [1]. Consequently memories are becoming the main responsible of the overall System-on-Chip yield.

Functional fault models, traditionally employed in RAM testing such as stuck-at, transition and coupling faults [2], are nowadays insufficient for the effects produced by some defects that may occur in VDSM technologies. Improvements in manufacturing process density and memory architecture have carried the development of new fault models, which are tightly linked to the internal memory structure [3, 4, 5, 6, 7, 8]. These faults are not directly detectable with most of standard March algorithms and thus need specific test sequences and, in some cases, at-speed tests which are necessary especially for delay fault detection.

Many links have been established between delay faults and resistive-open defects [9, 10]. Resistive-opens generally cause timing-dependent faults. A two-pattern sequence is usually necessary to sensitize the fault, but, unlike stuck-open faults, detection of resistive-opens often needs to be performed at-speed.

The significance of resistive-open defects has considerably increased in recent technologies, due to the presence of many interconnection layers and an ever-growing number of connections between each layer. In particular in [11] Intel reports that open/resistive vias are the most common root cause of test escapes in deep-submicron technologies. Hence resistive-open defects are the main target of this study. Resistive defects have been injected in the core-cell of the Infineon 0.13µm synchronous embedded-SRAM family. For each defect location, electrical simulations have been performed with

[*] This work has been partially funded by the French government under the framework of the MEDEA+ A503 "Associate" European program.

many parameters such as defect size, supply voltage, operating temperature and process corner.

In this paper we report some results that demonstrate the sensitivity of embedded SRAM core-cells to resistive-open defects and we provide a characterization of these defects in terms of fault models. These faults are Read Destructive Fault (RDF) static [4] and dynamic [12, 13], Deceptive Read Destructive Fault (DRDF) [4], Incorrect Read Fault (IRF) and Transition Fault (TF). Each of them requires specific test conditions to be detected. Different March tests are able to cover the static faults (RDF, DRDF, IRF and TF). On the other hand, the dRDF (dynamic RDF) is not tested by standard March tests [13] but can be detected by a modified March C-. We have proposed and described in details this modified March test in [14].

In this paper, we show that this single March test is able to detect exhaustively all the faults induced by resistive-open defects in the core-cell. This solution does not increase the complexity of the standard March C- (10N) [15, 16]. Our modification makes it able to detect not only dRDFs but also all the core-cell static faults (RDFs, DRDFs, IRFs and TFs). Our modified March C- detects dRDFs by using a particular addressing sequence allowed by the first of the six Degrees of Freedom (DOF) [17] of March tests. This modification induces, on the core-cells, the occurrence of stresses that are equivalent to the application of multiple read operations which are required for dRDF detection [14].

The rest of the paper is organized as follows. In the following section 2, the experiments are described, whereas Section 3 deals with the test procedures allowing the complete detection of all resistive-open defects in the core-cell. Concluding remarks are given in Section 5.

2 Experiments

2.1 Experimental conditions

Several resistive-open defects have been analyzed in the memory core-cell. Figure 1 depicts the scheme of a standard 6-transitors cell with six different resistive-open defects. Due to the symmetry of the structure these six locations allow an exhaustive analysis of the resistive-open defect within the core-cell structure.

Electrical simulations of these defects have been performed with the Infineon internal SPICE-like simulator. A reference 8Kx32 memory block has been considered, organized as an array of 512 word lines x 512 bit lines. In order to reduce the simulation time, the simulations have been performed on a simplified version of the memory circuit that includes a reduced set of the core-cells and all the critical paths as pre-charge devices, sense amplifiers, write drivers, output buffer and the column and row address decoders.

The whole operating environment range has been selected in order to maximize the fault detection probability. Hence simulations have been performed by the variation of the following parameters:

- Process corner: slow, typical, fast
- Supply voltage: 1.35V, 1.5V, 1.6V
- Temperature: - 40°C, 27°C, 125°C
- Resistance values have been chosen from few Ωs up to several MΩs since a large range of possible values have been reported [20].

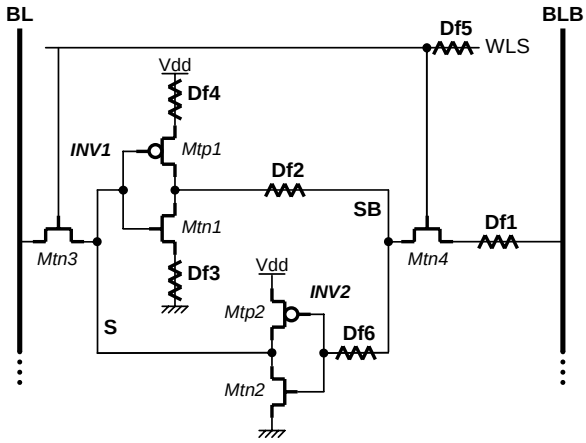

Figure 1: Resistive-open defects injected into the memory core-cell

2.2 Simulation results

In the following, the most significant simulation results are presented. Table 1 shows a summary of the fault models identified for each injected resistive-open defect, according to the conditions which maximize the fault detection, *i.e.* the minimum detectable resistance value. The faults have been detected by 1w0r0 or 0w1r1 sequences.

Dfi	Process corner	Voltage (V)	Temp (°C)	Min Res (kΩ)	Fault Model
1	Fast	1.6	-40	~25	TF
2	Fast	1.6	-	~8	RDF DRDF
3	Fast	1.6	125	~3	RDF DRDF
4	Fast	1.6	125	~130	dRDF
5	Fast	1.6	-40	100/140	IRF/TF
6	Fast	1.6	125	~2 M	TF

Table 1: Summary of worst-case PVT corners for the defects of Figure 1 and corresponding minimum detected resistance and fault models [18]

In this table the first column (Dfi) indicates the defect location in the core-cell. The following four columns correspond to the electrical parameters which maximize the fault detection. The last column gives the

corresponding fault models that have the following definitions:

- Transition Fault (TF): *A cell is said to have a TF if it fails to undergo a transition (0 → 1 or 1 → 0) when it is written.*
- Read Destructive Fault (RDF) [4]: *A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output.*
- dynamic Read Destructive Fault (dRDF) [12, 13]: *A cell is said to have an dRDF if a write operation **immediately** followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output.*
- Deceptive Read Destructive Fault (DRDF) [4]: *A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell.*
- Incorrect Read Fault (IRF): *A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell.*

2.3 Fault analysis

Now let us detail the faults induced by the injected defects with more details. For this purpose we analyze the effects produced for different resistance sizes by each single defect in **typical** condition of supply voltage, temperature and process corner. A special care is dedicated to the behavior that may involve dynamic faults that are notoriously hard to detect.

Defect 1 involves essentially a transition fault (TF) for a defect size larger than **40 kΩ**. The defect produces a delay in the operation of charging/discharging of the node SB during the writing phases. This kind of fault is static and many common March tests are able to detect it.

Defect 2 implies a RDF and in certain cases a DRDF. The defect induces a delay in the output of INV1 during the discharge of node SB. This delay may be the cause of a destructive read. During the r0 operation, BLB is pre-charged at Vdd and for a certain time it pulls-up SB that is at '0'. The capacitance of a bit line is much larger than the equivalent capacitance of cell node at SB. Moreover, the pull-up action is not well counterbalanced as expected by the pull-down action of INV1 because of the resistive defect. For this reason the read operation may cause the commutation of INV2 and so the swap of the cell. Sometimes the destruction of the stored value does not involve an incorrect read, so it is necessary a further read operation to observe the fault.

Defect 3 produces effects similar to those of defect 2. We can add that for both the faults inducted by defect 2 and 3, RDF and DRDF, the simulations have shown that the best sequence useful for the sensitization is the 0w1r1, not necessarily performed at speed frequency. This constraint is useful in the selection of the detection algorithm.

Defect 4 is placed in the pull up of INV1 and produces a hard to detect fault [6]. In this case a test for static faults can detect a faulty behavior only for very large resistance values (**>140MΩ**). The detection of the faults inducted by defect 4 can be improved by a series of read operations performed at speed. Under simulation, the sequence that allows the best fault sensitization is $1w0(r0)^n$, *i.e.* '1' is stored, a w0 is operated followed by *n* r0 operations [18]. At the n^{th} r0 operation the stored '0' swap to '1'. The number *n* is connected with the defect size. This is a dynamic Read Destructive Fault (dRDF).

Defect 5 may represent the resistive effect of long connections as the word lines are. It implies an IRF for defect size larger than **100kΩ** and also a TF for Df5 larger than **200kΩ**. IRFs and TFs are static faults. These two faults occurs because the read and write operations need a certain minimal time to be performed. During these operations the nodes S and SB are connected to the bit lines BL and BLB by the pass-transistors Mtn3 and Mtn4. The defect involves a delay in the switching on of these two transistors reducing the operative time of the read/write operations. The read operation needs a time larger than a write one to be acted, thus the IRFs appear for littler resistance size than the TFs.

Defect 6 is at the input of INV2 and involves a transition fault (TF). The fault appears for high values of resistance (**>2MΩ**) because the defect is placed at the gates of the two transistors of INV2. No bias current enters in the MOS transistor gate thus the resistive defect has to be very large to generate large delay. The TF appears during the write operations. Defect 6 produces a delay for both the operations of pull-up (w1, '1' on BL and '0' on BLB) and pull-down (w0, '0' on BL and '1' on BLB) of INV2, thus the write operation may fail. In particular for w0 there is a faulty behavior for **Df6 > 4MΩ**, while for w1 there is a faulty behavior for **Df6 > 2MΩ**. The different resistance threshold is outcome of the fact that, during a write operation in an SRAM cell, the first to commute is the node where a '0' is forced [19]. Consequently the incorrect writing is more probable when a '0' is forced on BLB, *i.e.* during a w1.

We can divide the elaborated fault models in two groups. The first one includes the dynamic fault produced by defect 4. The second group is composed by the faults

induced by defects 1, 2, 3, 5 and 6. These faults are static. We can remark that the dynamic fault is generated by a defect that contrasts the loop of the two inverters. In fact this defect disturbs the self refreshment of the stored value. Even if defect 2, 3 and 6 are also on the loop path, they present a static behavior as accurately shown by the simulations.

3 A test solution to detect all resistive-open defects

The static fault models extracted from the defect injection are covered by many common March tests as we show in the first sub-section. In the second one we focus especially on dynamic faults coverage. In the third sub-section we propose a unique test solution for all the examined faults.

3.1 Static fault testing

The static faults that are concerned in this study are TFs, IRFs, RDFs and DRDFs. The TFs are a particular case of SAFs. They occur when, for a certain cell, it is impossible to produce an up (down) transition. Many March tests, also simple like MATS and March X, cover TFs. In fact for their detection is it is sufficient the presence of March elements in which all the cells are written and read with both the logic values '0' and '1'. Thus both the transitions are tested.

The same simple requirements are needed for the IRFs and RDFs detection, because it is enough to write and read some data in the cells to verify eventual incorrect read. For the DRDFs there are supplementary requirements. The fault sensitization is operated during the read operation. When the value is read there is swap of the cell that does not involves necessary a wrong value read. Consequently the detection algorithm needs to have a least two sequential read operation for each cell, otherwise there can be a mask effect. Among the tests that can cover DRDFs there are March Y and March C+. All the March tests that we have been mentioned in this subsection are not able to cover the dRDFs induced by defect 4.

3.2 Dynamic fault testing

At this point we start with the detection of the dRDF. This is a dynamic fault that needs a sensitization sequence like $1w0(r0)^n$, *i.e.* a write operation and multiple read operations have to be performed in sequence to produce the swap of the value stored in the cell. If the required number of read operations is high the detection algorithm may increase dramatically in complexity. Therefore, it is opportune to use another way to sensitize this dynamic fault. For this purpose in our last work presented in [14], we have demonstrated that read or write operations on a cell involve a stress on the other cells of the same word line. This stress, called Read Equivalent Stress (RES), has the same effect than a read operation.

When a cell is selected for a read or write operation the pre-charge circuit is normally turned off in its bit line. For the bit lines that are not involved in the operation, the pre-charge circuit is commonly left on. With the pre-charge active and the word line being high on the unselected columns, the cells fight against the pre-charge circuit. Consequently the stress produced by a read operation on a cell is equivalent to the stress caused by a read or write operation performed on whatever cell on the same word line. The good equivalence between read stress and RES is confirmed by electrical simulations that have been performed on Infineon 0.13 µm embedded-SRAM family with the Infineon internal SPICE-like simulator. The waveforms in Figure 2 are referred to the case of a faulty cell, where the defect Df4 is present and has a size of 1.4 MΩ. The cases simulated are the following ones:

a. On the faulty cell a w0 operation is performed, immediately followed by r0 operations.
b. On the faulty cell a w0 operation is done, immediately followed RESs.

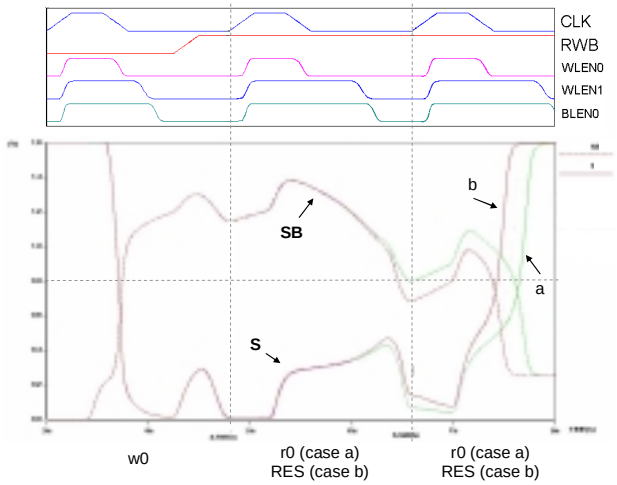

Figure 2: Waveforms of simulations (defect 4)

The waveforms represent the control signals: CLK, RWB which is the read/write selection, and the word line and bit line enable signals (WLEN0, WLEN1 and BLEN0). The voltage values of S and SB nodes (see core cell presented in Figure 1). These waveforms show that after a w0 operation the fault free inverter of the cell has its output (node S) normally switched to '0' logic, that is an effective electrical 0V. The other inverter has its output switched to '1' logic, that does not correspond to an exact Vdd value, due to the delay effect involved by defect Df4.

In the both cases, a and b, there is an abnormal swap of the faulty cell after two cycles. This is a confirmation that the effects produced by the read equivalent stress in term of sensitization of dRDF are very similar to actual read stresses. Moreover, parametrical simulations have been made with different cycle time and with a reasonable resistive range for the size of the resistive-open defect Df4 on the Infineon SRAM memory structure for both the

cases, a and b. The results summarized on the graphs of Figure 3 show that there is a clear similarity between the actual read stresses and RESs. A more detailed analysis of the two graphs in Figure 3 confirms that the sensitization effect of the RESs is higher than that produced by read operations on the faulty cell.

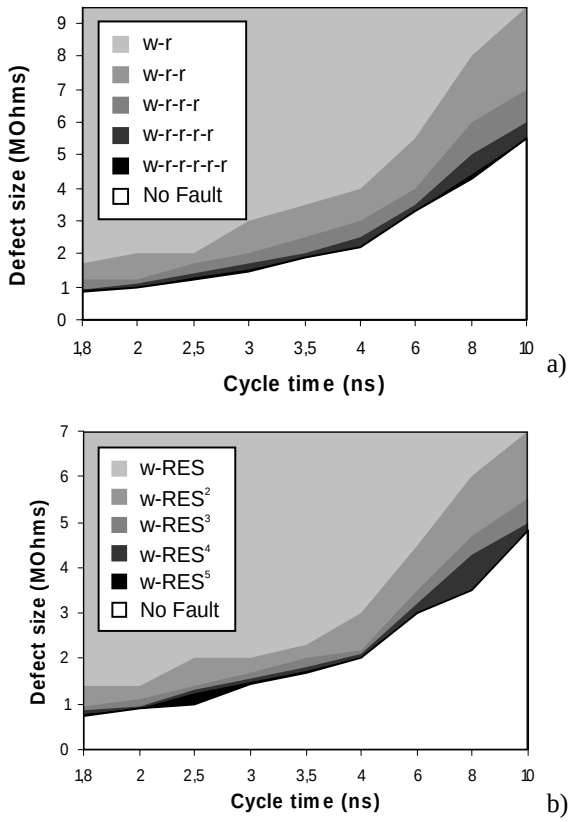

Figure 3: Fault detection as a function of the cycle time, defect size and number of a) read operations b) and RES*s* (typical process, T=125°C, V=1.6V)

3.3 The exhaustive March test solution

In this sub-section we use the results presented above in order to produce an efficient test for all the fault models that we have identified in the core cell, in particular for the dynamic one produced by defect 4. Among the various types of algorithm we choose March tests that allow to reach a good effectiveness though their small complexity. In order to ensure the detection of the dRDF, induced by defect 4, in [14] we have proposed to use the March C- that normally covers 0% of dRDF [13], with an opportune modification. March C- is represented in Figure 4 and the modification is the following one: The read/write operations of the algorithm have to be performed with a particular addressing order with the purpose to execute the March elements on the memory array by acting on word line after word line. This is necessary because the RESs are produced only by operating on the cells of the same word line. For example, let us consider again the Infineon 0.13 µm embedded-SRAM architecture. The read and write operations of the March elements have to be operated firstly on all the 512 cells of the first word line, then on the 512 cells of the second word line, and so on.

$$\{\Updownarrow(w0)\ \Uparrow(r0,w1)\ \Uparrow(r1,w0)\ \Downarrow(r0,w1)\ \Downarrow(r1,w0)\ \Updownarrow(r0)\}$$
$$M_0 \quad M_1 \quad M_2 \quad M_3 \quad M_4 \quad M_5$$

Figure 4: March C- structure

Some elements of March C- include w0 operations, necessary for sensitization of the dRDF, and r0 necessary for observation. The elements with w1 and r1 allow the detection of similar faults generated by resistive-open defects placed symmetrically in reference with Df4 (see Figure 1). Moreover, the elements, in particular the sensitization ones, are performed in $\Uparrow$ and $\Downarrow$ sequence. This condition allows that the cells endure a good average distribution of RESs for all the cells along the entire word lines.

The modification makes March C- able to detect dRDFs, but, due to the first of the six degrees of freedom [17] of March tests, it does not change the capability of March C- to detect the former target faults. Among these faults there are the static faults TFs and IRFs that are induced by defects 1, 5 and 6.

As shown in sub-section 3.1 the best sequence to detect the faults involved by defect 2 and 3 is 0w1r1. A '0' is stored, a w1 is operated followed by a r1. With this sequence the cell swaps its value to '0'. Another r0 is needed to observe the fault. As we can see in Figure 4 March C- do not has the pattern 0w1r1, thus apparently we have to use another algorithm that contains it, *e.g.* March Y [16]. As done for the dRDF (defect 4) we propose once again to use the effect of RES and now we show that the modified March C- is able to produce the needed sequence and consequently covers exhaustively all the core cell faults.

Element M_1 ($\Uparrow$ r0w1), operates a r0 (so a '0' is already stored) followed by a w1. The following missing r1 operation, useful to complete the detection sequence, is warranted by one of the RESs produced by modified March C-. This RES warrants the swap of the cell for the sensitization and, as shown by simulation (see Figure 5), the following operated RESs do not comport a mask effect with further swaps of the cell. In this figure, the first part concerns the clock signal (CLK) and the second one the voltage level of node S of the core-cell presented in Figure 1. These waveforms show that for Df2 = 13800 Ω there is not a flip of the cell. Otherwise, for just higher value of the defect Df2 (14100 Ω and 14200 Ω) the node SB commutes from '1' to '0' due to the first RES and does not swap for others following RESs. So, with the action of one RES, element M_1 allows to cover RDF and DRDF (defect 2 and 3).

The proposed March test solution presents many advantages as its linear complexity and the reutilization of an already existing March test. The main benefit is the

high efficiency to detect dynamic faults and its capability to cover exhaustively all the core cell faults.

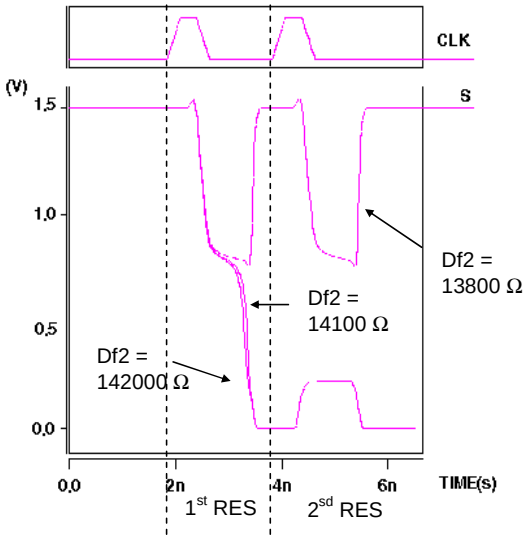

Figure 5: Waveforms of simulations (defect 2)

4 Concluding remarks and future works

In this work we have presented an exhaustive study on those faults that may occur in core-cells of SRAM memories. Evaluations of electrical simulations have been done after a resistive defect injection. We have also shown that a cell undergoes a stress equivalent to a read operation, Read Equivalent Stress (RES), when a read/write operation is performed on a cell of the same word line. Our modification of March C-, which allows to perform the maximum number of RESs, has been demonstrated to be able to test all the fault models resulting from the defect injection in the core cell.

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