A DC-100 GHz Frequency Doubler in InP DHBT Technology

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Abstract **— A broad-band monolithic integrated active frequency doubler operating in DC-100 GHz frequency range is presented. The circuit is fabricated in a self-aligned InP DHBT process. Circuit measurements show sinusoidal output waveform at 100 GHz with a rms time jitter of 400 fs. The doubler has a maximum conversion gain of +1 dB at 60 GHz. The fundamental suppression is better than 24 dB in the whole frequency range.**

Index Terms **— Active splitter, doubler, frequency multiplier, Gilbert cell, InP DHBT.**

I. Introduction

Frequency multipliers, and in particular frequency doublers are important building blocks for many applications, as well as for measurement equipment. The progress of semiconductor technologies based on both specific materials and proper scaling of devices enables to contemplate high speed broad-band system applications up to 100 GHz. Design, as well as measurement, of such high speed circuits presents important challenges. Specific design methodology should be applied. For measurement, high frequency sources are necessary but usual sources such as manufacturer synthesizers are limited at 60 GHz.

In this paper we present the design, fabrication and measurements of broad-band frequency doubler operating from DC to 100 GHz. To implement this frequency doubler, we have chosen a Gilbert multiplier structure [1]. This double-balanced architecture allows to achieve good fundamental and odd-harmonics rejection. The circuit is composed of a Gilbert cell with an input active splitter to achieve multiplication up to 100 GHz. To the author's knowledge, this is the highest frequency of operation for a broad-band active frequency doubler in any technology.

Broad-band active frequency doublers have been described in Si BJT at 12 GHz [2], in SiGe HBT at 42 GHz with 8.6 dB gain [3] and in GaAs pHEMT at 50 GHz with 5 dB loss [4].

In this work we present the InP DHBT technology used for doubler fabrication in section II, the doubler design in section III and measurement results up to 100 GHz in section IV.

II. Technology

The InP/InGaAs Double Heterojunction Bipolar Transistor (DHBT) technology presents several attractive aspects for the fabrication of high speed circuits.

Very high frequency characteristics are due to excellent electron transport properties of InP and InGaAs; the small bandgap of InGaAs base results in a low turn-on voltage, which means a potential for low power consumption; the double heterojunction gives a high breakdown voltage, necessary for large signal applications also studied in our laboratory such as optical modulator drivers; finally, the vertical technological process yields a very good built-in threshold voltage uniformity, very convenient for differential bipolar logics such as CML and ECL.

An InP/InGaAs self-aligned DHBT technology has been developed at OPTO+ [5]. Transistors exhibit a high breakdown voltage (BV_{CE0} >7 V) as the result of the double heterojunction structure. 150-180 GHz F_t and 210-220 GHz F_{max} are currently obtained on circuit-oriented devices at a current density of about 2 mA/μm². Three Ti/Au interconnection levels, TaN resistors, MIM capacitors and spiral inductors are also available to realize the circuit layout.

In Fig. 1 Ft and Fmax frequencies for 2x3 μm² and 2x10 μm² emitter transistors are compared as a function of collector current. Ft above 100 GHz and Fmax over 170 GHz are achieved for currents of 2 mA and up. This means that low power high frequency operation can be targeted.

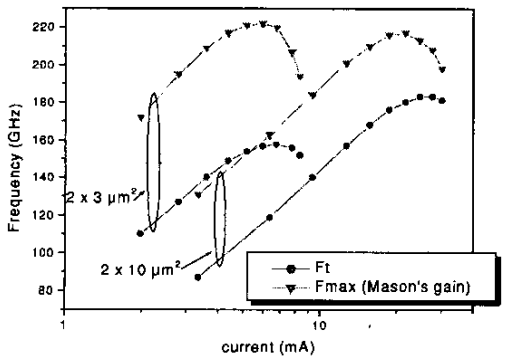

Fig. 1. Ft and Fmax for 2x3 and 2x10 µm² emitter transistors

III. Circuit Design

The frequency doubler is based on a Gilbert cell with the both inputs connected together as shown in Fig. 2. Frequency multiplication results in generating harmonics due to nonlinear characteristics of the transistors in the Gilbert cell.

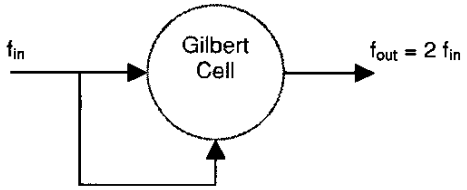

Fig. 2. Gilbert cell as a frequency doubler

A. Electrical design

The first goal of this design was the high frequency of operation (up to 100 GHz). The doubler block diagram is presented in Fig. 3. The IN input signal is changed by the input active splitter into two symmetrical signals (OUT1 and OUT2). These two signals enter on RF and LO Gilbert cell inputs. They are converted by the cell into an IF output signal of double frequency while the fundamental frequency is suppressed.

Usually, frequency doublers based on Gilbert cell structure use an external frequency splitter. In our case, we decided to use an internal splitter. Only one RF input signal is thus needed with the reference DC value (REF). However, two input symmetrical signals can be applied.

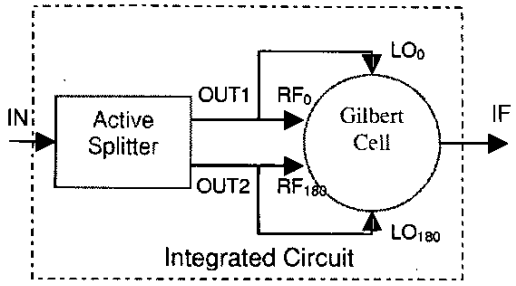

Fig. 3. Block diagram of the frequency doubler

Fig. 4 shows the electrical scheme of the frequency doubler. The active splitter is composed of a differential amplifier with feedback resistors that provide broad-band amplification. Emitter degeneration is used in the amplifier to linearize output splitter signals. The multiplier core (Gilbert cell) is composed of two pairs of emitter followers that feed the LO lower differential pair and one emitter follower pair connected to the RF upper differential pairs. These emitter follower stages realize a level shifting and impedance matching. The differential pair stage is where frequency multiplication occurs. Current mirrors act as stable current sources. All transistor sizes are optimized for the maximum frequency performance. Switch transistors (emitter size 2x10 µm²) operating at 1.5 mA/µm² collector current density are used. For biasing, larger transistors (emitter size 2x15 µm²) are chosen. No output buffer is used: to optimize output swing at high frequencies doubler output is directly connected to the Gilbert cell output. In contrast to most of Gilbert cell, we have chosen to use only one Gilbert cell output to minimize layout parasitics. In fact, this asymmetrical output architecture doesn't reduce circuit performance in simulation. Also, no output filter is used.

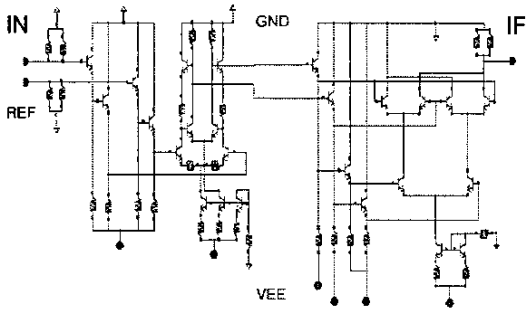

Fig. 4. Electrical scheme of the frequency doubler

B. Layout design

A microphotograph of the doubler circuit is presented in Fig. 5. The chip dimensions are 1400×1600 µm².

Signal lines (two inputs) are fed via matched 50 Ω GCPW (Grounded CoPlanar Waveguide) lines. Similarly output signal is connected to output pads with 50 Ω GCPW lines. Signal part of the layout is compacted to shorten high frequency paths. The circuit core is optimized for minimum wire length and maximum symmetry. The core footprint is 250x350 µm². DC bias connections are decoupled on wafer with RC circuits.

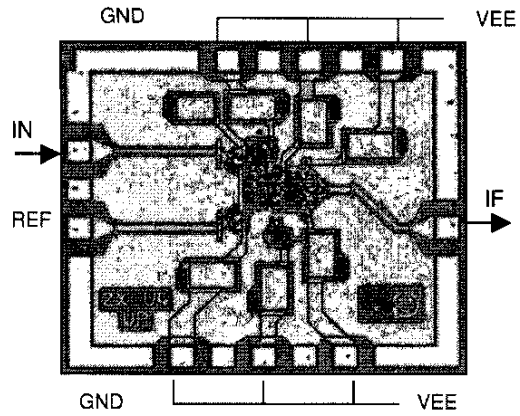

Fig. 5. Microphotograph of the fabricated doubler

IV. Measurement Results

The characterization of the frequency doubler requires adequate measurement equipment as well as a special care in the measurement set-up. The doubler characteristics were measured using on-wafer probing and bias lines. The measurement set-up is composed as follows:

A frequency synthesizer provides a signal up to 60 GHz. Output signal waveform is displayed on an oscilloscope.

65 GHz probes are used at the circuit output. Measurements are realized with remote sampling head (70 GHz) and very short cables. The use of a precision timebase module allows to characterize precisely the time jitter of the doubler.

It is clear from the equipment characteristics, that above 70 GHz our measurements are cumulating hard-to-estimate losses from different measurement elements (probes, cables, sampling head). Indeed, for example, sampling head data sheet give us it frequency response up to 70 GHz. At 70 GHz head losses are about 2.6 dB but above 70 GHz it is very difficult to extrapolate. In the best case, extrapolation is linear but, in the worse case, a bandwidth hole may appear and so losses can be very important.

The doubler was characterized by applying an RF signal on IN pad and a DC reference voltage signal on REF pad. VEE bias voltage is –4.5 V.

Fig. 6 shows the 50 GHz input signal and the 100 GHz output signal of the frequency doubler.

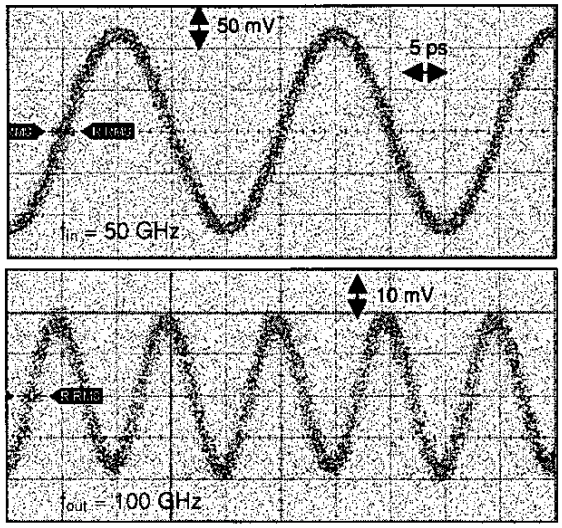

Fig. 6. Measured (top) input and (bottom) output waveforms at 100 GHz.

A 394 fs rms time jitter of the output signal is measured. It is comparable to the 422 fs rms time jitter of the input signal. The output signal amplitude is 41 mVpp.

In Fig. 7, the conversion gain versus output frequency is shown for -8 dBm input power.

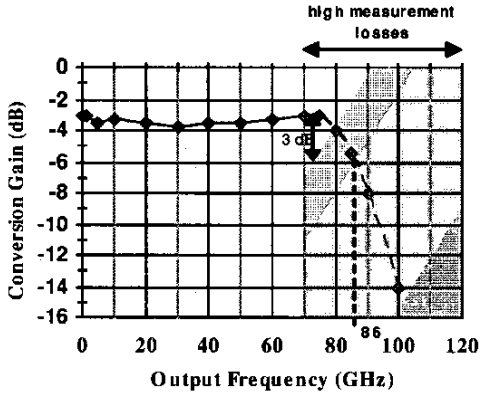

Fig. 7. Measured conversion gain versus output frequency for -8 dBm input power.

It is necessary to note that above 70 GHz the conversion gain is underestimated because of measurement bench losses. A minimal -3 dB bandwidth from DC to 86 GHz is measured.

In Fig. 8, output power and conversion gain versus input power are presented at 60 GHz. For input power values larger than -12 dBm the doubler is in saturation. The maximum output power is -10 dBm. Maximum of +1 dB gain is achieved at -12 dBm input power.

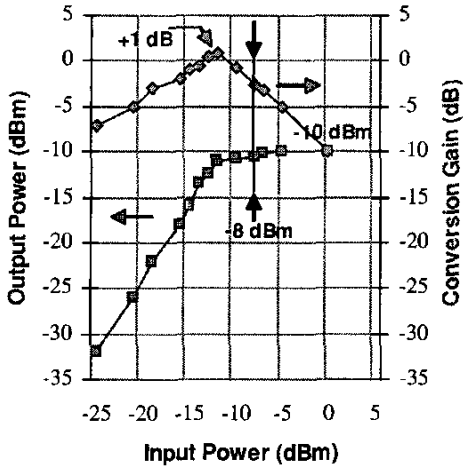

Fig. 8. Measured output power and conversion gain versus input power at 60 GHz.

The fundamental and second harmonic are measured using a spectrum analyser with 50 GHz bandwidth. The fundamental signal is suppressed to the desired spectrum up to 100 GHz with more than 24 dB (Fig. 9).

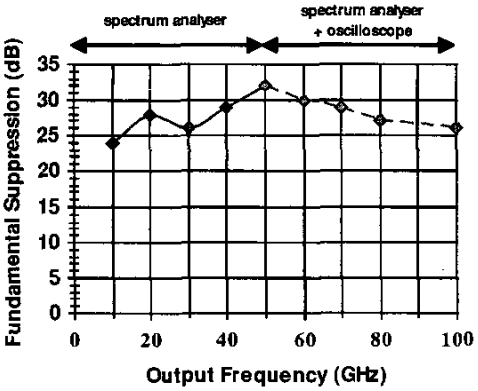

Fig. 9. Measured suppression of fundamental frequency versus output frequency. Input power is -8 dBm.

The circuit presents an optimum rejection of fundamental signal of 32 dB at 50 GHz. Above 50 GHz fundamental power is measured with spectrum analyzer and 2nd harmonic power is computed from oscilloscope output waveform.

The frequency doubler consumes 730 mW shared between the active splitter (580 mW) and the multiplier (Gilbert cell) core (150 mW).

V. Conclusion

In this paper we presented design, fabrication and measurements of broad-band frequency doubler operating in state-of-the-art DC-100 GHz frequency range. A Gilbert cell with integrated active splitter architecture allowed to obtain such high frequency. The fundamental signal suppression in the whole frequency range is better than 24 dB. At 60 GHz maximum conversion gain is 1 dB. These results were obtained in spite of measurement equipment limitations.

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