An Implantable Asic for Neural Stimulation

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AN IMPLANTABLE ASIC FOR NEURAL STIMULATION

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ABSTRACT

The integrated circuit proposed in this paper is dedicated to the neural stimulation of motor muscles for paraplegic people. For this kind of application, the constraints in terms of safety and performances are stringent. In practice our ASIC (Application Specific Integrated Circuit) allows us to deliver precise calibrated stimulation pulses to specific multi-polar electrode together with a very safety running cycle. In particular, the DAC has been thought to be fully monotonic and the output stage to ensure a passive and secure discharge of the safety capacitor. Also some tricky features have been added in order to improve the classical charge pump that generates on-chip high voltage.

1. INTRODUCTION

For a person with an injured spinal cord, the direct control of lower limbs by brain is lost but most of muscles and nerves below the injury remain intact. Two solutions exist to restore muscle control. The first one consists in "rebuilding" the marrow around the injured site. At the time, this technique is promising but not mature enough. The second solution is based on Functional Electric Stimulation (FES) that consists in electrically activating multiple muscles in coordinated sequences. Two FES techniques have been developed, namely (i) external stimulation with electrodes placed on the patient skin and (ii) internal stimulation with surgically implanted electrodes. Internal stimulation may be either epimysial with electrodes on muscles or neural with electrodes implanted on motor nerves.

Various implantable circuits have been recently proposed in the literature to internally generate stimulation waveforms. Some concern epimysial stimulation [1][2], others concern neural stimulation [3][4].

The present paper reports on a new implantable stimulator working in the context of neural internal FES. This ASIC is designed to deliver calibrated current pulses (waveform, amplitude, duration) to a multi-polar electrode directly implanted on the nerve controlling a motor muscle. Apart from the present introduction, the paper is organized into three main parts. Section 2 gives the circuit specifications derived from the global DEMAR project of which the present work is a part. The stimulation cycle is fully described and a model is given for the nerve-electrode interface. Section 3 is devoted to the complete description of the circuit. Emphasis is given on the original features we have developed in designing this circuit, namely (i) a fully monotonic 8-bits DAC, (ii) an improved DC-DC converter, (iii) an original output stage able to deliver multi-valued current and ensure safe discharge phase for stimulation cycles. Finally in the last section, we give some experimental results to evaluate the performances of the stimulator.

2. STIMULATOR SPECIFICATIONS

The design of the stimulator is part of a larger project, namely the DEMAR project (Artificial Movement and Deambulation) [5]. DEMAR aims to allow paraplegic patient to recover some mobility. The stimulator corresponds to the electrical part of this project and this section plans to describe its specifications.

2.1 Stimulation Current

Figure 1 shows the waveform of a classical stimulation cycle. For safety reasons, this pulse has to be a biphasic current pulse with a null mean value. Indeed, during the stimulation some charges are stored around the nerve and, to avoid any electrolytic effect, it is mandatory to draw out these extra charges. The stimulation phase is thus followed by a discharge phase with amplitude sufficiently low to not be perceived as a new nerve excitation.

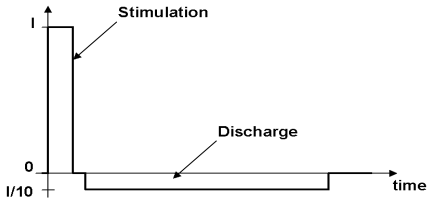

Figure 1. Stimulation cycle

For our application, we have to respect the specific constraints that are summarized in table 1.

Specifications	Values and ranges
Stimulus pulse width	20µs - 1ms by 5µs-steps
Stimulus pulse amplitude	0 - 5mA by 20µA-steps
Max. discharge current	$I_{stimulation}/10$
Min. cycle period	20ms

Table 1. Specifications of the stimulation cycle

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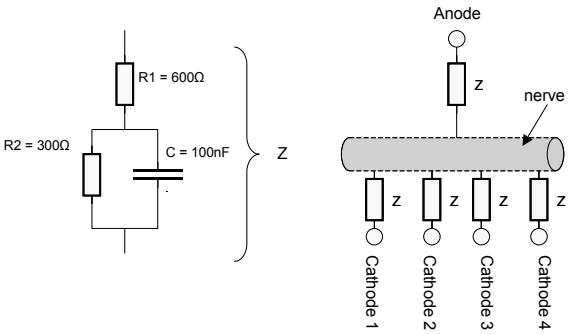
2.2. Stimulation Electrode

The neural stimulation electrode is an essential element. It is a multi-polar electrode with one anode and four cathodes. As shown in [6][7] a multi-polar electrode allows one to stimulate different parts of a nerve by varying the current ratio between cathodes. The Z impedance (figure 2a) models the contact between each terminal of the electrode and the nerve. If we consider the nerve as an ideal physiological medium that is perfectly conducting we can establish the simplified electrode model given in figure 2b. Obviously, the parameters of this model have been adjusted to match the behavior of the actual electrode.



a) b)

Figure 2. Model of nerve-electrode interface

On the other hand, safety regulations impose that a stimulation system must not create a DC current in any part of the body. To satisfy this requirement, a C_{safe}=2 µF capacitor is serially connected to each cathode.

Thanks to this complete model, we can estimate the minimum voltage (11.5V) we have to impose between the terminals of the electrode in order to force the stimulation current. Obviously, the stimulation circuit has to provide more than this critical voltage. In practice, we choose to dispose a 15V voltage in our stimulator.

The following section describes the design of this stimulator.

3. STIMULATOR DESIGN

The circuit architecture is described figure 3. It includes a digital part (not described in this paper), a high voltage source realized with an improved Dickson charge pump, a strictly monotonous Digital-to-Analog Converter and an output stage able to drive the multi-polar electrode.

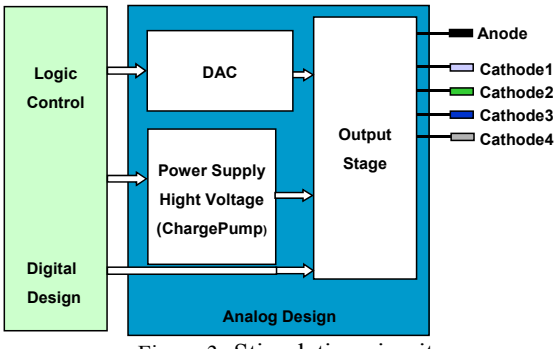
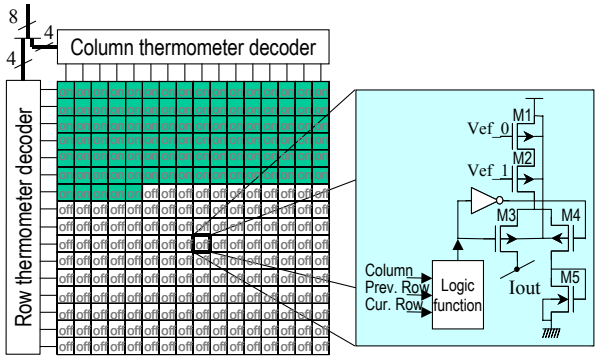


Figure 3. Stimulation circuit

3.1. Digital-to-Analog Converter

We have developed a current output 8-bit DAC. For our application, the Differential-Non-Linearity (DNL) is a very critical parameter. Indeed, 1 or 2 LSB current variation might induce a too strong muscle stimulation effect. Another critical parameter is the monotonicity. Indeed, this DAC will be used in a feedback loop that imposes it to be strictly monotonic. Although it is formally possible to design strictly monotonic weighted sources DAC at the price of a very careful analogue design, we chosen to develop a new fully monotonic DAC based on the partially monotonic Miki structure [8].

In the DAC architecture (figure 4), the thermometer decoders ensure that whenever the digital code increases, unity current sources are added to the set of current sources providing the output current without removing any of the previous ones. Provided that the output current of each unity current source is strictly positive, the converter is strictly monotonic.



a) b)

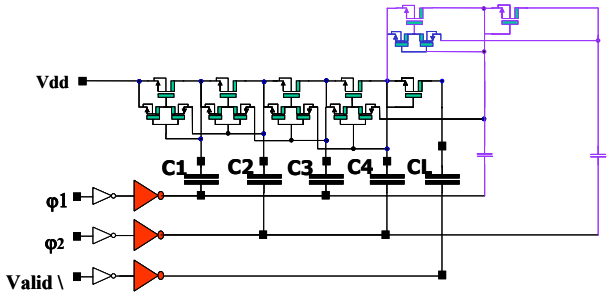
Figure 4. Fully monotonic DAC

Moreover, to obtain good figures for DNL we need very accurate unity current sources. Figure 4b shows the schematic of the unity current source we propose. In this structure, M3 and M4 implement current switches that avoid the current mirror (M1, M2) to be saturated when the source is unused. Furthermore, the loads of each branch are balanced in order to keep a constant potential on the sources of M3-M4 before and after the switching, thus optimizing it. In addition, in order to reduce the power consumption, the DAC is designed to generate a current that is smaller than the stimulation one. The final stimulation current will be obtained via the output stage that will mirror and amplify the DAC output current.

3.2. High voltage generator

As we have seen in the section 2.2, we need a 15V on-chip voltage to generate the maximum stimulation current. Because our circuit is designed for a 3V supply voltage, we need to integrate a DC-DC converter to generate this high voltage. Classically, we can consider two kinds of converters: inductive storage or capacitive storage converters. In spite of its good performances the inductor-based converter was discarded because the difficulty to integrate coils in a circuit. In practice, the power available at the output of a DC-DC capacitor-based converter grows with both

the size of the capacitors and the switching frequency. So, we chose to develop an original design based on an improved Dickson charge pump [9]. Our converter (figure 5) is made of 5 stages, with CTS (Charge Transfer Switches) [10] to improve voltage efficiency. Moreover, we have developed new particular features considering that the converter is used in a non-conventional context.



C1, C2, C3, C4 and CL are external capacitors

Figure 5. Charge pump

Our application forces us to avoid any switching activity during the stimulation phase. Consequently, we need to store enough energy in the capacitors before the stimulation. The needed energy imposes the size of capacitors. During the stimulation phase the output voltage weakens according to the simple following expression: $\Delta V=I.\Delta t/C$. Considering the difference between available and needed voltages ($\Delta V=15-11.5-1=2.5V$) and taking into account the maximal width and amplitude of the stimulation pulse ($\Delta t=1ms$ and $Io=5mA$, respectively), we can derive the minimum value for the capacitors ($C=2\mu F$). On the other hand, in order to optimize the power consumption, we want to minimize the switching frequency during pump loading. The charge of the pump will take place during the discharge phase of the stimulation cycle. For our pump, we have established that the full charge of the pump from a partially charged state needs about 60 switching periods. The minimum discharge time being around 20ms the minimum switching period is about 3kHz and in practice we choose 5kHz.

Let us have a look on another particular feature we have developed. In order to limit the peak power consumption, we have chosen to use output buffers with controlled slew rate to drive the capacitors. Considering that all capacitors are external, we can directly use the buffers naturally implemented in standard digital output pads.

3.3. Output stage

The output stage implements three functionalities:
First, its main role consists in mirroring and amplifying the output current of the DAC.
Second, the output stage must share out the I_0 stimulation current between cathodes in order to activate different parts of the nerve. In practice, we designed this output stage in such a way that each cathode can be fed by individual current taken among the following set of values { I_0; $3I_0/4$; $2I_0/3$; $I_0/2$; $I_0/3$; $I_0/4$; 0}. To implement these current ratios, the output transistor is split into 4 groups of 12 elementary transistors, each group being associated to one cathode as shown figure 6. The logic control (around 200 gates) has been designed in such a way that exactly 12 transistors are conducting at the same time, thus allowing us to obtain the 33 possible configurations.

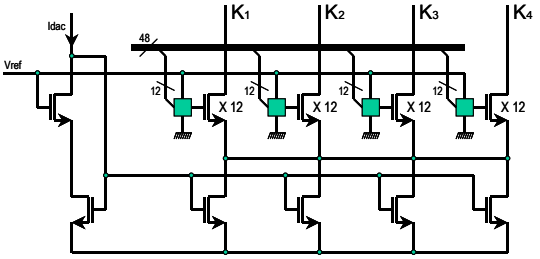


Figure 6. Output stage current mirror

Third, this output stage has to implement the discharge phase of the stimulation cycle corresponding to the discharge of the safety capacitor C_{safe}. To limit this discharge current to 10% of the max stimulation current, we should have to connect a large enough resistive load between each cathode and the common anode, in our case $R>5k\Omega$. However, with such large resistances, the discharge time would exceed the minimum stimulation cycle ($5.\tau=5.R.C_{safe}>20ms$). To prevent this drawback we implemented a design in which we have the opportunity to sequentially add smaller and smaller resistances in parallel. This allows us to progressively lower the time constant while preserving the maximum discharge current ($I_0/10$) at each step. The figure 7 shows a 3-step discharge phase.

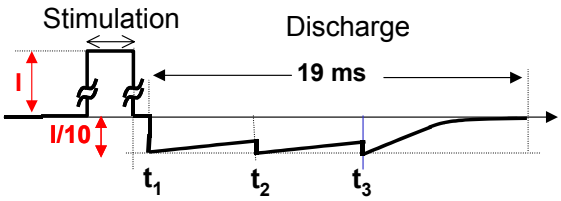


Figure 7. Three-step discharge phase

4. STIMULATOR PERFORMANCES

To validate and characterize the different blocks of the stimulator, we realized a test vehicle. In this circuit we have implemented two DACs and two Output Stages. One of each instance is totally controllable and observable allowing a fully independent characterization of each of these functional blocks. The second element permits us to assess the complete stimulator and the influence of each block on the other ones. This test vehicle has been fabricated using the 0.8µm High Voltage CXZ technology from AustriaMicroSystems. The silicon area of the ASIC is 4.5 mm x 3.4 mm = 15.3 mm^2. Figure 8 shows a die photomicrograph where we can distinguish: the charge pump in the lower left corner that occupies very few space on the final layout because capacitors are externals, the two instances of the DAC and the two instances of the output stage. On the latter, we can point: (1) the logic decoder driving the output transistors; (2) the four blocks of output transistors; (3)

the resistors and transistors of the discharge block; (4) the high voltage multiplexer that allows selecting the better anodic high voltage from the charge pump.

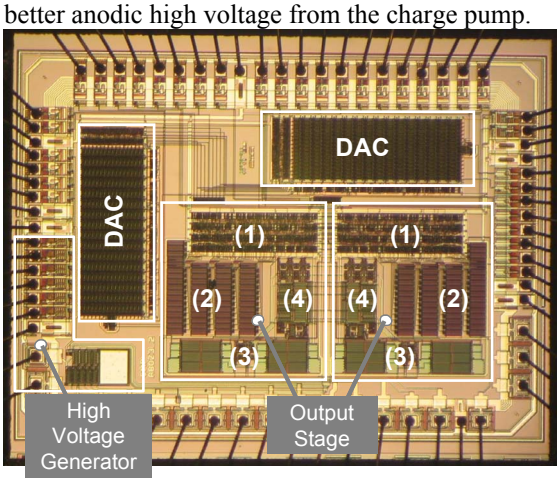


Figure 8. Die micro photograph

Figure 9 shows the two correlated current pulses available at the Cathode 3 and Cathode 4 ASIC outputs when it is configured for $I_{cathode3} = I_0/3$ and $I_{cathode4} = 2\ I_0/3$. Similar waveforms are obtained for all the planned configurations. On this figure, we can also verify the properly limited amplitude of the discharge current.

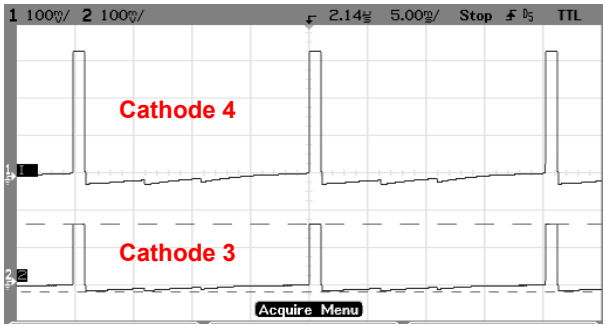


Figure 9. Measurement of the stimulation current

For the charge pump, we measured a 175ms settling time at the power up. The recovery time, i.e. the time needed by the pump to return to its "full charge" state after the highest stimulation (5 mA during 1 ms) never exceeds 15 ms, which is lower than the minimum stimulation cycle. These results are obtained with the quite low clock frequency of 5 kHz. Fitted with 2µF capacitors, powered under 3V and fully charged (175 ms after power up) the charge pump is able to provide the following voltages: 3, 6, 9, 12, 15 and 18V. The voltage drop induced by the drawing of the 5µ Coulomb of the larger stimulation pulse is 2.5 V for the 3, 15 and 18V outputs and 1.3 V for the others (6, 9, and 12V).

On the output stage, the output resistance of one cathode is 2.5MΩ and the inter-cathode resistance is 300kΩ. To achieve these results, the output voltage (measured between VSS and the ASIC output) must be larger than 0.85V. If this condition is fulfilled, for the maximum output current, the mismatch between two cathodes does not exceed 170µA, i.e. 5% of the total current.

As a conclusion, the specs of our stimulator are summarized in the following table.

Parameters	Values and ranges
Process:	AMS 0.8µm HV
Supply:	3 V
Output/Cross output resistance:	2.5MΩ / 300kΩ
Output current mismatch:	5 %
Output voltage range:	0.85 V – 18 V
Output stage linearity:	1 %
Charge pump clock frequency:	5 kHz
Charge pump capacitors:	2 µF
Charge pump settling time:	175 ms
Charge pump recovery time:	15 ms
Charge pump output voltages:	3, 6, 9, 12, 15, 18 V
Charge pump output capacity:	2 µF (3, 15 & 18 V) 4 µF (6, 9 & 12 V)

Table 2. Design Summary

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