Digital, Memory and Mixed-Signal Test Engineering Education: Five Centres of Competences in Europe

Marie-Lise Flottes, Yves Bertrand, Luz Maria Balado Suarez, Emili Lupon, Anton Biasizzo, Franc Novak, Stefano Di Carlo, Paolo Prinetto, Nicoleta Pricopi, Hans-Joachim Wunderlich

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Digital, Memory and Mixed-Signal Test Engineering Education: Five Centres of Competence in Europe

M-L. Flottes, Y. Bertrand
Centre de Ressources de Test du CNFM (CRTC), and Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM), University of Montpellier, France
flottes@lirmm.fr, bertrand@lirmm.fr

L. Balado, E. Lupon
Universitat Politècnica de Catalunya, Barcelona, Spain
balado@eel.upc.es, lupon@eel.upc.es

A. Biasizzo, F. Novak
Jozef Stefan Institute, Ljubljana, Slovenia
biasizzo@ijs.si, franc.novak@ijs.si

S. Di Carlo, P. Prinetto
Politecnico di Torino, Torino, Italy
stefano.dicarlo@polito.it , paolo.prinetto@polito.it

N. Pricopi, H-J. Wunderlich
Institut für Technische Informatik, Universität Stuttgart, Stuttgart, Germany
pricopin@ra.informatik.uni-stuttgart.de , wu@informatik.uni-stuttgart.de

Abstract

The launching of the EuNICE-Test project was announced two years ago at the first DELTA Conference [1]. This project is now completed and the present paper describes the project actions and outcomes. The original idea was to build a long-lasting European Network for test engineering education using both test resource mutualisation and remote experiments. This objective is fully fulfilled and we have now, in Europe, five centres of competence able to deliver high-level and high-specialized training courses in the field of test engineering using a high-performing industrial ATE. All the centres propose training courses on digital testing, three of them propose mixed-signal trainings and three of them propose memory trainings. Taking into account the demand in test engineering, the network is planned to continue in a stand alone mode after project end. Nevertheless a new European proposal with several new partners and new test lessons is under construction.

1. EuNICE-Test objective

EuNICE-Test acronym stands for **Eu**ropean **N**etwork for **I**nitial and **C**ontinuing **E**ducation in VLSI/SOC **Test**ing using remote ATE facilities. This is a 2-year long European IST (Information Society Technology) project that was just completed in September 2003. The objective of the project was to address the shortage of skills in the microelectronics industry by educating students at pre- and post-doctoral levels in the field of test engineering. The idea was to strengthen, in critical disciplines of design and test in microelectronics, leading educational centres, with the active support and guidance of industry. In the field of test engineering, the microelectronic industry suffers an important shortage in microelectronics engineers having sufficient skill in test development, especially for mixed-signal circuits. At the starting point of the project, initial education in that field was too little developed in Europe, just restricted to the French experience with 200 students and engineers trained per year. Taking into account the context described above, there was a strong demand from the microelectronics industry in engineers having knowledge ranging from the simple awareness of test problems (design engineers) to the full skill and competence in IC testing (product engineer, test engineer). It was the objective of the present educational project to respond this demand by implementing a European network for test engineering education both in initial and continuing education context. The project aims at educating European microelectronics students in IC testing through the implementation of dedicated training courses on high-performing ATEs.

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Such testers are intensively use by circuit manufacturers during either the characterisation phase of new designs or the production phase of mature devices.

In this context, EuNICE-Test project aims to be the seed of a European network for initial and continuing education in test engineering in order to respond the industrial demand for microelectronics engineers having a double Design & Test competence. This educational project is based upon the successful experience [2-5] of CRTC, the common test resource centre for French universities. The expansion at European level includes 4 new academic partners, namely UPC Barcelona (Spain) **[UPC]**, Politecnico di Torino (Italy) **[Polito]**, University of Stuttgart (Germany) **[UST]** and Institute Jozef Stefan of Ljubljana (Slovenia) **[JSI]**. Agilent Technologies **[Agilent]** is the key industrial partner of the project for providing up-to-date equipment and specific education on clearly identified hot test topics. CRTC **[CRTC/LIRMM]** is the leader of the project. Because CRTC is hosted by a research laboratory (LIRMM) internationally renowned in the field of circuit testing, it benefits from the competence of these permanent researchers. The teaching staff of CRTC is composed of researchers and professors fully implicated in various research projects on the design and test of integrated circuits and systems. Such projects include DFT and BIST for digital, analogue and mixed-signal circuits and design and test of fully integrated microsystems. Also, all the other participants in the consortium have a full competence and expertise in the field of IC testing. This ensures both solid theoretical background and up-to-date test knowledge for the trainees. Finally, the project benefits from the Agilent Technologies active support. This partnership allows taking advantage of the very last technological developments for ATEs and ensures the achievement of skill and practical knowledge for the trainees through the use of advanced test equipment.

2. Test resource mutualisation and remote testing

Each partner is a centre of excellence with international renown in the field of IC testing (new algorithms for ATPG, advanced DFT/BIST architectures, methods for analogue test, test standard development, IDDQ testing, etc.). The strong CRTC/Agilent partnership makes a high quality industrial tester (Agilent 83000 F330t) is available at CRTC. Tester comes with its software and is fully equipped with a server and a workstation. Classroom for lectures and practice are also available at CRTC. Additional hardware and software for each European centre is relatively limited and includes a server station equipped with Agilent SmarTest software suite, plus 8 workstations connected to it.

The network is articulated around CRTC common test resources. The advantage of having a one and only one resource centre for all the project partners is obvious. Mutualisation allows to put very performing up-to-date testers at partners disposal. This saves money by avoiding the replica of clearly underused test resources in several scattered centres. On the other hand, in a context of a "mass education", the price to pay for having centralised resources is the travelling and lodging costs for trainees. So, the original idea of the CRTC project was to permit a network connection on the common tester to implement a remote test of the circuit. Using this configuration, up to 16 students may be locally trained in parallel using the 8 workstations connected on a server equipped with software test development resources. Only at the very last moment of the physical test they have to be connected to the tester through the network (Figure 1).

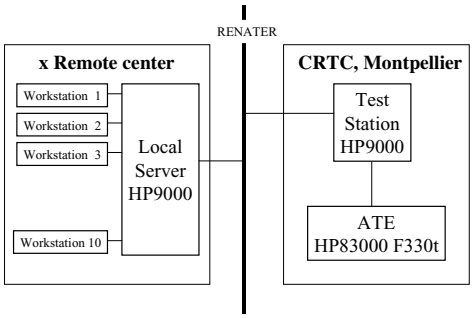

Figure 1: Network implementation for remote test

Training courses are open for pre- and post-doctoral students from universities or engineering schools. The training contents are issued from those developed by Agilent for the 83000 tester [6-8].

Digital training courses aim to initiate students and engineers to digital IC test. After completing level 1 training, each trainee will be able to (i) make competent use of any digital ATE to test a device for its performance parameters and specifications, (ii) build up a test flow to automate the test execution and (iii) create a test program to be executed on the production test floor. After completing level 2 training, he will have gained the know-how to (i) test complex devices, (ii) convert simulation data and (iii) make optimum use of tester resources. Both training courses use a standard digital circuit as DUT (Device Under Test) to simply illustrate all the test functions. Each training course is built up on lessons and related lab exercises. The network configuration of CRTC allows any trainee in any distant center to prepare lab exercises using the local resources. Also the correctness of both input signal shapes and output strobe locations may be locally verified. Only the test execution itself necessitates a remote connection on the CRTC tester in Montpellier.

Mixed-signal training courses aim to initiate students and engineers to the test of analogue and mixed-signal circuits.After completing the training, students are able to

make competent use of the Agilent 83000 F330 to test a mixed-signal device for its performance parameters and specifications. They are prepared to plan appropriate tests by utilizing the SmartDSP instruments. They are able to develop test programs for mixed-signal devices and use the available tools for developing and debugging mixed-signal tests.

Memory training courses aim to initiate students and engineers to the test of various types of memory, including memories embedded in SoC. After completing the training, students have an overview of the common elements of a memory device, and what is involved in testing memories. They know how the memory test software works, and how to set up and execute a memory test using the user interface. They learn how to use the result tools available that enable to characterise the device.

3. Project workplan

EuNICE-Test project is a two-year long project divided into four interdependent work-packages. The Gann chart of these work-packages is given in Figure 2. The trainers of each academic partner have been first trained to test engineering on the Agilent 83K tester of CRTC in Montpellier (WP1: Digital Training for Trainers). Next, these trainers have performed the same training course to their students, concurrently in each centre [UPS, Polito, UST and JSI] (WP2: Training implementation). Finally, the industrial partner [Agilent] taught academic participants to specific test techniques (WP3: Specialized Test Training for Trainers) and one of the partners [JSI] organized a specialized training to their students (WP4: Mixed-signal Test Training implementation). So at the end of the project, each academic centre is specialised in a given test field: mixed-signal test and/or memory test.

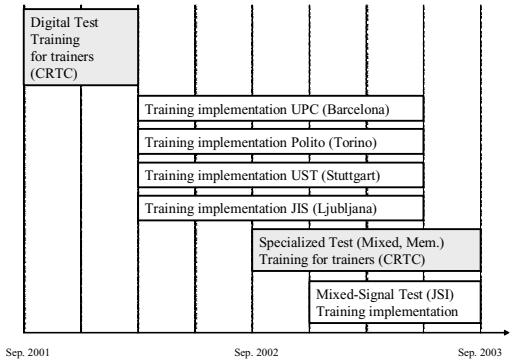

Figure 2: EuNICE-Test project planning

4. Project outcomes and assessments

4.1. Training implementation

All the tasks of the Gann chart of Figure 2 have been completed on time according to original schedule.

First, all the European trainers (9 people) have been trained in digital test at CRTC during two weeks.

Then the set-up of the four centres has been completed for student local education. This set-up covers:

- Equipment purchase order & installation
- Software installation and running
- Network and Internet connection up and running
- First successful online connection to ATE.

The way each training course for student is implemented depends on the local context. The global organisation of syllabus, the initial level of the students and the pedagogical approach of the teaching team make the organisation is different in terms of number of students, number of groups and course duration (see Table 1). This demonstrates the good adaptability of the remote system. Once a working time slot is reserved through the Web site of CRTC [9], the tester is fully devoted to the remote centre. Then the teacher is free to dispose of the tester, exactly as if it was located on the local site, and he can implement the training at his own convenience.

The initial objective of training 16 students per academic centre during the project has been globally respected. Of course, depending on local context and need, the figures vary a little bit but the mean value of trained student is around 17. During the EuNICE-Test mid-term meeting in Stuttgart (September 2002) the efficiency of remote test connection for educating student in digital test has been demonstrated by a demo and approved by both the European referee and the European Project Officer.

So, the EuNICE-Test project has permitted training 69 additional students in digital test in Europe (Table 1). This gives an increase of 43% compared to the sole educational program in France (160 trainees).

Table 1: Digital Training implementation in European Centres

Centre	# Students	# Groups	# Students per group	# Days	# Hours Per student (Lecture + Labs)	# Trainers
UPC	10	5	2	6	18 + 24	3
POLITO	25	6	4 (or 5)	16	22 + 14	2
JSI	21	2 x 5	2 (or 3)	6	6 + 9	2
UST	13	6	2 (or 1)	10	20 + 20	2
Total	69					9
LIRMM	20	10	2	6	18 + 24	3
France	160					24

Also mixed-test and memory training for trainers have been implemented in each of the 4 European centres. All have been completed on time according to original schedule.

Specialized test training on Mixed-Signal testing was organized in January 2003 at LIRMM/CRTC. Seven persons involved in the EuNICE-Test project participated to this specialized training: 2 from LIRMM/CRTC, 2 from UPC and 3 from JSI. In order to provide the project with the necessary hardware equipment, Agilent improved the LIRMM/CRTC Agilent 83000 F330t tester configuration. The following cards have been installed:

- SWI (Smart Waveform Instrument) card. This card features two independent but identical instruments called SWI channels. Each SWI channel contents an arbitrary waveform generator, a waveform digitizer, and a DSP.
- SWG (Smart Waveform Generator) card. This card can be used to generate up to four independent analogue signals, including high frequency sinusoid and video waveforms.
- SVS (Smart Video Sampler) card. This hardware is aimed at dynamic measurement of video signals. It contains also two waveform digitizers for general purpose applications.
- SCM (Smart Capture Memory). It can acquire up to 64K of 16 bits words at rate up to 50 MHz.

Specialized test training on Memory testing was organized in April 2003 at the Training Centre of Agilent Technologies (Böblingen, Germany). Seven trainers involved in the EuNICE-Test project participated to this specialized training: 3 from LIRMM/CRTC, 2 from Polito and 2 from UST.

Finally, as scheduled in the EuNICE-Test project, JSI has implemented a Mixed-Signal training course for its students. During the EuNICE-Test final meeting in Ljubljana (September 2003) the efficiency of remote test connection for educating student in mixed-signal testing has been demonstrated by a demo and approved by both the European reviewer and the European Project Officer.

4.2. Assessments

Let us now give the global feeling from the synthesis of the partner feedback (deliverable reports, e-mails, phone contacts, meeting at conferences, etc.).

Positive points:

- Global feedback is good
- To accede an up-to-date, industrial ATE is a very critical opportunity for electrical engineering education
- Training course is globally proved to be effective for student learning
- Technical collaboration with CRTC/LIRMM has been very satisfactory
- Average time for connecting Montpellier ATE is globally practicable even if strongly dependent on network traffic

Negative points:

- Training course is mainly designed to fulfil production test objectives. It is often necessary to add some introductory lectures to give the basics of test.
- The lack of physical contact with ATE is a little bit frustrating for students.

So, the global feedback from European partners about the implementation of these first training courses on digital test engineering is very good. The remote access has been proved to be very compliant and adaptable to local context. The opportunity of acceding to a real industrial test tool is fully appreciated. Depending of the level the training is given (MS, PhD) and taking into account the local educational context it may be necessary to add complementary lectures. The major drawback of the system is the lack of physical contact with the tester. In the future, it will be mandatory to add some video materials to compensate the student frustration of never seeing the tester. Finally, it is of interest to indicate that some European partner have created their own Web page to present the training course to their students.

4.3. Test education offer at European level

Starting from the situation of 2001, we have clearly extended the opportunity for a European student to have high-level education in test engineering. The original French network composed of 10 centres connected on the CRTC resources (Figure 3) is now a European network with 4 new academic centres of excellence.

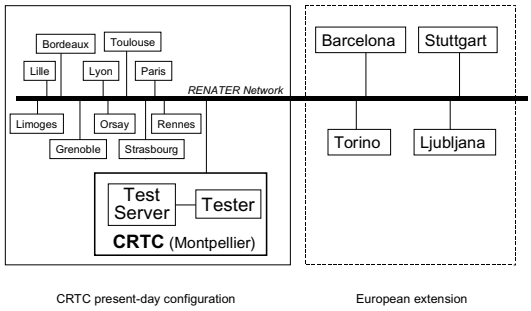

Figure 3: European network for test education

By the end of the project, test engineering knowledge dissemination now results in 3 European centres of competence in digital and mixed-signal testing and 3 European centres of competence in digital and memory testing (Table 2).

This configuration allows the per-year offer in test engineering education in Europe to be:

- 5 training courses in Digital Test
- 3 training courses in Mixed-Signal Test

- 3 training courses in Memory Test

Co-ordinated training scheduling should permit any European student to dispose several time slots for digital and/or specialised test training.

Table 2: Centres of competence in test engineering

Centre	Digital Test	M-S Test	Memory Test	Teaching Language
Montpellier (F)	X	X	X	French English
Barcelona (E)	X	X		Spanish English
Torino (I)	X		X	Italian English
Stuttgart (D)	X		X	German English
Ljubljana (SI)	X	X		Slovenian English

5. Conclusion and follow-up

The paper deals with a European experience of education in test engineering using resources mutualisation and remote testing facilities. The project addresses the problem of the shortage in microelectronics engineers aware with the new challenge of testing mixed-signal circuits for multimedia/telecom market. The project aims at providing test training facilities at a European scale in both initial and continuing education contexts. This was done by allowing the academic and industrial partners of the consortium to train engineers using the common test resources centre (CRTC) hosted by LIRMM (Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, France). CRTC test tools include an up-to-date/high-tech tester (Agilent 83000F330-t) that is fully representative of real industrial testers as used on production testfloors. At the end of the project, each new European centre (UPC, Polito, UST and JSI) is fully equipped and educated to permit a normal operating of about 16 trainees per year. The full success of the project has been validated during the mid-term and final meetings of the EuNICE-Test project. The interest of partner is such that each of them has planned to continue this network collaboration beyond the project. Indeed, some of them have already reproduced (UST) or scheduled (Polito) student training.

It is now planned to propose a new European project with an extension of the number of academic participants. Considering the level of the academic demand, a European network connecting about 10 centres may be easily envisaged. On the other side, regarding the strong European demand in SoC testing education it is also planned to drastically enhance the offer in terms of mixed-signal and memory testing training. Finally, contacts have established with other ATE makers in order to propose a more diversified and complete approach for test engineering education.

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