Design of Routing-Constrained Low Power Scan Chains

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Abstract

Scan-based architectures, though widely used in modern designs, are expensive in power consumption. Recently, we proposed a technique based on clustering and reordering of scan cells that allows to design low power scan chains [1]. The main feature of this technique is that power consumption during scan testing is minimized while constraints on scan routing are satisfied. In this paper, we propose a new version of this technique. The clustering process has been modified to allow a better distribution of scan cells in each cluster and hence lead to more important power reductions. Results are provided at the end of the paper to highlight this point and show that scan design constraints (length of scan connections, congestion problems) are still satisfied.

1. Introduction

The full-scan design is considered to be the best DfT discipline [2]. It can be completely automated using commercially available design tools. Over the years, it has gained wide-spread acceptability in system design environments and is now commonly used to test digital circuitry in integrated circuits (ICs) or System-on-Chip (SoC) cores. However, scan-based architectures are expensive in power consumption as each test pattern requires a large number of shift operations with a high circuit activity [2]. This elevated test power may be responsible for several kinds of problems: instant circuit damage, increased product costs, decreased system reliability, performance degradation, reduced autonomy of portable systems and decrease of overall yield. A survey of these problems is given in [3].

It is of course possible to reduce average power during scan testing by simply scanning at a lower frequency. However, this increases test application time. Another solution is to add logic to hold the output of the scan cells at a constant value during scan shifting [4]. The drawbacks of this approach are the area overhead and the performance degradation that it incurs, as well as the negative impact on the design flow. Some other solutions have been proposed recently to cope with the power problem during scan testing: low power ATPGs [5, 6], a scan path segmentation technique [7], a static compaction technique [8], two clock scheme modification techniques [9, 10], an interleaving scan architecture for multiple-scan circuits [11], a test data compression technique [12], two test scheduling techniques [13, 14], …

Actually, an alternative solution for minimizing power consumption during scan testing is to use scan cell ordering techniques. Scan cell ordering has been investigated first in [15] and more recently in [16] and [1]. In those techniques, the goal is to find a new order for connecting the scan elements of each scan chain such that the number of transitions generated in the scan chain during shift operations is minimized. In the latter technique [1], power-driven chaining of scan cells is done by taking care of the scan routing, which is one of the main concern when designing a scan chain in traditional DfT flows. The goal is to avoid congestion problems which have a negative impact on area overhead and timing closure [17, 18, 19, 20].

When designing power-optimized scan chains with the technique proposed in [1], a routing constraint is defined as the maximum length accepted for scan connections. The technique is a three-step process that can be applied once scan synthesis, placement and ATPG tasks have been performed. First, scan cells that belong to a same region of the chip are grouped together to form clusters. The number of clusters is a user-defined parameter established with respect to the routing constraint. Next, the power-driven scan cell ordering procedure presented in [16] is used to reorder scan cells in each cluster. Each cluster thus

contains a sub scan chain with minimum test power and has definite input and output scan cells. Finally, the output scan cell of each cluster is connected to the input of its closest neighbor according to a predefined cluster ordering. This technique for designing power-optimized routing-constrained scan chains offers numerous advantages. It works for any conventional scan design – no extra DfT logic is required – and can be easily inserted in any traditional DfT flow. It does not modify the fault coverage and the test time, and can be easily extended to deal with industrial designs that contain multiple scan chains and multiple clock domains. It provides significant reductions in terms of power consumption during scan testing, guarantees short scan connections and eliminates congestion problems.

In this paper, we propose a new version of this technique. Clustering in [1] was done by using a simple geographical criteria, irrespective of the number of scan cells contained in each cluster after clustering. Here, the clustering process has been modified to allow a better distribution of scan cells in each cluster and hence lead to more important power reductions. Experimental results are provided at the end of the paper to highlight this point and show that scan design constraints (length of scan connections, congestion problems) are still satisfied with this new version of the technique.

The remainder of the paper is organized as follows. In Section 2, we present the power-driven routing-constrained scan chain design technique proposed in [1] by detailing the three main phases of the process: clustering of the scan cells, scan cell reordering within a cluster, and cluster ordering. In Section 3, we describe the new clustering process and discuss the impact on the overall process. In Section 4, experimental results obtained on benchmark circuits are reported and discussed.

2. Scan chain design with minimum test power under routing constraint

2.1 Clustering operation

The clustering operation consists in grouping together cells that belong to a same region of the chip to further allow scan connections only between cells of a same region and hence avoid long scan connections in the design. Clustering also allows the degree of congestion to be reduced – by transforming the most congested area into several less congested sub-areas - and the total wire length to be minimized.

The number of clusters in the design is a user-defined parameter established with regard to the routing constraint. Formally, the stronger will be the constraint on the longest scan connection, the higher will be the number of clusters. On another hand, the higher will be the number of clusters,

the lower will be the reduction in test power on the final scan chain. In fact, with a high level of clustering, most of the scan cells are connected based on the closest neighbor criteria and only a few of them are connected according to test power optimization. Consequently, the best tradeoff between test power reduction and length of the longest scan connection has to be found by the user to determine the number of clusters for each design.
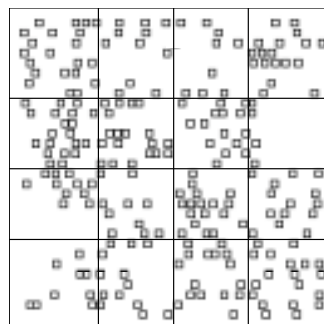

Figure 1: Clustering in circuit s9234 - 16 clusters

A lot of different solutions can be used to perform the clustering operation. As for defining the number of clusters, the way to make these clusters will be defined by the user considering parameters such as placement of flip-flops in the design (in order to deal with situations in which flip-flops are not equally distributed over the design), compatibility with the number of scan chains and clock domains, existence of one or more groups of pre-connected scan cells, etc. In [1], clustering is performed simply by defining a number of clusters and operating a squaring on the design with respect to this number. Each cluster is thus defined geographically with respect to the design and contains scan cells of a same region. Moreover, all the clusters have the same area but may contain a different number of scan cells. An example of the clustering process applied on circuit s9234 is reported in Figure 1. This circuit belongs to the ISCAS'89 family and has 228 scan flip-flops. In Figure 1, nodes represent the position of scan cells in the design obtained after synthesis with the tool "Silicon Ensemble" of Cadence Design System [21]. In this example, the number of clusters is 16 and the number of scan cells within each cluster ranges from 4 to 21.

2.2 Scan cell reordering within a cluster

Once clusters in the design have been defined, scan cell reordering within a cluster is done by using the power-driven scan cell ordering procedure presented in [16]. Here, the inputs to this procedure are i) the set of scan cells belonging to the considered cluster, and ii) the corresponding bits of these scan cell in the sequence of deterministic test vectors and output responses. For example, consider the test set shown in Figure 2, which is

composed of four test vectors (V_1 to V_4) and the corresponding four output responses (R_1 to R_4). This set of vectors is provided by an ATPG tool assuming a random initial order of the scan cells in the scan chain. In this example, scan cell 1, denoted as sc1, corresponds to bit 1 in each scan vector, scan cell 2, denoted as sc2, corresponds to bit 2, and so on. Consider now that four scan cells (sc2, sc3, sc5, sc6) among the n scan cells of the design are in the same region and hence belong to the same cluster Ck. In this example, the subset of bits to consider during scan cell reordering within cluster Ck will be the one highlighted in grey in Figure 2.

	sc1	sc2	sc3	sc4	sc5	sc6	sc7	…	scn
$V_1 =$	1	1	0	1	0	1	0	…	1
$R_1 =$	1	0	1	1	0	0	0	…	1
$V_2 =$	0	0	1	0	0	1	1	…	0
$R_2 =$	0	0	0	0	1	0	1	…	0
$V_3 =$	0	1	1	1	1	1	1	…	1
$R_3 =$	1	1	0	1	1	1	0	…	0
$V_4 =$	0	1	0	1	1	0	0	…	0
$R_4 =$	1	1	0	0	0	1	0	…	1

Cluster Ck

sc2	sc3
sc5	sc6

Figure 2: An example scan chain before reordering within a cluster

From the scan cells in the considered cluster and the corresponding subset of bits, it is then possible to determine the best scan cell order within the cluster. The best scan cell order is the one that assures a minimum toggling during scan operations within the cluster. It is obtained by applying the power-driven scan ordering procedure described in [16]. Applying this procedure to the above example leads to the following result: the final order of scan cells within cluster Ck is sc2-sc6-sc3-sc5, where sc2 is the input cell and sc5 the output cell of cluster Ck. Details to obtain this result can be found in [16]. The next step in this phase consists in performing scan cell reordering within another cluster, and to continue until all clusters in the design have been reordered.

2.3 Cluster ordering

The last phase of the scan chain design technique consists in connecting all clusters in the design so as to obtain the final scan chain. This is done by connecting the output scan cell of each cluster to the input of its closest neighbor according to a predefined cluster ordering. However, connecting clusters to form one or several scan chains can be done following different ways. The only requirements are i) to have each cluster connected to one of its closest neighbors to satisfy the constraint on the longest scan connection, and ii) to get through all clusters in the design to have all scan cells included in the final scan chain (s). Due to its exponential nature, solving this problem optimally is not a good option (this is an NP-hard problem). A better option is to use linear-time algorithmic solutions. As our main motivation in this work was more to

demonstrate the feasibility and efficiency of our approach than proposing a new algorithm for a graph traversal problem, we decided to implement a simple solution based on a given style of cluster ordering. This solution is depicted in Figure 3.a and consists in connecting clusters simply by following the *x*-axis direction. Of course, several other simple cluster orderings could be defined, for example by following the *y*-axis direction (Figure 3.b) or by considering the position of scan in and scan out pins (Figure 3.c). As for the clustering operation, the way to connect clusters to form scan chain(s) has to be defined by the user considering its design knowledge and constraints. In the rest of this paper, results are all based on the cluster ordering shown in Figure 3.a.
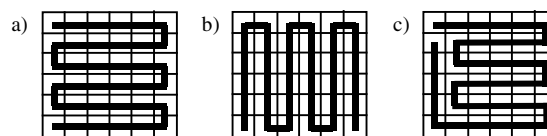

Figure 3: Different styles of cluster ordering

In order to estimate the global efficiency of our approach, we report in Figure 4.b the scan chain routing obtained on circuit s9234 with the technique presented in [1]. Compared to the scan routing obtained on the same circuit with the technique presented in [16] (see Figure 4.a), in which no routing constraint is considered, it is clear that the new solution greatly reduces the degree of congestion as well as the total wire length of the scan chain. The number of clusters in this design example is equal to 16, which allows to guarantee short scan connections. The reduction in average power consumed in the scan chain during scan testing is roughly equal to 12 %. This percentage is a test power comparison between the proposed scan ordering technique [1] and the layout-driven ordering produced by the tool "Silicon Ensemble" of Cadence, which is a routing-driven scan ordering solution.
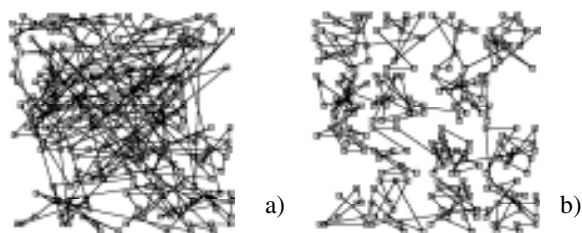

Figure 4: Power-optimized scan chain design s9234

3. New clustering operation

In this part, we propose an improved version of the technique presented in [1]. The improvement consists in defining a new clustering operation that allows to better distribute scan cells in each cluster. The goal is to have all

clusters containing more or less the same number of scan cells. Defining such kind of clustering allows to more efficiently reorder scan cells within each cluster and hence provide more important power reductions.

In [1], clustering is performed simply by defining a number of clusters and operating a squaring on the design with respect to this number. All the clusters have the same area but may contain a different number of scan cells. In the example shown in Figure 1 and concerning circuit s9234, the number of clusters is 16 and the number of scan cells within each cluster ranges from 4 to 21. In this context, it is foreseeable that the second step of the process (scan cell reordering within a cluster) will not be so efficient in terms of power reduction for clusters having a small number of scan cells. Now, if we consider a new clustering which is so that all the clusters have the same number of scan cells, it is more likely that the reduction in test power will be higher.
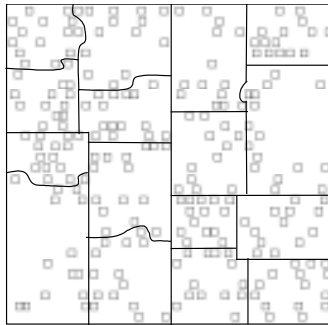

Figure 5: New clustering in circuit s9234 - 16 clusters

To highlight this point, consider again the same example circuit (s9234) and assume a clustering operation providing the result shown in Figure 5. Here, the number of clusters is still the same (16) than in the example of Figure 1. However, the number of scan cells is now roughly the same in each cluster (14 or 15). Considering this new clustering and applying the complete scan chain design process, the reduction in average power consumed during scan testing increases from 12.11% to 13.57%. The total wire length is roughly the same in both cases, demonstrating that the new clustering operation does not negatively impact the routing area. More details on these results are provided in Section 4. Additionally, it is shown in Section 4 that for all experimented circuits, the same conclusion can be drawn: a clustering process in which all clusters have the same number of scan cells provides better results than those obtained with the technique presented in [1].

A deeper observation of the results obtained on circuit s9234 leads to the following comment. Going from clusters composed of 4 scan cells to clusters composed of 14 (or 15) scan cells allows a more efficient reordering of scan cells (in terms of test power). However, the gain obtained

by this way could be eliminated by the loss observed when going from clusters composed of 21 scan cells to clusters composed of 14 (or 15) scan cells. In fact, results obtained on biggest benchmark circuits show that the gain is always higher than the loss, and that balancing the number of scan cells in each cluster always increases the performance of the power-driven routing-constrained scan chain design technique.

As for the original version of the technique, a lot of different solutions can be used to perform a clustering operation providing clusters with the same number of scan cells. Among the variety of solutions that can be imagined to perform such king of clustering, we have implemented a simple solution based on the use of a recursive algorithm. This algorithm is given in Figure 6, and has provided results discussed in Section 4. For every design, the algorithm provides clusters having either the same number of scan cells or numbers which differ of one unit.

```
/* Inputs */
FF = {FF0, FF1, …, FFn-1}; // Set of scan flip-flops
// For each flip-flop FFi, its position in the design, referenced by Xi and Yi, is known

nb_cluster ; // Desired number of clusters

/* Main Program */
…
nb_cut = log2 (nb_cluster) ;
Clustering (FF, nb_cut) ;
….
/* Function */
Clustering (FF', nb_cut') {
    if (nb_cut' > 0) {
        ΔX = Xmax - Xmin of FF' elements;
        ΔY = Ymax - Ymin of FF' elements;
        if (ΔX > ΔY)
            FF' elements are sorted by increasing order of X ;
        else
            FF' elements are sorted by increasing order of Y ;
        m = number of FF' elements ;
        FF1 = First m / 2 elements of FF' ;
        FF2 = FF' - FF1 ;
        Clustering (FF1, nb_cut'-1) ;
        Clustering (FF2, nb_cut'-1) ;
    }
    else
        FF' memorisation ;
}
```

Figure 6: New clustering algorithm

The algorithm described in Figure 6 works as follows. From the desired number of clusters (defined by the user), we first calculate the number of iterative cutting (or separating) operations to apply in the design (nb_cut). For example, if 16 clusters are desired, the number of cuttings will be 4 (4=$\log_2$16). After that, from the X and Y positions of all scan cells in the design, we calculate ΔX and ΔY which represent the maximum distance between two cells on either the X axis or the Y axis. We consider the max between ΔX and ΔY, and operate a first cutting operation in one of the two directions. At that moment, two groups of scan cells are formed in the design and a new iteration of

the algorithm can start. During this new iteration, the separating operation is performed again, such that four groups of scan cells are obtained at the end. The process continues similarly until the required number of clusters has been obtained.

4. Experimental results

The benchmarking process described here was performed on biggest circuits of the ISCAS'89 [22] benchmark suite. Power consumption in each circuit was estimated by using PowerMill of Synopsys [23], assuming a clock frequency equal to 200 MHz and a power supply voltage of 2.5 V. Experiments performed on each circuit have been done with technology parameters extracted from a 0.25μm digital CMOS standard cell library. In this section, we first recall the results obtained with the power-driven routing-constrained scan chain design technique presented in [1]. These results analyze the impact of clustering on the reduction in test power and on the overall scan chain routing. Next, we present results obtained with the new clustering operation and compare these results to those presented in [1].

First, structural characteristics and test parameters of the experimented circuits are reported in Table 1. All experiments are based on deterministic testing from the ATPG tool "TestGen" of Synopsys [24]. The missing faults in the fault coverage (FC) column are the redundant or aborted faults. The first part of Table 1 shows the number of scan cells and the number of gates for each benchmark circuit. The primary inputs and primary outputs were not included in the scan chain, but were assumed to be held constant during scan-in and scan-out operations. In the second part, we report the test length of each test sequence and the corresponding fault coverage. An important point to note is that the proposed scan optimization technique does not modify these values.

Circuit	# scan cells	# gates	# patterns	FC (%)
s5378	179	2225	145	99.05
s9234	228	4678.5	249	93.99
s13207	669	6395.5	354	98.99
s15850	597	7987	279	97.84
s35932	1728	16726.5	112	100

Table 1: Main features of the experimented circuits

Results obtained on the ISCAS'89 benchmark circuits are listed in the first part of Table 2. The results were obtained following the style of cluster ordering shown in Figure 3.a. For each circuit, we first report the average power reductions obtained during scan testing with respect to the number of clusters. These results are expressed in percentage and represent a test power comparison between the scan ordering technique proposed in [1] and the routing-driven ordering produced by "Silicon Ensemble". The main conclusion we can drawn from these results is

that power reduction decreases when the number of clusters increases. For circuit s9234, the power reduction ranges from 22.39 % with 1 cluster to 12.11 % with 16 clusters.

In the first part of Table 2, we also report the values of the scan wire length (WL - in μm) obtained with the technique presented in [1]. These results show that the total wire length of the scan chain decreases when the number of clusters increases, thus proving the efficiency of our clustering process. These results also show that it is possible to efficiently tradeoff between test power reduction and wire length minimization for big circuits. Thought not formally proven by experimental results, it is important to recall that the degree of congestion is always reduced and that short scan connections are always guaranteed with this technique.

	# clusters	[1]		New results	
		Power	WL	Power	WL
s5378	1	29.05 %	9.70E+4	29.05 %	9.70E+4
	2	19.17 %	7.20E+4	22.27 %	7.05E+8
	4	19.77 %	5.10E+4	21.38 %	5.35E+8
	16	12.25 %	3.40E+4	13.90 %	3.11E+8
s9234	1	22.39 %	1.20E+5	22.39 %	1.20E+5
	2	20.63 %	9.40E+4	21.59 %	9.66E+4
	4	15.78 %	8.20E+4	16.64 %	8.16E+4
	16	12.11 %	5.50E+4	13.57 %	5.63E+4
s13207	1	26.40 %	5.90E+5	26.40 %	5.90E+5
	2	19.50 %	4.40E+5	22.62 %	4.33E+5
	4	17.90 %	3.10E+5	20.57 %	3.13E+5
	16	14.40 %	1.80E+5	16.68 %	1.77E+5
s15850	1	17.80 %	5.00E+5	17.80 %	5.00E+5
	2	14.90 %	3.90E+5	16.23 %	3.99E+5
	4	15.20 %	2.70E+5	15.92 %	2.78E+5
	16	11.30 %	1.60E+5	11.76 %	1.64E+5
	32	8.90 %	1.30E+5	9.24 %	1.40E+5
s35932	1	19.60 %	3.30E+6	19.60 %	3.30E+6
	2	18.00 %	2.50E+6	19.42 %	2.45E+6
	4	16.60 %	1.60E+6	18.21 %	1.65E+6
	16	13.10 %	8.30E+5	14.79 %	8.32E+5
	32	11.10 %	6.20E+5	12.82 %	6.27E+5
	64	8.90 %	4.20E+5	10.43 %	4.34E+5

Table 2: Results obtained with the new clustering

In the second part of Table 2 (New results), we present the results obtained with the new clustering operation and compare these results to those given in the first part. For each circuit, we report and compare the percentage of average power reduction and the total wire length of the scan chain. In the technique presented in [1], a variable number of scan cells in each cluster is found after the clustering operation. In the new version of the technique, the number of scan cells in each cluster is always the same (±1). As can be observed, the reduction in average power consumed during scan testing is always higher with the new version of the technique. For example, assuming a number of clusters equal to 16, the power reduction goes from 12.25 % to 13.90 % for circuit s5378, from 12.11 %

to 13.57 % for circuit s9234, from 14.40 % to 16.68 % for circuit s13207, and so on. In the mean time, the total wire length of the corresponding scan chain remains more or less the same: sometimes, it is slightly longer (s9234, s15850, s35932), sometimes it is shorter (s5378, s13207). These results i) prove the effectiveness of the new clustering operation in the proposed scan design technique (although better algorithmic solutions could be imagined), and ii) show that the original technique presented in [1] is scalable and can be improved by modifying some procedures of the overall three-phase process. Among the possible solutions to further improve this technique, it is possible to optimally redefining the cluster ordering (step 3 of the overall process). Additional work can also be done to deal with more representative designs containing multiple scan chains, multiple clock domains and lockup latches.

A last comment on these results is about the time taken by the proposed technique to provide a power-optimized routing-constrained scan chain for a given circuit. This time is always less than one hour for the biggest ISCAS'89 benchmark circuits and increases only linearly with the number of scan cells in the circuit. Computations have been done on a SUN Enterprise 3000 station with 256 MB of RAM.

Note that the proposed technique works for any conventional scan design and can be easily inserted in any traditional DfT flow. The proposed technique does not modify the fault coverage and the test time, and can be easily extended to deal with industrial designs that contain multiple scan chains and multiple clock domains. It can also deal with huge designs containing several thousands (i.e. 500 K) of scan flip-flops. In this case, the design is partitioned into several blocks and each block is treated individually. For more details on this point, the reader can refer to [1].

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