A Novel DFT Technique to Test a Complete Set of ADC's and DAC's Embedded in a Complex SiP

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Abstract:
This paper proposes an original Design-For-Test (DFT) technique allowing the test of a complete set of converters embedded in a complex System-in-Package. The fundamental idea consists in implementing an additional circuitry allowing to interconnect the analogue ouputs of DAC's with the analogue inputs of ADC's. This globally results in an Analogue Network of interconnected Converters (ANC) that can be tested in a fully digital way. It is demonstrated that different configurations of the network can be described through a system of linearly independent equations. Solving the system of equations allows to determine the harmonic contribution of every converter in the network.

Keywords: *ADC, DAC, mixed-signal testing, DFT*

1 Introduction

Many electronic solutions are developed nowadays for portable applications, such as mobile phones, laptops, or audio MP3 players. The basic trend in these areas can be summarized as follows: more features in smaller volumes. The System-in-Package (SiP), a package that combines all the electronic components (digital ICs, analogue ICs, RF ICs, passive components or other elements) needed to provide a system or subsystem in one package, represents an opportunity to accelerate the development of highly miniaturized solutions.

Although the integration of many different functions into a single package offers several clear benefits, it implies significant test challenges. As an example, in the set-top-box project of Philips (STBSiP [1]), the test of the analogue blocks in the system represents up to 80% of the whole test effort while these blocs represent only 20% of the whole chip area.

When testing analogue blocks, the main difficulty comes from the performance requirements of the test instruments. Indeed, analogue testing is made of a long sequence of parameter characterization that is performed using very expensive instruments able to accurately measure analogue signals. In addition to these required expensive instruments, we should note that controllability and observability of deeply embedded analogue blocks are much reduced and the possibility of external testing may be limited. Indeed the number of pads are greatly reduced. Consequently the internal accessibility of the whole system decreases drastically. Also, as systems are operated at higher speeds, external testing becomes more susceptible to noise, crosstalk and probing problems.

To overcome these problems, several authors have proposed different Built-In-Self-Test (BIST) techniques where signals are internally generated and/or analysed [2-8]. Another possible and less expensive solution consists in using DFT techniques to internally transform the analogue signals into digital signals that are made controllable and observable from the chip I/Os [4, 9, 10, 11, 12]. So, only digital signals are externally handled by a non-expensive "digital" test equipment.

In the STBSiP product, like in most current mixed-signal systems, the converters are among the main components: 2 ADC's and 6 DAC's are embedded in the same SiP. The today specifications for these converters require a 10-bit resolution, but the next generations will make use of 12-bit converters. Testing this set of converters is a complex task requiring a long test time because of the problems of accessibility, signal integrity, accuracy of converter parameter measurements.

In this context, the authors propose an original DFT technique to test the whole set of embedded ADC's and DAC's. An extremely small circuitry is added to the original chip allowing a fully digital test approach for the whole set of converters.

In section 2, we give the fundamental principle of the test technique. In this section, the test of the set of n DAC's and m ADC's is made equivalent to a system of equations where the converter characteristics are the unknowns. A concept of duality is introduced between the system of equations to be solved and the possible configurations C(n,m) of the set of converters. Section 3 explores the space of possible configurations of the network and defines the corresponding equations. In section 4, the proposed technique is validated through simulations. Finally, section 5 gives some concluding remarks.

2 ANC Fundamental Principle

As often mentioned, analogue testing is classically oriented to performance characterization of a function under test. Performance characterization is obtained through a number of static and dynamic parameter estimations.

2.1 ADC and DAC testing

A crucial parameter, for ADC and DAC testing, is the Integral Non Linearity (INL). In addition, a number of dynamic parameters is also considered [10-14]. For most application domains, two key dynamic parameters are:

- Total Harmonic Distortion (THD),
- Spurious Free Dynamic Range (SFDR),

These dynamic parameters are computed from the harmonic values appearing in the output signal spectrum.

It means that a common way to estimate the dynamic parameters of a given converter is to perform a spectral measurement, i.e. to apply a 1-tone sine-wave to the converter input and compute the FFT of the output signal. The obtained harmonic values are then used to compute the dynamic parameters.

Note that even some static parameters may be derived from these harmonic values as demonstrated in [15, 16].

Given the above comments, it clearly appears that accurate measurement of the set of harmonic values of the output signal is a crucial point for any converter testing technique.

Considering the test of a single ADC using efficient instruments, it has been demonstrated in [15] that the output signal can be represented by (1). This equation includes an ideal sampled sine-wave x(n) and the sum of all the harmonic values introduced by the converter errors

$$s(n) = x(n) + \sum_{k \geq 0} Hconv_k \cos(k(\theta_n + \theta_0)) \qquad (1)$$

where n is the sample index, θ_0 the initial phase and $Hconv_k$ the k^{th} harmonic amplitude.

The above equation may also apply to the test of a single DAC, because the analogue output signal is converted into a digital sample set.

2.2 Analogue Network of Converters

Considering a complex system with several ADC's and DAC's, the objective of this paper is to measure the harmonic values $Hconv_k$ of each converter output signal using a fully digital way [17]. To be fully digital from an outside chip perspective, a simple circuitry is added to the system to:

- Realize the analogue sum of any combination of DAC outputs,
- Connect the resulting sum to any combination of ADC inputs.

This DFT technique requests a simple circuitry as illustrated in Figure 1. A simple OPAMP-based analogue adder can be used to implement the proposed DFT. The multiplexer control signal Ii allows to connect the corresponding DACi numbered i. In the same way, the multiplexer control signal Oj allows to connect the corresponding ADCj numbered j.

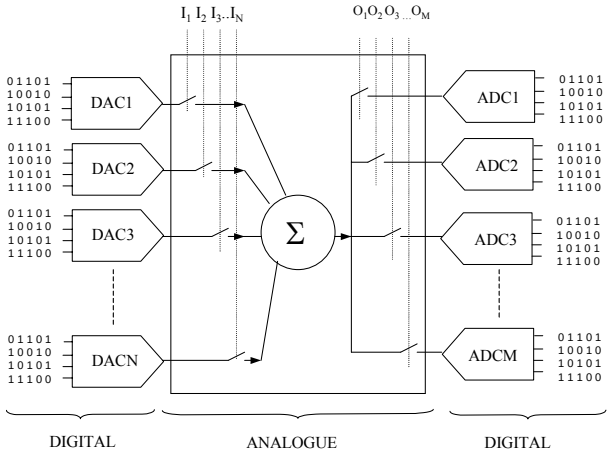

Figure 1: The ANC DFT technique

For a given combination of the control signals Ii and Oj in the configuration register, we obtain a given configuration of the ANC. When n DAC's are connected with m ADC's, this is called a configuration C(n,m).

Using configuration C(1,1), the spectrum of the output signal can be measured and we can extract the values of the harmonics. But in this case, the output signal includes both the errors of DAC1 and the errors of ADC1. In other words, the spectrum includes the harmonic contribution of DAC1 as well as the harmonic contribution of ADC1. So, due to the linearity of the system, we can write the following equation:

$$H_k^{measure} = H_k^m = Hdac1_k + Hadc1_k \qquad (2)$$

In this equation, we assume that the harmonic amplitudes created by the DAC are negligible with respect to the fundamental amplitude of the signal. Thus, we can consider the signal driving the ADC as a single tone signal. This working hypothesis will be verified in the validation phase described in section4.

Thanks to (2), we obtain a relation between the harmonic contributions of the different converters. Indeed, in (2), the left member is known; it is the k^{th} bin measured at the output of the ADC, while the right member represents the unknowns.

This example demonstrates the relationship between one configuration and its resulting equation, which leads to the fundamental idea of the ANC DFT technique. By using different configurations C(n,m) we are able to obtain a set of different equations. So, with an adequate set of configurations (i.e. system of equations), we expect to be able to fully determine the set of unknowns, i.e. the individual harmonic contribution of each converter.

The ANC DFT technique creates a duality between the configurations and the equations allowing the estimation of the harmonic contributions of each converter. The next section explores the space of possible configurations to obtain such a set of equations.

3 Configuration C(n,m)

The ANC principle consists in using different hardware configurations in terms of converter interconnections. Then, the idea is to find an adequate test setup to discriminate the influence of each converter on the final response. In practice, the only test setup parameters we can easily control are the phase and the amplitude of the digital stimulus. In this section, two configurations using DAC1, DAC2 and ADC1 are studied in order to discriminate their harmonic contributions.

3.1 Configuration C(1,1) at full-scale

The first configuration considered is made of a single DAC and a single ADC (Figure 2).

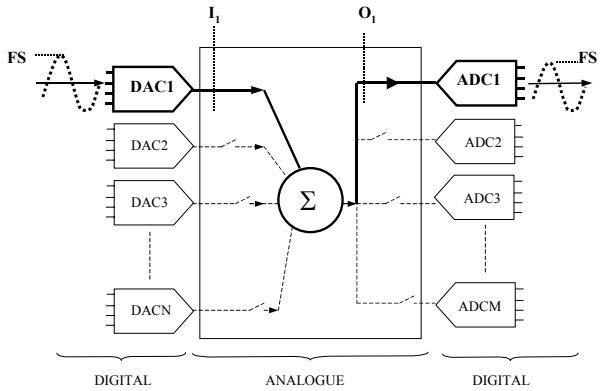

Figure 2: C(1,1) test configuration

According to the harmonic contribution model (2), the influence of the two data converters appears in the output sampled signal as shown in (3):

$$s(n) = x(n) + \sum_{k\geq 0}\left(Hdacl_k^{FS} + Hadcl_k^{FS}\right)\cos\left(k(\theta_n + \theta_0)\right) \quad (3)$$

where $Hdacl_k^{FS}$ and $Hadcl_k^{FS}$ are respectively the k^{th} harmonic contribution of the DAC1 and the ADC1 for an input signal reaching the converter full-scale. Notice that, in this study, we consider that all the converters have the same dynamic range.

If we only consider the three converters DAC1, DAC2 and ADC1, we generate two test setups. In a first step, a sine-wave is sourced from DAC1 to ADC1, with amplitude covering the converter full-scale. The expression of $H_k^{m,a}$, the amplitude of the k^{th} harmonic measured on the ADC1 output is given by:

$$H_k^{m,a} = Hdacl_k^{FS} + Hadcl_k^{FS} \quad (4)$$

In the second step, the test path goes through DAC2 and ADC1. The amplitude of the test signal still reaches the full-scale of the converters. Therefore, we obtain a second equation given by (5), where $H_k^{m,b}$ is the amplitude of the k^{th} harmonic measured on the ADC1 output.

$$H_k^{m,b} = Hdac2_k^{FS} + Hadcl_k^{FS} \quad (5)$$

At this point, we have three unknown parameters ($Hdacl_k^{FS}, Hdac2_k^{FS}, Hadcl_k^{FS}$) and only two equations (4 and 5) from two acquisitions.

One could think to play with the amplitude and phase of the input signal to establish new equations. Unfortunately, variations of these test setup parameters give no additional independent information to discriminate the influence of each converter on the final response. Indeed, the input signal phase has no influence on the converter harmonic contribution and even if the input signal amplitude A_{in} modifies the converter harmonic contribution ($Hdacl_k^{A_{in}} \neq Hdacl_k^{FS}$ if $A_{in} \neq FS$), each new acquisition would give a new equation but also two new unknown parameters ($Hdacl_k^{A_{in}}, Hadcl_k^{A_{in}}$).

To avoid this problem, the two DAC outputs can be added to establish a new configuration. This new configuration is called C(2,1) and is described in the next section.

3.2 Configuration C(2,1) at full-scale

The second hardware configuration is made up of two DAC's and one ADC. The input of the ADC is the sum of the two DAC outputs. A C(2,1) test configuration has already been described in [18]. But in this case, the objective is to test only the ADC, and DAC's must have higher resolutions than the ADC.

Unfortunately, considering three converters with the same resolutions and dynamic ranges, the sum of two full-scale signals from DAC1 and DAC2 with no relative phase shift is twice the converter full-scale and would saturate the ADC.

The solution to overcome this problem is to introduce a relative phase shift of $2\pi/3$ between the two input signals (Figure 3).

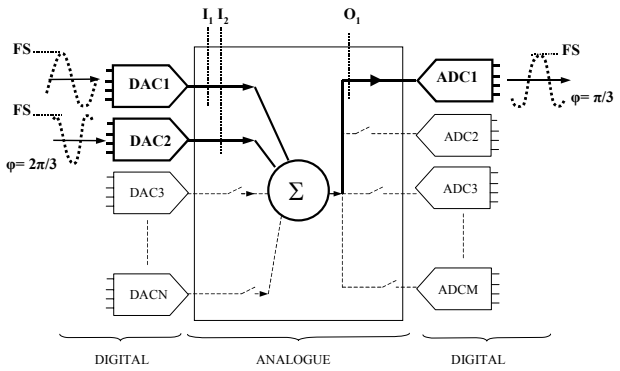

Figure 3: Test setup to obtain an additional equation.

The sum of the two DAC outputs is a full-scale signal; this property is mathematically explained by (6).

$$\cos\left(x + \frac{2\pi}{3}\right) + \cos(x) = 2\cos\left(x + \frac{\pi}{3}\right)\cos\left(\frac{\pi}{3}\right) = \cos\left(x + \frac{\pi}{3}\right) \quad (6)$$

As a consequence we obtain (7), the third equation:

$$H_k^{m,c} = Hdacl_k^{FS} + Hdac2_k^{FS}\cos(k2\pi/3) + Hadcl_k^{FS}\cos(k\pi/3) \quad (7)$$

where $H_k^{m,c}$ is the amplitude of the k^{th} harmonic measured on the ADC output. So finally, we obtain the following equation system for each k^{th} harmonic contribution:

$$\begin{cases} H_k^{m,a} = Hdac1_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,b} = Hdac2_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,c} = Hdac1_k^{FS} + Hdac2_k^{FS}\cos(k2\pi/3) + Hadc1_k^{FS}\cos(k\pi/3) \end{cases}$$

We finally obtain a system of 3 equations with the 3 converter harmonic contributions, which looks fine to determine the individual contributions. However, we are still unable to determine each converter contribution because the 3 equations are not always independent. Indeed, for some value of k and for the corresponding value of the cosines, the third equation happen to be a combination of the other two ones. In this case, we no longer have a 3-equation system and we are not able to discriminate the different harmonic contributions.

For the harmonic components of a prime order and greater than three (k=5,7,11…), the third equation is a linear combination of the two other ones. To improve the discrimination capability, we need more equations and so, we need to create new test configurations. A solution can be to modify the amplitude of the input signal. This concept is developed in the next sections.

3.3 Configuration C(1,1) at ½ full-scale

The second parameter we can control is the input signal amplitude. As previously explained, harmonic contribution depends on the stimulus amplitude ($Hdacl_k^{A_{in}} \neq Hdacl_k^{FS}$ if $A_{in} \neq FS$) and no trivial relationship exists between these different harmonic contributions. Consequently, the use of different amplitudes induces additional unknown parameters. Nevertheless, it also introduces new test setup possibilities that can be exploited to get additional independent useful information.

Practically, we have looked for a system of equations that allows the discrimination of the three converter harmonic contributions, $Hdacl_k^{FS}$, $Hdac2_k^{FS}$, $Hadcl_k^{FS}$ using test stimuli with amplitude at full-scale and amplitude at ½ full-scale.

The new third equation is the result of a test at ½ full-scale through DAC2 and ADC1.

The measured harmonics are the sum of DAC2 and ADC1 harmonic contributions for an input signal at ½ full-scale.

$$H_k^{m,c} = Hdac2_k^{FS/2} + Hadcl_k^{FS/2} \quad (8)$$

Thanks to this test, we add two new unknowns. In order to keep the same number of unknowns and increase the number of equations, it is possible to associate DAC1 at full-scale as described in the next section.

3.4 Configuration C(2,1) at ½ full-scale

½ full-scaled input signal has introduced two unknown parameters, $Hdac2_k^{FS/2}$ and $Hadcl_k^{FS/2}$. Three independent equations have already been established, (4) (5) and (8), so we need two additional independent equations. C(2,1) configuration with both amplitude and phase variations is used to establish these two equations. The 4th test setup involves a full-scale input signal on DAC1 and a ½ full-scale input signal on DAC2 with a π phase shift (Figure 4). The resulting signal at the ADC input is a sine-wave at ½ full-scale:

$$\cos(x) + \frac{\cos(x+\pi)}{2} = \cos(x) - \frac{\cos(x)}{2} = \frac{\cos(x)}{2} \quad (9)$$

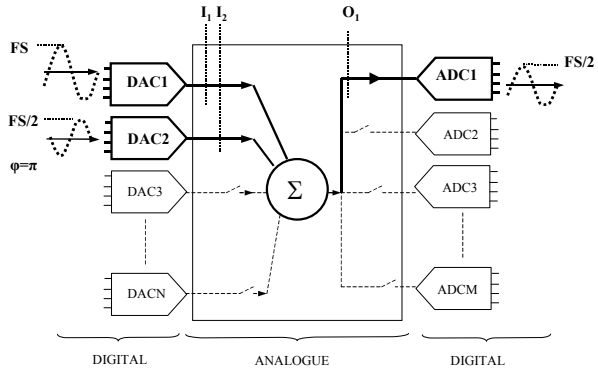

Figure 4: Test setup to obtain the 4th independent equation

The resulting equation is the sum of the harmonic contribution at full-scale of DAC1, the harmonic contribution at ½ full-scale of DAC2 balanced by the phase shift and the harmonic contribution at ½ full-scale of ADC1.

$$H_k^{m,d} = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k\pi) + Hadc1_k^{FS/2} \quad (10)$$

The 5th required test setup is very similar to the previous one. The input amplitudes are the same as before but they are relatively phase shifted of φ_1. The resulting signal at the ADC input is now a sine-wave at full-scale with a phase shift of φ_2.

$$\cos(x) + \frac{\cos(x+\varphi_1)}{2} = \cos(x+\varphi_2) \quad (11)$$

$$\text{with } \varphi_1 = \pi - 2\arccos\left(\frac{1}{4}\right) \quad \varphi_2 = \pi - \arccos\left(\frac{1}{4}\right) \quad (12)$$

The 5th equation then corresponds to the sum of the harmonic contributions balanced by their phase shift:

$$H_k^{m,e} = Hdacl_k^{FS} + Hdac2_k^{FS/2}\cos(k\varphi_1) + Hadcl_k^{FS}\cos(k\varphi_2) \quad (13)$$

In summary, the proposed test strategy is composed of five successive tests. Each test consists in an acquisition and a spectral analysis (with Fast Fourier Transform) to evaluate harmonic bins. We obtain a 5-equation system for each harmonic bin:

$$\begin{cases} H_k^{m,a} = Hdacl_k^{FS} + Hadcl_k^{FS} \\ H_k^{m,b} = Hdac2_k^{FS} + Hadcl_k^{FS} \\ H_k^{m,c} = Hdac2_k^{FS/2} + Hadcl_k^{FS/2} \\ H_k^{m,d} = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k\pi) + Hadc1_k^{FS/2} \\ H_k^{m,e} = Hdacl_k^{FS} + Hdac2_k^{FS/2}\cos(k\varphi_1) + Hadc1_k^{FS}\cos(k\varphi_2) \end{cases}$$

This system of independent equations is sufficient to calculate the values of the required harmonic contributions

($Hdac1_k^{FS}$, $Hdac2_k^{FS}$, $Hadc1_k^{FS}$). It allows thus a fully independent characterization of the three converters of the C(2,1) configuration in terms of harmonic contributions.

3.5 Configuration C(n,m)

Thanks to the converter characterization obtained from the C(2,1) configuration, it seems easy to test every other converter embedded in the same complex chip.

The idea is to use one of the three previously characterized converters as a measurement instrument whose non-ideal features are well known.

Test time directly depends on the number of required acquisitions. The first step of the test procedure needs five acquisitions to test three devices. Then using a C(1,1) test configuration (cf 3.1) with an already characterized converter, considering (4) there is only one unknown variable: the harmonic contribution of the uncharacterized converter. As a consequence we need only one additional acquisition to test this converter. So, the number of acquisitions for a complex chip with n DAC's and m ADC's is only of n+m+2 acquisitions without any external analogue equipment requirement.

Moreover, because only digital ATE resources are required, it is conceivable to test several converters at the same time. Consequently, after the first step, each new step could use simultaneously all available characterized converters as measurement instruments. In this configuration, the testing time could be drastically reduced.

4 Validation

A number of experiments based on simulation have been conducted to validate the proposed approach. The converter model used for simulation is first introduced, then the simulation setup is defined, and finally experimental results are presented. The performance of the proposed test strategy is discussed in terms of estimation error on the harmonic components and on the dynamic parameters.

4.1 Data converter model

To simulate the test strategy, we need to establish a model that takes into account the effects of the converter non-idealities. Three main sources of errors will be considered, i.e. the sampling jitter of the converter, the non-linearities of its transfer function and the thermal noise.

Let us consider an input sine-wave passing through an ideal converter. This sampled signal can be expressed (in LSB unit) by:

$$x(n) = 2^N \left(\frac{V_0}{V_{FS}} \right) \cos(\theta_n + \theta_0) + 2^N \left(\frac{V_{DC}}{V_{FS}} \right) \qquad (14)$$

where N and V_{FS} respectively represent the number of bits and the full-scale voltage of the converter, V_0 and V_{DC} respectively correspond to the amplitude and the DC component of the input sine-wave, and θ_0 and θ_n are respectively the initial and nominal sampling phase of the signal. The nominal sampling phase is given by:

$$\theta_n = 2\pi \left(\frac{P}{M} \right) n \qquad (15)$$

where M is the number of samples and P the number of periods in the record.

Let us now introduce the sampling jitter of the converter. Essentially, it is a phase noise that changes the ideal sampling time. The resulting deteriorated signal is given by:

$$r(n) = 2^N \left(\frac{V_0}{V_{FS}} \right) \cos(\theta_n + J_t + \theta_0) + 2^N \left(\frac{V_{DC}}{V_{FS}} \right) \qquad (16)$$

where $J_t = 2\pi f_0 \delta_t$, with f_0 the frequency of the input signal and δ_t a centred Gaussian noise. According to [5] and thanks to a Taylor series development, the jitter contribution can be separated from the input signal expression in (16). Finally, considering an additional thermal noise we obtain the following expression:

$$r(n) = x(n) + \varepsilon(n) \qquad (17)$$

where ε(n) is the sum of the noise induced by the sampling jitter and the thermal noise (N_{Th}). The thermal noise is usually modelled by a centred Gaussian noise.

$$\varepsilon(n) = 2^N \frac{V_0}{V_{FS}} J_t \sin(\theta_n + \theta_0) + N_{Th} \qquad (18)$$

The second significant source of errors that has to be considered is the non-linearity of the converter transfer function. A common approach to analytically model the converter INL is based on polynomial approximation [5, 15, 20]. However, such modelling does not permit to describe the sharp transitions usually encountered for actual INL. In order to alleviate this drawback, we choose a different approach which consists in using "true" INL curves extracted from measurements on real data converters.

Consequently, let us consider s(n) the signal deteriorated by the two types of errors:

$$s(n) = [\ r(n) + \mathrm{INL}([r(n)])\ ] \qquad (19)$$

where INL(x) is a non-linearity curve measured through histogram testing of a real converter. This non-linearity curve is indexed by the rounded signal [r(n)], including the sampling jitter effect The complete equation is rounded to model the quantization effect.

Equation (19) is the equation that models the deterioration of a sine-wave signal passing through a converter affected by sampling jitter, transfer function non-linearities and thermal noise. This equation has been used for the simulations described in the following sections.

4.2 Simulation setup

To validate the proposed test strategy, we have conducted a number of simulations considering data converters of the same resolution and sampling frequency. The objective is to compare the values of the harmonic components

evaluated using the proposed strategy to the ones obtained using a classical stand-alone test.

At first, we have performed histogram tests on 15 real data converters to extract INL curves (PHILIPS TDA9910). Using equation (19), we can therefore model 15 different converters. Then we have conducted two sets of simulation:

- At first, we have considered each data converter in a stand-alone configuration to get reference values.
- Then, we have considered five different C(2,1) configurations, each one involving three different converters. For each C(2,1) configuration, we have simulated the test algorithm described in section 3.4.

4.3 Results and discussion

As an example, Figure 5 presents the results obtained for one converter. The amplitude of the harmonic components evaluated using the C(2,1) configuration (black bins) are compared to the amplitude of the harmonic components computed using the classical stand-alone test configuration (grey bins).

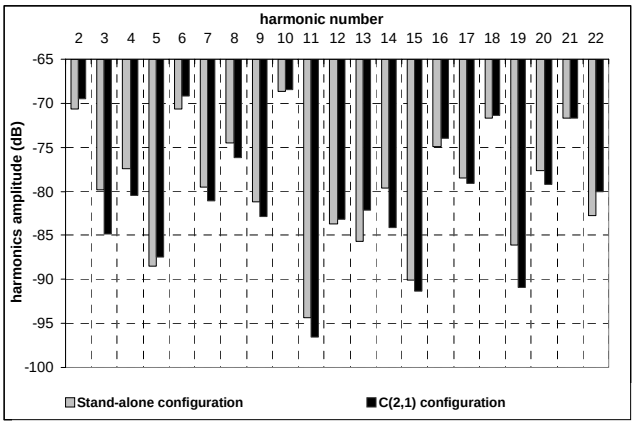

Figure 5: Estimation of the first 20 harmonics of one converter vs. reference values

The maximum estimation error observed on the amplitude of the first 20 harmonic components is about 5dB. However, it is worth pointing out that this error is observed for a harmonic component of very small amplitude (≈-85dB). Considering only the major harmonic components with amplitude higher than -75dB, the observed estimation error remains inferior to 2dB. These results show the efficiency of the proposed strategy that permits an accurate evaluation of the converter harmonic components.

Similar simulations have been performed for the complete set of 15 different converters. Results are summarized in Table 1 that reports the maximum estimation error observed on the amplitude of the first 20 harmonic components for the different converters. Note that the results have been classified in three different ranges according to the amplitude of the harmonics:

- Range 1 corresponds to harmonic higher than -75dB.
- Range 2 corresponds to harmonic higher than -85dB and lower than -75dB.
- Range 3 corresponds to harmonic lower than -85dB.

It should be reminded that the harmonics will be later used to compute the dynamic parameters of the converters. It is obvious that harmonics belonging to range 1 will have a significant impact on the dynamic parameters, while harmonics in the third range are so small that they will have almost no impact on the values of the dynamic parameters.

	H>-75dB	-75dB>H>-85dB	H<-85dB
Converter#1	0.28	-7.99	-16.04
#2	-0.64	7.58	-19.23
#3	0.36	7.62	3.55
#4	-0.26	6.1	-8.49
#5	-0.25	0.91	11.60
#6	-0.33	-4.89	5.73
#7	0.24	-3.73	-18.16
#8	-0.39	2.10	-22.31
#9	0.25	8.00	6.58
#10	3.50	1.03	3.70
#11	-0.10	-2.10	-2.96
#12	-0.29	-1.02	22.9
#13	-0.37	-1.2	4.59
#14	0.14	3.17	14.20
#15	-0.45	-4.84	-5.42

Table 1: Maximum estimation errors vs. the amplitude range of the harmonic components (in dB)

Analyzing the results in Table 1, it can be observed that the harmonics in range 1 with high amplitude exhibit the lowest estimation error. On the complete set of 15 converters, the maximum estimation error remains:

- Below 3.5dB for harmonic components belonging to range 1,
- Below 8.00dB for harmonic components belonging to range 2,
- Below 22.9dB for harmonic components belonging to range 3.

Moreover, we observed that the estimation error is globally proportional to the inverse of the harmonic amplitude and that harmonics remain in the same range even considering the error estimation (e.g. range 3).

As a conclusion, we can say that the largest errors are made on harmonic in range 3, i.e. the harmonics with a very low impact on the computation of the dynamic parameters.

To further validate the efficiency of the proposed strategy, we have evaluated two dynamic parameters, the THD and the SFDR, for the 15 different converters. These parameters are evaluated from the spectral distribution. Results are summarized in Table 2, which reports the THD/SFDR values computed using the stand-alone configuration and the THD/SFDR values computed using the C(2,1) configuration, and the corresponding estimation error.

Conveter Number	Wanted THD (dB)	THD estimation (dB)	THD error (dB)	Wanted SFDR (dB)	SFDR estimation (dB)	SFDR error (dB)
#1	-59.1	-59.0	-0.1	68.8	69.3	-0.5
#2	-58.0	-57.9	-0.1	69.3	69.9	-0.6
#3	-58.2	-58.2	0	67.9	67.5	0.4
#4	-64.3	-63.9	-0.4	69.4	68.9	0.5
#5	-66.7	-66.9	0.2	70.9	71.1	-0.2
#6	-61.7	-58.8	-2.9	63.4	64.2	-0.8
#7	-48.1	-48.1	0	67.1	66.3	0.8
#8	-62.7	-62.2	-0.5	65.4	64.7	0.7
#9	-60.7	-60.9	0.2	64.9	65.5	-0.6
#10	-59.7	-59.7	0	62.2	62.2	0
#11	-61.5	-61.8	0.3	64.0	65.1	-1.1
#12	-61.6	-61.4	-0.2	62.8	62.8	0
#13	-70.4	-69.6	-0.8	71.1	67.4	3.7
#14	-55.5	-55.6	0.1	65.0	65.0	0
#15	-64.0	-63.6	-0.4	68.6	68.4	0.2

Table2: THD & SFDR estimation errors

Analyzing these results, it can be seen that the strategy enables an accurate measurement of both dynamic parameters, with an estimation error that remains below 3.7dB for the 15 different converters considered in the experiment. Note that such a low estimation error actually corresponds to the accuracy range that we can expect for the measurement of these parameters taking into account fluctuations in the test environment. Indeed, the reference values computed here with the stand-alone configuration are obtained considering ideal test instruments. However in a real environment, the repeatability of the measurements is impacted by unavoidable fluctuations in the test instrumentation. As a result, it is classical to observe dispersions in the range of 5 to 10% when measuring the THD and SFDR parameters in a real environment.

5 Conclusion

In this paper, we have presented a new concept called "Analogue Network of Converters" (ANC) that can be used to test distortion of embedded converters. Using this approach we have demonstrated that a fully digital test of the converters can be performed thus decreasing significantly the cost of the test.

Moreover in the case when CPU resources (DSP) are already present in the chip, it is possible to implement a complete BIST setup.

Our test strategy is well suited to SiP components which are usually complex, including several DAC's and ADC's.

The next step presently under development consists in a validation by an experimentation and an evaluation of the robustness by varying several parameters like: amplitudes of different converters or different data converter resolutions.

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