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Abstract:
Nowadays a lot of complex circuits as SiP and SoC contain several ADCs and DACs in one package. The performances and number of these converters are continuously increasing, leading to ever higher test costs. This paper presents an experimental validation of a new concept called "Analogue Network of Converters" that permits to reduce drastically the testing time of these converters and requires only a low cost fully digital ATE.

1 Introduction

The convergence of both communication and consumer markets increases silicon usage and needs for integrating various analogue or mixed-signal blocks into a single System-in-Package (SiP) or System-on-Chip (SoC): mobile phones, laptops, audio players… Figure 1 gives an example of such a complex mixed-signal system integrated into a single package. The integration of many different functions into a single package offers several clear benefits but, on the other hand, implies very significant test challenges. As an illustration of these difficulties, examples are usually reported where the test of the analogue blocks in the system may represent up to 90% of the whole test effort while these analogue blocks only represent 10% of the whole chip area.

Analogue blocks are usually tested with respect to their specified parameters. Consequently, the main difficulty comes from the performance requirements on the test instruments. Indeed, analogue testing consists in a long sequence of parameter characterization that is performed using very expensive instruments able to accurately measure analogue signals. In addition to these required expensive instruments, we should note that controllability and observability of deeply embedded analogue blocks are limited and the possibility of external testing may be limited. Also, as signals become faster and systems are operated at higher speeds, external testing becomes more susceptible to noise, crosstalk and probing problems.

To overcome these problems, several authors have proposed different BIST techniques where signals are internally generated and/or analysed [1-7]. Another possible and less expensive solution consists in using DFT techniques to internally transform the analogue signals into digital signals that are made controllable and observable from the chip I/Os [3,8,9]. As a result, only digital signals are externally handled by an inexpensive "digital" test equipment (Low Cost Tester).

In current systems, it should be mentioned that converters (Analogue to Digital Converters–or ADCs– and Digital to Analogue Converters –or DACs) are among the main components of any mixed-signal chip. Nowadays, many ADCs and DACs may be implemented in a complex SoC or SiP. For instance, Figure 1 proposes a microphotography of the PNX8327 device for set-top box applications (digital audio and video decoder) where 2 ADCs and 7 DACs are embedded in the same SiP. Basically, two strategies may be used for testing a complex system. The first approach consists in testing the system per block. In such a case, access and control of the embedded ADCs and DACs are often difficult. The alternative is the path-based one, where the whole chain is tested, for example the transmitter or the receiver, from RF to digital blocks [10]. Although this approach can guarantee the functionality of the system, it does not give any information about the quality and the performances of the embedded converters and other analogue blocks.

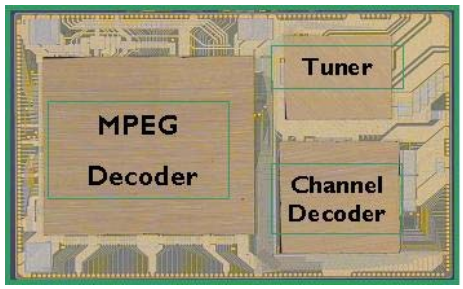

Figure 1: SiP for set-top box applications

In this context, this paper proposes an original DFT technique called "Analogue Network of Converters" (ANC) that permits to test the whole set of embedded ADCs and DACs. An extremely small circuitry is added to the original chip allowing to apply a fully digital test approach to the System-in-Package/System-on-Chip.

In the remainder of the paper, section 2 gives the fundamental principle of the ANC technique. In this section, the test of a set of n DACs and m ADCs is associated to a system of equations where the converter characteristics are the unknowns. Section 3 explores the space of possible configurations of the network and defines the corresponding equations. In section 4, the proposed ANC technique is validated through simulations and

measurements. Finally, section 5 gives some concluding remarks.

2 ANC Fundamental Principle

2.1 DAC and ADC testing

As often mentioned, analogue testing is classically oriented to performance characterization of a function under test. Performance characterization is obtained through a number of static and dynamic parameter estimations.

A crucial parameter, for ADC and DAC testing, is the Integral Non Linearity (INL). In addition, a long list of dynamic parameters is also considered [9,10,11]. For most of the application domains, two of the key dynamic parameters are:

- Total Harmonic Distortion (THD),
- Spurious Free Dynamic Range (SFDR),

The INL is derived [10] and the THD and SFDR computed [9] from the harmonic values appearing in the spectrum of the output signal.

That means that a very common way to estimate the dynamic parameters of a given converter is to perform a spectral measurement, i.e. to apply a single tone sine wave signal to the converter input and compute the FFT of the output signal. The obtained harmonic values are then used to compute the dynamic parameters.

Considering for instance the test of a single ADC using accurate instruments, it has been demonstrated [10] that the output signal can be represented by (1). This equation includes an ideal sampled sine wave x(n) and the sum of all the harmonic values introduced by the converter errors.

$$s(n) = x(n) + \sum_{k\geq 0} H_k^{converter} \cos(k(\theta_n + \theta_0)) \quad (1)$$

In equation (1), n is the sample index, θ_0 the initial phase shift, $H_k^{converter}$ the amplitude of the k^{th} harmonic and θ_n is the nominal sampling phase

$$\theta_n = 2\pi\left(\frac{P}{M}\right)n \quad (2)$$

where M is the number of samples and P the number of periods in the record.

Given the above comments, it clearly appears that accurate measurement of the set of harmonic values $H_k^{converter}$ of the output signal is a crucial point for any converter testing technique. The above equation may also apply to the test of a single DAC, because the analogue output signal is converted into a digital sample set before the FFT analysis.

2.2 Analogue Network of Converters

Considering a complex system with several ADCs and DACs, the objective of this paper is to measure the harmonic values $H_k^{converter}$ of each converter output signal using a fully digital way [12]. To be fully digital from an outside chip perspective, a very simple circuitry is added to the system:

- to realize the analogue sum of any combination of DAC outputs,

- to connect the resulting sum to any combination of ADC inputs.

This DFT technique requests an extremely simple and limited circuitry as illustrated in Figure 2. A simple OPAMP-based analogue adder can be used to implement the proposed DFT. The multiplexer control signal Ii allows to connect the corresponding DACi. In the same way, the multiplexer control signal Oj allows to connect the corresponding ADCj.

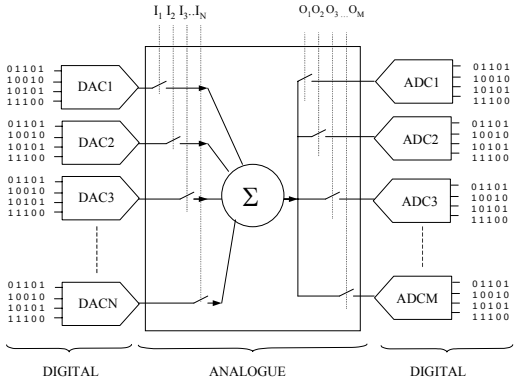

Figure 2: The ANC DFT technique

When n DACs are connected with m ADCs, this is called a configuration C(n,m). Using configuration C(1,1), the spectrum of the output signal can be computed and we can extract the values of the harmonics $H_k^{C(1,1)}$. But in this case, the output signal includes both the errors of DAC1 and the errors of ADC1. In other words, the spectrum includes the harmonic contribution of DAC1 as well as the harmonic contribution of ADC1. So, due to the linearity of the system, we can write the following equation:

$$H_k^{measure} = H_k^m = \left(H_k^{DAC1} + H_k^{ADC1}\right) \quad (3)$$

In this equation, we assume that the harmonic amplitudes created by the DAC are negligible with respect to the fundamental amplitude of the signal. Thus, we can consider the signal driving the ADC as a single tone signal. This working hypothesis will be verified in the validation phase described in section 4.

Thanks to equation (3), we obtain a relation between the harmonic contribution of the different converters. Indeed, in equation (3), the left member is known (it corresponds to the amplitude of the k^{th} spectral bin measured at the output of the ADC), while the right member represents the unknowns.

This small example demonstrates the relationship between one configuration and its resulting equation, which leads to the fundamental idea of the

ANC DFT technique. By using different configurations C(n,m) we are able to obtain a set of different equations. So, with an adequate set of configurations (i.e system of equations), we expect to be able to fully determine the set of unknowns, i.e. the individual harmonic contribution of each converter.

The ANC DFT technique creates a duality between the configurations and the equations allowing the estimation of the harmonic contributions of each converter. The next section explores the space of possible configurations to obtain an appropriate set of equations.

2.3 New test method using C(1,1) and C(2,1) configurations

The ANC principle consists in using different hardware configurations in terms of converter interconnections. Then, the idea is to find an adequate test setup to discriminate the influence of each converter on the final response. In practice, the only test setup parameters we can easily control are the phase and the amplitude of the digital stimulus. In this section, two configurations, using DAC1, DAC2 and ADC1, are studied in order to discriminate their harmonic contributions.

In summary, the proposed test strategy, described in [12], is composed of five successive tests. Each test consists in an acquisition and a spectral analysis (by Fast Fourier Transform) to evaluate harmonic bins. We obtain a 5-equation system for each harmonic bin:

$$\begin{cases} H_k^{m,a} = Hdac1_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,b} = Hdac2_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,c} = Hdac2_k^{FS/2} + Hadc1_k^{FS/2} \\ H_k^{m,d} = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k\pi) + Hadc1_k^{FS/2} \\ H_k^{m,e} = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k\varphi_1) + Hadc1_k^{FS}\cos(k\varphi_2) \end{cases} \quad (4)$$

$$\text{with } \varphi_1 = \pi - 2\arccos\left(\frac{1}{4}\right),\ \varphi_2 = \pi - \arccos\left(\frac{1}{4}\right)$$

The three first tests use a C(1,1) configuration. The two first equations result from a test at full-scale (FS) through DAC1 and DAC2 respectively, then ADC1 (the converters are considered of same analogue full-scale range). The third equation results from a test at half full-scale (FS/2) through DAC2 and ADC1.

The two last tests use a C(2,1) configuration. The two last equations result from tests that combine the outputs of the two DACs. The output range of DAC1 is full-scale while the output level of DAC2 is half full-scale. The two DAC input sine-waves are relatively phase shifted, in order to obtain output signal with a relative control phase shifted. After the sum of this relative phase shifted DAC output, we obtain the following particular amplitudes of the input signal of ADC1:

- full-scale for the fourth test
- half full-scale for the fifth test.

This system of independent equations is sufficient to calculate the values of the required harmonic contributions ($Hdac1_k^{FS}, Hdac2_k^{FS}, Hadc1_k^{FS}$). It allows thus a fully independent characterization of the three converters of the C(2,1) configuration in terms of harmonic contributions.

2.4 Configuration C(n,m)

Thanks to the converter characterization obtained from the C(2,1) configuration, it seems easy to test every other converter embedded in the same complex chip.

The idea is to use one of the three previously characterized converters as a measurement instrument whose non-ideal features are now well known.

The first step consists in using the C(2,1) configuration to characterize the three first converters (ADC1, DAC1 and DAC2). Then, DAC1 can be used to characterize the harmonic contribution of each ADCi in the chip by using only one digital stimulus at full-scale to obtain the following additional equation:

$$H_k^{m,j} = Hdac1_k^{FS} + Hadci_k^{FS} \quad (5)$$

In the same way, ADC1 can be used to characterize all the DACs present within the system.

Concerning test time, it directly depends on the number of required acquisitions. The first step of the test procedure implies five acquisitions to test three devices. Then, only one additional acquisition per device under test is needed. So, the number of acquisitions for a complex chip with n DACs and m ADCs is only of n+m+2 acquisitions without any external analogue equipment requirement.

Moreover, because only digital ATE resources are required, it is conceivable to test several converters at the same time. Consequently, after the first step, each new step could use simultaneously all available characterized converters as measurement instruments. In this configuration, the testing time could be drastically reduced.

3 Validation

Simulation results have provided a first validation of the proposed method [12]. In this section, we show the results of the first experiments, evaluating the effectiveness of the method in the estimation of ADC distortion components. The experimental setup is first introduced, then the experimental protocol is described and finally the results are presented. The performance of the

proposed test strategy is discussed in terms of difference found on SFDR and THD results.

3.1 Experimental setup

In order to experiment the test strategy, we need at least two DACs and one ADC to establish a C(2,1) configuration (Figure 3).

For a faster implementation, we have decided to carry out the first experiments using a 2-channel Arbitrary Wave Generator (AWG) to play the role of the two DACs. Each channel is composed of a 12-bit DAC and an amplifier.

In addition, two low-pass filters are placed between the AWG outputs and the adder in order to reduce the second and third harmonics generated by the AWG. These two harmonics are too high to emulate correctly two 12bit DACs.

A combiner/splitter HP11667B is used to sum the signals.

The stand-alone ADC used for experimentation is a TDA9910 Philips

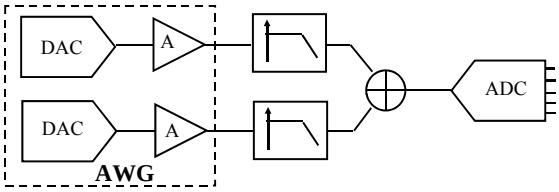

Figure 3: Experimental setup

For comparison, reference measurements have been collected using a standard setup, as shown in Figure 4.

The test signal is generated by an AWG, and the spurious components (noise and harmonics) are removed by a band-pass filter centred on the test frequency.

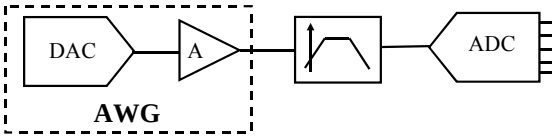

Figure 4: Reference measurement setup

3.2 Experimental protocol

The objective is to compare the values of the harmonic components of the ADC evaluated using the proposed strategy to the ones obtained using a standard test configuration. To this purpose, we have conducted this experiment on 3 different ADC samples, chosen in a THD range from –70 to -63dB. Each data acquisition is achieved 20 times and averaged, in order to reduce the noise influence.

The harmonic components are individually evaluated, from the 2nd to the 10th order, then the THD and SFDR parameters, given respectively by (6) and (7), are calculated.

$$THD(dB) = 10 * \log_{10}\left(\frac{\sum_{k=2}^{10} H_k^2}{H_1^2}\right) \quad (6)$$

$$SFDR(dB) = 20 * \log_{10}\left(\frac{H_1}{\max(H_k)}\right) \quad (7)$$

where H_1 is the amplitude of the fundamental and H_k the amplitude of the k^{th} harmonic.

3.3 Experimental results

The results presented in Table 1 are experimental results for one ADC. The harmonics 2 to 10 have been measured by the classical method as well as the new method. The last column corresponds to the difference between the two measures.

Harmonic number	*Reference values (dB)*	*Method results (dB)*	*Measurement difference (dB)*
2	-69.2	-68.1	-1.1
3	-67.9	-67.8	0.1
4	-72.5	-70.8	-1.7
5	-70.8	-71.8	1.0
6	-95.7	-86.2	-9.5
7	-78.2	-79.4	1.2
8	-102.9	-97.6	-5.2
9	-78.7	-78.9	0.2
10	-92.0	-86.7	-5.3

Table 1: First harmonics estimation for one ADC

From the results shown in Table 1, we can conclude that the new method correlates with the reference when the level of the harmonic is higher than –80dB, which corresponds to the level of the highest noise component of this device.

Table 2 and 3 give a comparison between the two methods, concerning THD and SFDR measurements.

To estimate the performances of the new method, three components with different characteristics have been chosen: a component with a high quality THD (THD=-70.4dB), another component with THD at the tolerance limit (THD=-66.4dB) and a component that wouldn't pass the test (THD=-63.2dB, beyond device specifications).

ADC number	*THD reference (dB)*	*THD measured (dB)*	*Measurement difference (dB)*
1	-63.2	-63.6	0.4
2	-66.4	-66.0	-0.4
3	-70.4	-69.4	-1

Table 2: THD estimation for 3 ADCs

ADC number	*SFDR reference (dB)*	*SFDR measured (dB)*	*Measurements difference (dB)*
1	67.8	65.3	2.5
2	66.9	66.9	0
3	70.7	72.1	-1.4

Table 3: SFDR estimation for 3 ADCs

Analysing the results of Tables 2 and 3, the maximal difference between the two evaluation methods is 1dB for THD and 2.5dB for SFDR. Correlating the results of harmonic measurements represents a big challenge, because of their high sensitivity to the variations of the input sine wave amplitude [13]. Due to this sensitivity a maximum error of reproducibility of +/-3dB on individual harmonics and SFDR is accepted for a 12-bit resolution. For THD parameter, a +/-1.5dB variation is generally accepted. As a consequence, the results obtained by the new method are very acceptable and promising.

4 Conclusion

This paper has introduced the novel concept of "Analogue Network of Converters" (ANC) to test distortion of embedded converters. Thanks to this approach, we have demonstrated that it is possible to solve the problem of expensive tester instruments by achieving a fully digital test. Moreover, by using an embedded DSP, it could be possible to implement a complete BIST setup. This is a breakthrough in the domain of BIST strategy and data converter testing.

Our test strategy is well suited to SiP components. Indeed, they are complex components containing several DACs and ADCs. In addition to this complexity of design, there is a complexity of test due to reduced block observability and controllability.

Further validations would be achieved on a set of converters embedded in a complex component. It would consist in an evaluation of the robustness by varying several parameters like: different amplitudes between converters or various data converter resolutions.

References:

[1] M.Toner, G.Roberts, **"A BIST scheme for an SNR test of a sigma-delta ADC"**, Proc International Test Conference, Pp:805 – 814, 1993.

[2] M.Toner, G.Roberts, **"A BIST Technique for a Frequency Response and Intermodulation Distortion Test of a Sigma-Delta ADC"**, Proc IEEE VLSI Test Symposium, pp:60 – 65, 1994.

[3] M.J.Ohletz, **"Hybrid Built In Self Test (HBIST) for Mixed Analog/Digital Integrated Circuits"**, Proc. European Test Conference, pp.307-16, 1991

[4] S.K.Sunter, N.Nagi, **"A simplified polynomial-fitting algorithm for DAC and ADC BIST"** Proc. IEEE International Test Conference, pp.389-395, 1997.

[5] F.Azais, S.Bernard, Y.Betrand, M.Renovell, "**Towards an ADC BIST scheme using the histogram test technique"** IEEE European Test Workshop, pp:53 – 58, 2000.

[6] F.Azais, S.Bernard, Y.Bertrand, M.Renovell, "**Implementation of a linear histogram BIST for ADCs"** Proc. Conference and Exhibition Design, Automation and Test in Europe, pp:590 – 595, 2001.

[7] K.Arabi, B.Kaminska, J.Rzeszut, **"A New Built-In Self Test Approach For Digital-to-Analog and Analog-to-Digital Converters"**, Proc. IEEE International Conference on Computer-Aided Design, pp: 491-494, 1994.

[8] N.Nagi, A.Chatterjee, J.Abraham **"A Signature Analyzer for Analog and Mixed-Signal Circuits"**, Proc. IEEE International Conference on Computer Design, pp: 284-287, 1994.

[9] M. Mahoney, **"DSP-Based Testing of Analog and Mixed-Signal Circuits"**, IEEE Computer Society Press, ISBN 0-8186-0785-8, 1987.

[10] Ozev, S.; Bayraktaroglu, I.; Orailoglu, A.; **"Seamless test of digital components in mixed-signal paths"** IEEE Design & Test of Computers, Volume 21, Issue 1, pp:44 - 55, 2004

[11] J-M. Janik, **"Estimation of A/D Converter Nonlinearities from complex Spectrum"**, IEEE Proc. International Workshop on ADC Modeling and Testing, pp.8-10. 2003.

[12] V. Kerzérho, P. Cauvet, S. Bernard, F. Azais, M. Comte and M. Renovell "**"Analogue Network of Converters"**: A DFT technique to test a complete set of ADCs and DACs embedded in a complex SiP or SoC" IEEE Proc European Test Symposium, 2006

[13] de Vries, R.; Janssen, A.J.E.M.; **"Decreasing the sensitivity of ADC test parameters by means of wobbling"** IEEE Proc VLSI Test Symposium,. pp:386 – 391, 1998