Minimizing Test Power in SRAM through Pre-charge Activity Reduction

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Abstract

In this paper we analyze the test power of SRAM memories and demonstrate that the full functional pre-charge activity is not necessary during test mode because of the predictable addressing sequence. We exploit this observation in order to minimize power dissipation during test by eliminating the unnecessary power consumption associated with the pre-charge activity. This is achieved through a modified pre-charge control circuitry, exploiting the first degree of freedom of March tests, which allows choosing a specific addressing sequence. The efficiency of the proposed solution is validated through extensive Spice simulations.

1. Introduction

Reducing power dissipation during testing of complex Systems-on-Chip (SoC) has been acknowledged as a major concern. Industrial research has shown that the power dissipation during test mode can be several times larger than in normal functional mode [1, 2]. We have chosen to focus our attention on memories because, as indicated by the ITRS'03 [3], over 90% of SoC area in 2008 will be employed by memories. Minimizing test power in embedded memories is important since they are becoming the main contributor to the overall IC power dissipation.

Whilst numerous papers on constraining power dissipation during test exist [4, 5], there appear to be only few publications that address reducing test power in memories. In [6] and [7], the authors outline techniques that mainly reduce power during functional mode and they indicate how their technique can be employed during test or error correction. In this paper, we propose a new method that minimizes the test power in SRAM memories, by exploiting the predictability of the addressing sequence. It is known that [8, 9] the pre-charge circuits are the principal contributor to power dissipation in SRAM. These circuits have the role of pre-charging and equalizing the long and high capacitive bit lines. This action is essential to ensure correct memory operation. In this work we have developed a technique that reduces the pre-charge activity during test. This technique is based on the fact that in functional mode the cells are selected in random sequence, and therefore all pre-charge circuits need to be always active, while during the test mode the access sequence is known, and consequently, only the columns that are to be selected need to be pre-charged. We implemented this low power test mode by using a modified pre-charge control circuitry.

The rest of the paper is organized as follows. In Section 2, we describe the SRAM pre-charge operation in functional mode. In Section 3, we present the new method that allows reducing the pre-charge activity during test mode, and its implementation in Section 4. Experimental validation of the proposed low power technique for SRAM is presented in Section 5. Conclusions and future work directions are given in Section 6.

2. Background: SRAM functional mode

In random access memories during functional mode, the addressing sequence is unpredictable. Consequently, all bit lines need to be pre-charged (to VDD) in order to have all the array columns ready for a new operation. When a cell is selected for a read/write operation, the corresponding pre-charge circuit is normally turned off during the time required for the operation. For the columns that are not involved in the operation, the pre-charge circuit is commonly left *ON* and the corresponding cells undergo a stress called RES (Read Equivalent Stress), as it has been demonstrated in [10]. For example, in an 8kx32 SRAM, organized as an array of 512 rows x 512 column, when a read/write operation is performed on a cell, the other 511 cells of the same row undergo RESs. This is illustrated in Figure 1. When the cell $C_{i,0}$ is selected for a read/write operation, the word line selection signal

WL_i is activated and all the cells of the i^{th} row are selected, and thus connected with their bit lines.

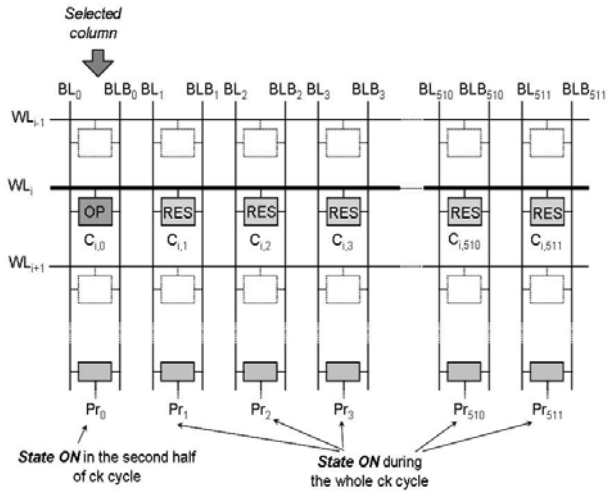

Figure 1 – Functional mode of an SRAM array

The actual operation is performed on cell $C_{i,0}$, while all the other cells in the row undergo RESs. With the pre-charge circuits (Pr_j) active and the word line command being high on the unselected columns, the cells fight against the pre-charge circuits, that pull-up the voltage level at VDD. In Figure 2, we show the operational diagrams of a pre-charge circuit of a selected and an unselected column.

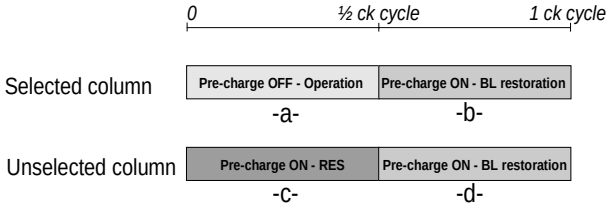

Figure 2 - Pre-charge action for a selected and an unselected column

In the following, we will identify the two main sources of power consumption in the unselected columns related to the pre-charge activity. Firstly, the cells in the unselected columns consume power due to the RES. Secondly, there is power dissipation in the pre-charge circuits of these columns because they are always *ON*. In the normal operation mode of a random access memory, this pre-charge activity is essential and the RES is tolerated, because at the end of each operation all the columns of the array, including the current selected column, need to be ready for the next operation, whose location is unpredictable.

During the memory test mode, however, the addressing order to access the cells (and the columns) is known. Consequently the power dissipation due to pre-charge and RESs could be significantly reduced by pre-charging only the necessary columns as it will be shown in the following section.

3. Reducing power dissipation during test

Memories are mainly tested with fault-oriented algorithms, such as March tests [11]. All March tests are characterized by six Degrees Of Freedom (DOF) and the first one states: any arbitrary address sequence can be defined as an ⇑ sequence, as long as all addresses occur exactly once (⇓ is the reverse of ⇑). The fault detection properties are independent of the utilized address sequence [12, 13]. This means that we can choose the addressing sequence of a March test without changing its capability to cover the target faults, for most March algorithms. We exploit this property of March tests in order to minimize power dissipation during test by eliminating the unnecessary pre-charge activity.

For this purpose, we choose the addressing sequence ‘word line after word line'. For example, consider an SRAM organized as an array of *n* rows x *m* columns. The read and write operations of each March element need be operated first on all the *m* cells of the first word line, then on the *m* cells of the second word line, and so on, as shown in Figure 3.

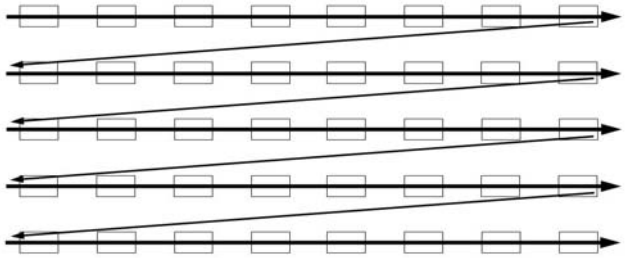

Figure 3 – Access order “word line after word line”

With this particular addressing sequence, when one March element is operated on a certain cell, and thus in a certain column of the array, the following cell to be selected is placed in the column that immediately follows. This means that the pre-charge action is required only in two columns of the entire memory array:

- In the selected column, because the bit line restoration is needed for each following operation of the current March element.
- In the column that immediately follows, because the next cell to be accessed is placed there.

Considering the scenario of a 512x512 SRAM array configuration, we have:

- In the selected column: pre-charge is OFF during the first half of the cycle. Pre-charge is ON during the second half of the clock cycle, see Figure 2a and 2b.
- In next column to be selected, the pre-charge is ON during the entire clock cycle, see Figure 2c and 2d.

– In all the other 510 columns the pre-charge circuit can be turned OFF, because the cells of these columns are not involved in the immediately following operation. This leads to a significant saving in cell array power consumption, as it will be shown in the experimental section.

Figure 4 shows the previously described scenario when in the memory array column ‘0’ is selected.

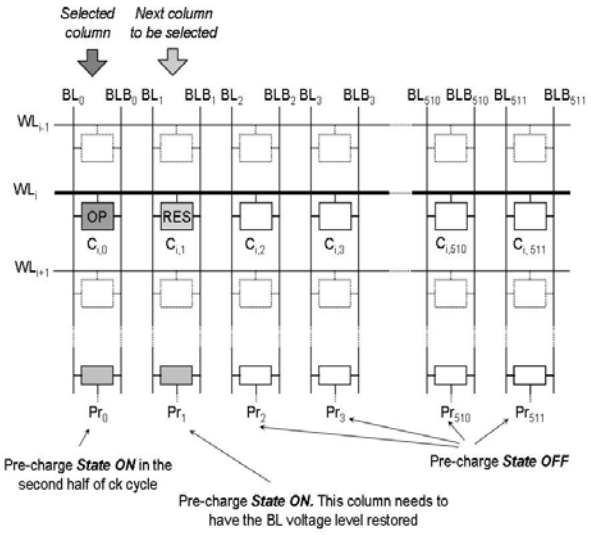

Figure 4: Proposed pre-charge activation

For the 510 columns where the pre-charge circuit is inactive, the cells are still selected by the common word line selection signal. This implies that these cells are still interacting with their corresponding bit lines. These bit lines behave like floating capacitors, which are not driven any longer by the pre-charge circuits, but by the cells. We have studied this interaction with Spice simulations using the following parameters: technology: 0.13µm; clock cycle: 3ns; voltage supply: 1.6 V. The scheme used in the simulation is depicted in Figure 5, while the results are shown in Figure 6.

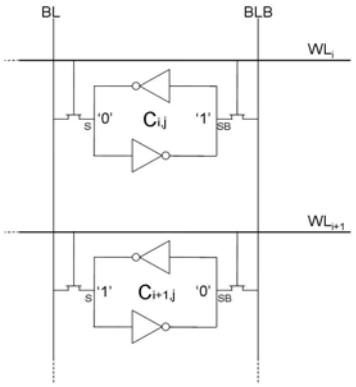

Figure 5 – Scheme of interaction between unselected cells and bit lines

The scheme in Figure 5 shows two cells $C_{i,\,j}$ and $C_{i+1,\,j}$ placed in the same column. Cell $C_{i,\,j}$ stores ‘1’ (node S at ‘0’and node SB at ‘1’) and $C_{i+1,\,j}$ stores the opposite value ‘0’ (node S at ‘1’and node SB at ‘0’). In the first part of simulation, cell $C_{i\,j}$ is selected (WL_i at VDD) and interacts with the bit lines. After a certain delay, cell $C_{i,\,j}$ is deselected (WL_i at ‘0’), and cell $C_{i+1,\,j}$ selected (WL_{i+1} at VDD).

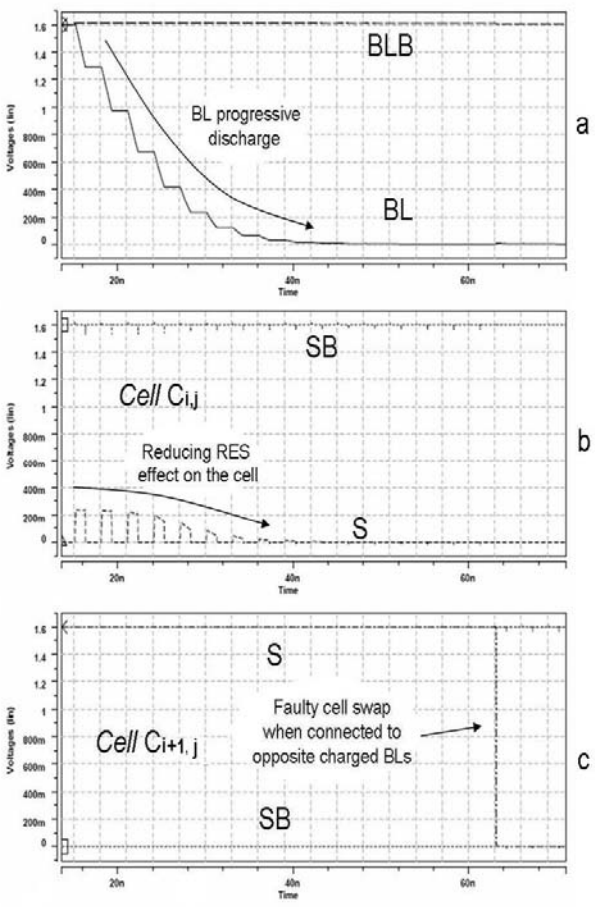

Figure 6 - Spice simulations of the interaction between unselected cells and bit lines

The waveforms in Figure 6a and 6b show that the contact between node SB of cell $C_{i,j}$ and bit line BLB has no effect on the voltage levels of BLB and node SB, because both of them are at VDD. On the other hand, the contact between cell node S active at ‘0’ and bit line BL floating at VDD produces the progressive discharge of BL to 0V (logic value ‘0’) in nearly nine clock cycles. This implies that, after a short time, in all the unselected columns, the cells are not stressed anymore by the bit lines. The consequence is that in the unselected cells there is no more power consumption associated with RES, as shown in Figure 6b.

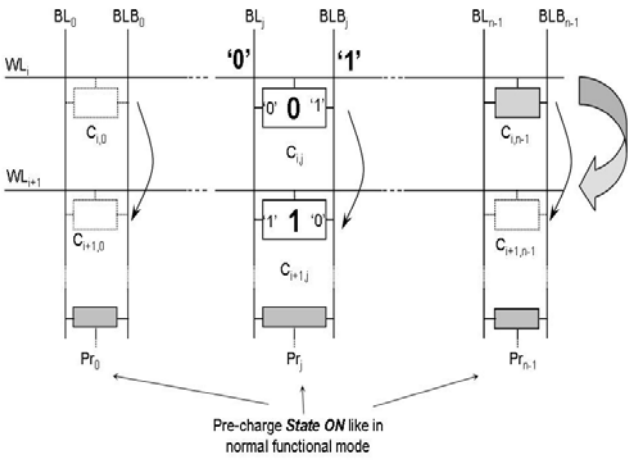

Figure 7 – Preserving faulty cell swap during row transition

The transition from the current array row *i* to *i+1* may lead to a problem as shown in Figure 7. Cell $C_{i,j}$, storing a '0', has driven its bit lines BL and BLB respectively at '0' and '1'. In the transition from the i^{th} row to the $(i+1)^{th}$ row, these same bit lines are connected to cell $C_{i+1,j}$ that stores an opposite value ('1'). This event causes the faulty swap of cell $C_{i+1,j}$. This is because the bit lines drive the value of the cell $C_{i+1,j}$, since their equivalent capacitances are much larger than the cell nodes capacitances. The occurrence of this faulty swap is shown in Figure 6c. The solution that we propose for this problem is: in the last operation on the last cell on the current row, the bit line level of all columns is restored at VDD by activating their pre-charge circuits for only this clock cycle (Figure 7). The advantage of this solution is that it preserves the data background independency, which means that any value can be stored in the cells.

4. Pre-charge control modification

According to the proposed low power test technique the SRAM memory can operate in two different modes: a functional mode in which the memory acts normally and a low power test mode in which the addressing sequence is fixed to 'word line after word line' and the pre-charge activity is restricted to two columns for each clock cycle: the selected column and the following one. During the last operation on the last cell of each row, the memory returns to functional mode for only one clock cycle, in order to restore voltage level of all the bit line at VDD, for the operations in the next row.

We propose a practical implementation of this method consisting in a modification of the pre-charge control circuitry, which allows switching between the functional mode and the low power test mode. In the low power test mode, the pre-charge is active for the selected column *j* and the following one, and for this purpose, we use as pre-charge signal (NPr_j): the column pre-charge signal (Pr_j) when the column *j* is selected; the previous column selection signal ($\overline{CS}_{j-1}$) when the column is not selected; the new pre-charge control logic is depicted in Figure 8.

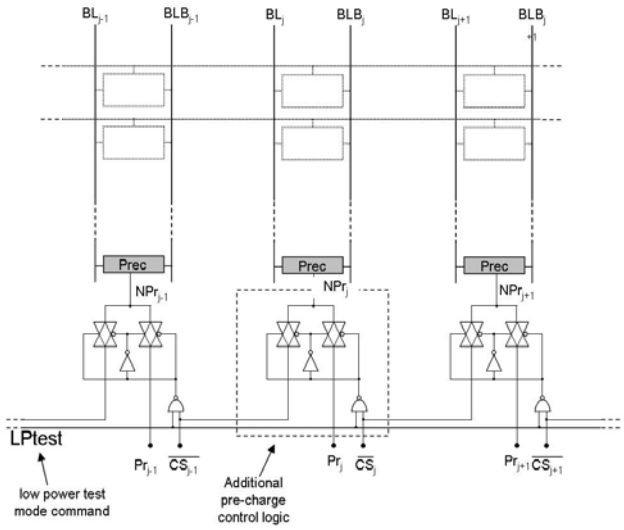

Figure 8 – The modified pre-charge control logic

The modified pre-charge control logic contains an additional element for each column. This element consists of one multiplexer (two transmission gates and one inverter) and one NAND gate. The additional cost of the added logic is ten transistors. The signal LPtest allows the selection between the functional mode and low power test mode. The signal Pr_j is the former pre-charge signal, while $\overline{CS}_j$ is the complementary of column selection signal. The multiplexer acts the mode selection, while the NAND gate forces the functional mode for the column when it is selected for a read/write operation. When LPtest is ON, the signal $\overline{CS}_j$ of a column j drives the pre-charge of the next column j+1. Note that the pre-charge is active with the input signal at '0'. The $\overline{CS}$ signal of the last column is not connected to the first column pre-charge control, because it is not necessary. As stated above, for the transition from a row to the next one, the functional mode is restored for one clock cycle, making the first column ready to be accessed for a read/write operation, and avoiding faulty cell swaps in the other columns.

We have studied the effect of the modified pre-charge logic and we have found that it has negligible impact in terms of performance during normal operation. The switching between the functional mode and the low power test mode is achieved by a multiplexer implemented by two transmission gates (Figure 8). When the functional mode is selected the transmission gate on the right in Figure 8 allows signal Pr_j to drive the pre-charge circuit. We have chosen the transmission gate (two transistors),

instead of a single pass transistor, to ensure the minimum delay in the transitions ($0\rightarrow1$ and $1\rightarrow0$) of the Pr_j signal during the normal functional mode, as well as CS_{j-1} signal during low power test mode.

The proposed method assumes 'word line after word line' addressing sequence. It should be noted that for algorithms that require different addressing sequence or rely on normal operation power consumption [10, 12, 14 and 15], the normal function mode can be selected.

5. Experimental results

In this section, we first analyze the sources of power consumption in the traditional and proposed test scenario. Next, based on this analysis we show how the power dissipation of the two scenarios is computed. Finally, we present and discuss the experimental results. Our analysis shows hat there are five main sources of power dissipation during test:

1. Pre-charge circuits. Apart from the selected column, (n-1) pre-charge circuits are ON in functional mode, while only one pre-charge circuit is ON in low power test mode.

2. Array row transition. The activation of the normal mode, for one clock cycle at the row transition, involves significant power dissipation, due to the restoration at VDD voltage level for about 50% of all the bit lines in the array. This is because half of the bit lines have been driven to '0' by the indirect selected cells, with few of them not completely discharged, as shown in Figure 6a. Note that, even though this event involves significant power dissipation, its impact on the average power per clock cycle is reduced because of its unfrequent occurrence. This line is charged and discharged only once for each row transition, thus its frequency is very low:

F(Row transition) =1/(#March element operations)* *(#memory columns)

Considering a one operation March element and n=512, the signal there is a row transition once for each 512 (=512*1) clock cycles. For a four operations element it happens once every 2048 (=512*4) clock cycles. For its low occurrence the average power increment per clock cycle can be neglected.

3. Driver of signal LPtest. The line that carries this signal has the same equivalent capacitance of a word line, because it has the same length and it drives the same number of MOS transistors. This line is charged and discharged only once for each row transition, thus its frequency is very low (see point 2) and therefore its contribution to the average power per clock cycle that it brings can be neglected.

4. Read Equivalent Stress consumption. The (n-1) cells undergo RESs in functional mode, while, in low power test mode, only one cell undergoes a full RES. This cell is the one placed in the column immediately after the selected one. Moreover, few other cells (<10), undergo a reduced RES, as shown in Figure 6a and 6b. We identify with α ($2<\alpha<10$) the average number of cell that undergo to a RES in low power test mode. We have performed Spice simulations showing that the cell power dissipation during a RES is three orders of magnitude smaller than the pre-charge power dissipation during the RES. Consequently the cell power dissipation can be neglected.

5. Modified pre-charge control logic. The gates that used to realize this logic are designed with minimal dimensions because their output load is very low. The capacities driven by these gates are about three orders of magnitude smaller than a single bit line capacitance. Moreover, there is only one control element switching for each column changing. For these reasons, the contribution of the new control elements to the overall power dissipation can be considered negligible.

Based on the previous analysis, it can be concluded that the power dissipation reduction depends on the memory array organization (#row and #col) and on the March algorithm that is being run (#elements and # operations per element). Also the number of read (#read) and write operations (#write) of the algorithm is important in the computing, because the power dissipation of a read action is lower than that of a write action. On the other hand, the power reduction per operation offered by the method is independent on the type of performed operation.

The average power dissipations per clock cycle during functional mode and low power test mode (respectively P_F and P_{LPT}) are given by:

$$P_F = \frac{\#\,\text{read} \cdot P_r + \#\,\text{write} \cdot P_w}{\#\,\text{operations}}$$

and

$$P_{LPT} = P_F - \left((\#\,\text{col} - 2) \cdot P_A - \frac{\#\,\text{elements}}{\#\,\text{operations}} \cdot P_B \right)$$

where:

P_A: Power consumption of one pre-charge circuit during a RES;

P_B: Power consumption of a column restoration during the row transition;

P_r: Memory power consumption during a read operation;

P_w: Memory power consumption during a write operation.

We define the Power Reduction Ratio (PRR) as

$$PRR = 1 - \frac{P_{LPT}}{P_F}$$

To give insight into the test power reduction, we have run a set of well-known March tests in the functional and low power test modes, on a 512x512 0.13µm SRAM. We have chosen these algorithms, because they consist of

different number of elements and operations. The Spice simulation results, with the following operational parameters (3ns clock cycle and 1.6V voltage supply), are shown in Table 1.

Algorithm	# elm	# oper	# read	# write	PRR
March C-	6	10	5	5	47.3 %
March SS	6	22	13	9	50.0 %
Mats+	3	5	2	3	48.1 %
March SR	6	14	8	6	49.5 %
March G	7	23	10	13	50.5 %

Table 1 – PRR for different March algorithms

The experimental results show that this method leads to a significant reduction in terms of overall power consumption (~50%) for the considered SRAM memory. This result can be extended to all SRAM memories because it reduces the pre-charge circuitry activity, which represents up to 70%-80% of the overall power dissipation of SRAM memories, as demonstrated in [8].

6. Conclusions

In this work we have presented a method that minimizes the test power in SRAM memories by reducing the pre-charge activity. This was achieved by exploiting the fact that the addressing sequence during test is predictable, and hence only two columns need to be pre-charged in each clock cycle. We have implemented this low power test mode by using a modified pre-charge control logic. Spice simulations used to validate the proposed method show significant power reduction in the cell array (~50%). It has been shown that the effect of the modified pre-charge logic on the normal functional mode is negligible.

In this study we have considered only bit-oriented memories. We are currently extending the method to word-oriented memories. Also, we will consider the capability of the proposed method to reduce power consumption during test when applied to other types of memories.

Acknowledgements

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References

[1] C. Shi and R. Kapur, “How power aware test improves reliability and yield”. In *EDDesign*.com, 2004

[2] P. Girard “Survey of Low-Power Testing of VLSI Circuits”, IEEE Design & Test of Computers, 19(3), 2002, pp. 82-92

[3] Semiconductor Industry Association (SIA), "International Technology Roadmap for Semiconductors (ITRS)", 2003

[4]P. Rosinger, B. Al-Hashimi, and N. Nicolici, “Scan architecture with mutually exclusive scan segment activation for shift and capture power reduction”. IEEE Transactions on Computer Aided Design of Integrated Circuits, 23(7), 2004, pp 1142–1154

[5]E. Larsson, K. Arvidsson, H. Fujiwara, and Z. Peng, “Efficient test solutions for core-based designs” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 23(5), 2004, pp. 758–775

[6] S. Bhattacharjee, D.K. Pradhan, “LPRAM: A Novel Low-Power RAM Design with Testability”, IEEE Transactions on CAD, 23, 2004, pp. 637-651

[7] P. Ohler, S. Hellebrand, “Low power embedded DRAMs with high quality error correcting capabilities”, Proc. European Test Symposium, 2005, pp.148 - 153

[8] D. Liu and C. Svensson, “Power Consumption Estimation in CMOS VLSI Chips”, IEEE Journal of Solid State Circuits, 28 (6), 1994

[9] T. Nirshl, B. Wicht, D. S. Landsiedel, “High Speed, Low Power Design Rules for SRAM Pre-charge and Self-Tming under Technology Variation”, Proc. Intern. Workshop of Power and Time Modeling Optimization and Simulation, 2001, Suisse

[10] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan “Efficient March Test Procedure for Dynamic Read Destructive Faults detection in SRAM Memories” JETTA: Journal of Electronic Testing: Theory and Application, 21 (21), 2005, pp 551-561

[11] A.J. van de Goor, “Testing Semiconductor Memories: Theory and Practice”, COMTEX Publishing, Gouda, The Netherlands,1998.

[12] D. Niggemeyer, M. Redeker and J. Otterstedt, “Integration of Non-classical Faults in Standard March Tests”, Records of the Int. Workshop on Memory Technology, Design and Testing, 1998

[13] M. Nicolaidis, “An Efficient Built-In Self-Test Scheme for Functional Test of Embedded Memories”, Proc. Int. Symposium Fault Tolerant Computing, 1985.

[14] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel and S. Borri, "March iC-: An Improved Version of March C- for ADOFs Detection", Proc. IEEE VLSI Test Symposium, 2004, pp. 129-134.

[15] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, M. Hage-Hassan “Data Retention Fault in SRAM Memories: Analysis and Detection Procedures” Proc. IEEE VLSI Test Symposium, 2005