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Temperature and Voltage Aware Timing Analysis: Application to Voltage Drops

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Abstract

In the nanometer era, the physical verification of CMOS digital circuit becomes a complex task. Designers must account of new factors that impose a significant change in validation methods. One of these major changes in timing verification to handle process variation lies in the progressive development of statistical static timing engines. However the statistical approach cannot capture accurately the deterministic variations of both the voltage and temperature variations. Therefore, we define a novel method, based on non-linear derating coefficients, to account of these environmental variations. Based on temperature and voltage drop CAD tool reports, this method allows computing the delay of logical paths considering more realistic operating conditions for each cell. Application is given to the analysis of voltage drop effects on timings.

I-Introduction

The common way to validate a circuit is to use the known based approach during the static timing analysis (STA). The main drawback of such analysis lies in its conservatism [1]. If the resulting design margins guarantee obtaining high yield values, they may induce some convergence problem during the timing optimization step. The Statistical Static Timing Analysis [1-4] appears as a powerful alternative to reduce these design margins and also to take inter and intra-die process dispersions into account. However statistical methods can be applied while dealing with random variables, and thus cannot handle the deterministic variations of the temperature (T) and the supply voltage (V).

This paper tackles only the problem of V, T variations, and more precisely their effects on timings. As aforementioned, the effects of V, T variations on timings are actually taken into account considering the worst case operating condition. As for process variations, this can be pessimistic. Indeed, due the complexity of circuits, temperature and voltage gradients may be as large as 50°C and 200mV. In order to reduce this pessimism, methods must be defined to manage, during the STA, various operating conditions.

Despite the reduction of design margins, the definition of such methods could be of great help within the context of low power applications. Indeed, among all the low power design techniques formerly proposed, the use of a reduced V_{DD} values [5-6] or the use of different supply domains [7-8] are popular solutions. However these solutions require intensive timing analysis to validate a design, i.e. to capture the true timing worst case. Considering for example the validation step, this requires characterizing separately each voltage island with its specific corners. This quickly leads to consider more than four corners for the validation of dual supply voltage chips.

This doubling (at least) of the number of corners is moreover amplified by the apparition of the reversal of temperature sensitivity [9-11] while working with reduced V_{DD} values. Indeed, due to the combined use of high V_T devices and reduced supply voltage values, the worst case timing conditions becomes less predictable and may occur at any temperature. In most of cases, this temperature effect is taken into account through design margins. However for high performance designs it may be necessary to perform validations in more than 2 PVT conditions (up to 8 for dual V_{DD} chips) in order to guarantee the correct behavior of a design.

Within this context, timing analysis techniques able to handle different temperature and voltage conditions are required to speed up the validation process of complex designs. The definition of such techniques is all the more important as they may help designers to reduce the important design margins by considering different temperature and voltage islands during the validation rather than global and pessimistic values.

This paper aims at introducing a non linear derating based timing analysis technique. The main advantage of the proposed technique lies in its ability to handle, at cell level, different temperature and supply voltage conditions. Besides this significant advantage, the proposed technique does not require any additional characterization step nor as any drastic change in the way to characterize standard cell libraries. The remainder of the paper is organized as follows. In section II, we introduce the analytical timing model from which the non linear coefficients have been deduced. This model is then used in conjunction with electrical

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simulations to analyze in section III the non linear effects of temperature and voltage changes on timings. In Section IV, we introduce more formally the proposed timing analysis technique and also derive from the analytical model the associated non linear derating factors. In section V, the proposed timing analysis technique is validated at cell and path levels. Finally a conclusion is drawn in section VI.

II-Analytical Timing Model

It has been shown in [12-14] that the propagation delay of CMOS structures can be evaluated using an analytical representation of the cell output transition time with an explicit identification of the design and process parameters. Since the model proposed in [12-14] is intensively used all along this paper, we sum-up below its main characteristics considering for simplicity only the case of falling output edges.

A. Transition time modeling

Modelling the transistor as a current generator [13], the output transition time of CMOS primitives can be obtained from the modelling of the discharging current that flows during the switching process and from the amount of charge ($C_L \cdot V_{DD}$) to be removed from the output pin:

$$\tau_{outHL} = C_L \cdot V_{DD} / I_{MAX} \qquad (1)$$

where C_L represents the total output load, I_{MAX} is the maximum current available in the structure. The key point here is to evaluate I_{MAX} value which depends on the input and output controlling conditions. For that, two domains have to be considered: the Fast input and the Slow input ramp ranges.

In Fast input ramp domain, the high slew rate of the incoming signal forces the structure to provide all the current it can deliver [12]. As a result, the switching current has a maximum and constant value which can easily be obtained from the alpha power law model [15]:

$$I_{MAX}^{Fast} = K_N \cdot W_N \cdot (V_{DD} - V_{TN})^{\alpha_N} \qquad (2)$$

Combining then (1) and (2) finally leads to the output transition time expression associated to the Fast input ramp range

$$\tau_{outHL}^{Fast} = \frac{DW_{HL} \cdot C_L \cdot V_{DD}}{K_N \cdot W_N \cdot (V_{DD} - V_{TN})^{\alpha_N}} \qquad (3)$$

where DW_{HL} coefficients is the logical weight or the logical effort of the considered CMOS structure (DW_{HL}=1 for inverters), $C_{N/P}$ are N/P gate capacitance of N/P transistors respectively.

In the Slow input ramp domain, the maximum switching current decreases with the input ramp duration. Extending the results of [5] to general value of the velocity saturation index, we did obtain a manageable transition time expression in the Slow input ramp domain:

$$\tau_{outHL}^{Slow} = \left(\frac{DW_{HL} \cdot Cl \cdot \tau_{IN}^{\alpha_N} \cdot V_{DD}^{1-\alpha_N}}{\alpha_N \cdot K_N \cdot W_N} \right)^{\frac{1}{1+\alpha_N}} \qquad (4)$$

To conclude with the modeling of the output transition time, one can observe that in the Fast input range the transition time only depends on the output load while in the slow input range, it also depends on the input transition time duration, and is threshold voltage independent.

B. Propagation delay modeling

The delay of a CMOS gate is load, gate size and input slew dependent. Following [16-18], the input slope and the I/O coupling capacitance can be introduced in the propagation delay as

$$t_{HL} = \frac{\tau_{in}}{\alpha_N + 1} \left(\frac{\alpha_N - 1}{2} + \frac{V_{TN/P}}{V_{DD}} \right) + \left(1 + \frac{2C_M}{C_M + C_L} \right) \frac{\tau_{outHL}}{2} \qquad (5)$$

The latter expression captures all the delay sensitivity of basic CMOS gates to its environment (τ_{IN}, τ_{out}).

C. Timing model for thermal analysis

In the preceding paragraphs, we have introduced a design oriented model of the two main timing metrics that exhibits all the useful design parameters such as the gate capacitance, the load and the input slew. If V_{DD} appears explicitly in this timing representation, the temperature does not. Therefore the model should be improved to capture the effects of the temperature. This can be easily done. Indeed, to characterize a process with respect to the temperature (θ), only two coefficients have to be considered (δ and X_k) [18, 19] that give respectively the temperature dependency of V_T and K:

$$V_T = V_{Tnom} - \delta \cdot (\theta - \theta_{nom}) \quad K = K_{nom} \cdot \left(\frac{\theta_{nom}}{\theta} \right)^{X_K} \qquad (6)$$

Including (6) in eq. (3, 4, and 5) leads to temperature explicit model. The resulting expressions (9, 10, and 11) can be used for thermal analysis.

$$\tau_{outHL}^{Fast} = \frac{DW_{HL} \cdot Cl}{K_N \cdot \left(\frac{\theta_{nom}}{\theta} \right)^{X_K} \cdot W_N \cdot (V_{DD} - V_{TN} + \delta \cdot (\theta - \theta_{nom}))^{\alpha_{N/P}}} \qquad (7)$$

$$\tau_{outHL}^{Slow} = \left(\frac{DW_{HL} \cdot Cl \cdot \tau_{IN}^{\alpha_N} \cdot V_{DD}^{1-\alpha_N}}{\alpha \cdot K_N \cdot W_N} \cdot \frac{\theta^{X_K}}{\theta_{nom}^{X_K}} \right)^{\frac{1}{1+\alpha_N}} \qquad (8)$$

$$t_{HL} = \frac{\tau_{in}}{\alpha_N + 1} \left(\frac{\alpha_N - 1}{2} + \frac{V_{TN} - \delta \cdot (\theta - \theta_{nom})}{V_{DD}} \right) + \left(1 + \frac{2C_M}{C_M + C_L} \right) \frac{\tau_{outHL}}{2} \qquad (9)$$

Expressions (7-9) reveal an interesting point. The comparison of the output transition expression (8-9) shows that the temperature has a different influence on the output slope in the Fast and Slow input ramp domain. This is mainly due to the fact that the transition time is threshold voltage independent in the slow input ramp domain. This justifies why in the following paragraphs the T and V_{DD} induced effects on performances are studied considering several input ramp durations.

III-Non-linear effects of T and V_{DD} variations

In order to analyze these effects, we simulated the sensitivity of the timings to V_{DD} and T for a Fast (1ps) and a slow input ramp (300ps). The results we obtained are reported on Fig.1 and 2.

As expected from the timing model, for a given V_{DD} value, the sensitivity of the output transition time for Fast input ramps is quite limited compared to that simulated for the Slow input ramp domain. This is mainly explained by the opposite influence of the temperature induced variations of K and V_T in the Fast input range (9). The temperature induced effect on the output transition time in the Slow input range is more complex. To get insight, let us consider the derivative with respect to the temperature of eq. (10).

$$(\tau_{IN})^{\frac{\alpha}{1+\alpha}} \cdot (V_{DD})^{\frac{1-\alpha}{1+\alpha}} \cdot \theta^{\frac{X_k}{1+\alpha} - 1} \qquad (10)$$

This expression indicates that for a given V_{DD} value, the sensitivity is a decreasing function of the temperature (X_k<1). Moreover (10) predicts that the rate of decrease is all the more important as the V_{DD} is small. This prediction can be verified on Fig.1 except for high V_{DD} values. For such V_{DD} values the short

circuit current, which is not taken into account by the model, has a significant impact on the temperature dependency. This lack will be considered later in the paper.

Fig.2 gives the derivative of the propagation delay wrt the temperature for supply voltage values varying from 0.9V to 1.45V. As shown, two behaviors associated respectively with the fast and slow input ramp domains clearly appear. As expected from the preceding discussion, the sensitivity in the Fast input range is quite constant. For the Slow input ramp, the first term of (9) which is proportional to V_T (11) and to the input ramp duration imposes the waveform of the associated surface.

$$\frac{\partial t_{HL}^{Slow}}{\partial \theta} = \frac{-\delta \cdot \tau_{IN} \cdot \theta}{(1+\alpha) \cdot V_{DD}} + \frac{\partial \tau_{outHL}^{Slow}}{\partial \theta} \qquad (11)$$

The propagation delay sensitivity to θ in the slow input ramp domain (Fig.2) gives is a direct illustration of the reversal of temperature dependency. Indeed, despite the respective trends with V_{DD} and T, in the slow input domain the sensitivity starts from a positive value for high V_{DD} and quickly becomes negative for lower V_{DD} values.

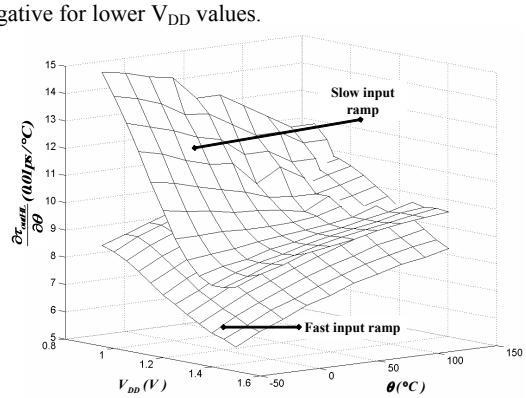

Figure 1. Sensitivity of the τ_{OUT} to T (°C) wrt V_{DD}

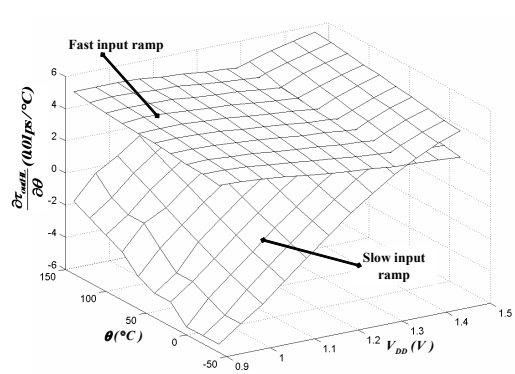

Figure 2. Sensitivity of the t_{HL} to the T (°C) wrt V_{DD}

If for the process under consideration, this appears in the Slow input ramp domain, this reversal of the temperature dependency could also appear in the Fast input domain. In Fact as demonstrated in [11], there is always an input ramp value for after which the propagation delay sensitivity to the temperature becomes negative. This input ramp value could either be a Fast or Slow input ramp depending on the V_T/V_{DD} ratio that fixed the relative importance of the first term of (11) with respect to the second one.

Fig.2 also shows that the point at which the sensitivity is zero depends on both the temperature and supply voltage values. Thus, at cell level, the reversal of temperature dependency could or could not appear depending on the (V_{DD}, T, τ_{IN}, C_L) quadruplet.

IV-Derating Factors

To validate a circuit designed with a process subjected to the reversal of temperature dependency, timing analysis must be performed considering at least four different PVT corners: 2 to guarantee that there are no hold time violations and 2 others to guarantee that there are no setup time violations. As a result standard cell libraries must be at least characterized for these four different corners. If the corner based approach is extremely robust, it does not allow designers to deal with different supply voltage and temperature domains.

In this paragraph we introduce a method to handle T and V_{DD} variations during the timing analysis while keeping the fundamental advantages of the corner based approach i.e. its simplicity and its robustness. The basic goal of the proposed timing analysis technique is to allow designers to predict, starting from a worst case analysis, more realistic performances for all the cells of a design considering more realistic T and V_{DD} values. This is achieved using a simple derating method:

$$(t,\tau)_{P_{corner},V_{corner},T_{corner}} = (t,\tau)_{P_{corner},V,T} + \left(\frac{\delta t,\tau}{\delta V_{DD}}\right)\Delta V_{DD} + \left(\frac{\delta t,\tau}{\delta \theta}\right)\Delta\theta \quad (12)$$

The key point is to develop accurate derating factors. The sensitivity analysis performed above has demonstrated that the derating factors are non linear, design dependent (through C_L and τ_{IN}) and may have different forms depending on the considered input ramp domain. Let us derive from the analytical model the expressions of these factors and more precisely their general mathematical forms.

A. Supply voltage Sensitivity template

Let us first derive from expressions (3), (4), and (6) the mathematical forms of V_{DD} dependency of the both the propagation delay and the output slope. Differentiating the expressions (3) and (6) wrt V_{DD}, we obtained the partial derivatives of the output transition time:

$$\frac{\delta \tau_{outHL}^{Fast}}{\delta V_{DD}} = \frac{DW \cdot C_L}{K_N \cdot W_N} \cdot \frac{(1-\alpha) \cdot V_{DD} - V_T}{(V_{DD} - V_T)^{1+\alpha}} \qquad (13)$$

$$\frac{\delta \tau_{outHL}^{Slow}}{\delta V_{DD}} = \frac{1-\alpha}{(1+\alpha) \cdot \alpha \cdot K_N \cdot W_N} \cdot \left(DW \cdot C_L \cdot \tau_{IN}^{\alpha}\right)^{\frac{1}{1+\alpha}} \cdot \left(V_{DD}\right)^{\frac{-2\cdot\alpha}{1+\alpha}} \qquad (14)$$

These expressions are too complex to be easily calibrated, we thus adopted the simplified expressions, considering that the velocity saturation index value is close to 1:

$$\frac{\partial \tau_{OUT}^{Fast}}{\partial V_{DD}} = \frac{a_{Slope}^{Fast}}{V_{DD}^{2}} + \frac{b_{Slope}^{Fast}}{V_{DD}^{2}} C_L \qquad (15)$$

$$\frac{\partial \tau_{OUT}^{Slow}}{\partial V_{DD}} = a_{Slope}^{Slow} \cdot V_{DD} \cdot (\tau_{IN} \cdot C_L)^{1/2} + b_{Slope}^{Slow} \cdot \frac{\tau_{IN}}{C_L} \qquad (16)$$

where a_{Fast}, b_{Fast} and a_{Slow} are supply voltage independent parameters to be calibrated. They depend on the process and the topology of the cell. Note that the last terms of (16) is a pseudo-empirical term introduced to take into account the effect of the short circuit current effect. For typical design conditions this term is negligible, however for extremely large input ramp values and small load values it becomes significant wrt the two first terms [14]. However this does not correspond to practical design conditions.

Considering that the propagation delay is the sum of two terms, one directly related to the output transition time, the derivation of the derating factor for the propagation delay in the Fast and Slow

input ramp domain is straight forward. As for the output transition time, the obtained expressions have been simplified to obtain the following V_{DD} sensitivity templates of the delay:

$$\frac{\partial t_{HL}^{Fast}}{\partial V_{DD}} = \frac{a_{Delay}^{Fast}}{V_{DD}^{2}} + \frac{b_{Delay}^{Fast}}{V_{DD}^{2}} \cdot \tau_{IN} + \frac{c_{Delay}^{Fast}}{V_{DD}^{2}} C_L \quad (17)$$

$$\frac{\partial t_{HL}^{Slow}}{\partial V_{DD}} = \frac{a_{Delay}^{Slow}}{V_{DD}^{2}} \cdot \tau_{IN} + b_{Delay}^{Slow} \cdot (\tau_{IN} \cdot C_L)^{1/2} + c_{Delay}^{Slow} \cdot \frac{\tau_{IN}}{C_L} \quad (18)$$

All the coefficients a_{Delay} to c_{Delay} have to be calibrated for each cell and for each input pin of a cell.

B. Temperature Sensitivity template

At the end of section II, we have transformed the design oriented model into a thermal analysis oriented one. This transformation has led to expressions (9) to (11). Processing as for the V_{DD} sensitivity, we obtained the mathematical templates of the temperature dependency of the output transition time

$$\frac{\partial \tau_{OUT}^{Fast}}{\partial \theta} = a_{Slope}^{Fast} + b_{Slope}^{Fast} \cdot C_L \quad (19)$$

$$\frac{\partial \tau_{OUT}^{Slow}}{\partial \theta} = a_{Slope}^{Slow} \cdot (\tau_{IN} \cdot C_L)^{1/2} + b_{Slope}^{Slow} \cdot \frac{\tau_{IN}}{C_L} \quad (20)$$

and of the propagation delay for falling output edges:

$$\frac{\partial t_{HL}^{Fast}}{\partial \theta} = a_{Delay}^{Fast} + b_{Delay}^{Fast} \cdot \tau_{IN} + c_{Delay}^{Fast} \cdot C_L \quad (21)$$

$$\frac{\partial t_{HL}^{Slow}}{\partial \theta} = a_{Delay}^{Slow} \cdot \tau_{IN} + b_{Delay}^{Slow} \cdot (\tau_{IN} \cdot C_L)^{1/2} + c_{Delay}^{Slow} \cdot \frac{\tau_{IN}}{C_L} \quad (22)$$

These expressions and those related to the supply voltage values constitute generic expressions of the temperature dependency of basic CMOS cells such as nand, nor, inv. However most of actual libraries include complex cells.

C. Complex gates

Complex gates can be viewed as the aggregation of several basic gates. For example an And2 can be viewed as the cascade of a nand gate (First stage) and an inverter (Second stage). For such structures, the templates defined in the two preceding sections are not sufficient. However, they can be combined to capture accurately the V_{DD} and T dependencies of timing performances.

Let us consider again an And2 gate. In case of a falling output edge, its propagation delay is the sum of the delay of the First and Second stages. Its temperature dependency is therefore the sum of two the four templates defined in the preceding paragraph. There are hence four different configurations depending on the controlling and loading conditions. However complex gates are usually designed such as the first stage provides a fast input ramp to the last stage to achieve high performances. This is typically achieved by designing the first stage such that the intermediate load remains small, and therefore such that its propagation delay remains small compared to that of the second stage. Consequently the temperature dependency of the last stage is given by the (21) while the sensitivity to the first stage is given by either (21) or (22) depending on the input ramp applied on the input. This leads, for the considered And2, to the two expressions of the temperature dependency:

$$\frac{\partial t_{HL}^{Fast}}{\partial \theta} = a_{Delay}^{Fast\ (1)} + b_{Delay}^{Fast\ (1)} \cdot \tau_{IN} + c_{Delay}^{Fast\ (1)} \cdot C_2 + a_{Delay}^{Fast\ (2)} + b_{Delay}^{Fast\ (2)} \cdot \tau_1 + c_{Delay}^{Fast\ (2)} \cdot C_L = A_{Delay}^{Fast} + B_{Delay}^{Fast} \cdot \tau_{IN} + C_{Delay}^{Fast} \cdot C_L \quad (23)$$

$$\frac{\partial t_{HL}^{Slow}}{\partial \theta} = a_{Delay}^{Slow\ (1)} \cdot \tau_{IN} + b_{Delay}^{Slow\ (1)} \cdot (\tau_{IN} \cdot C_2)^{1/2} + c_{Delay}^{Slow\ (1)} \cdot \frac{\tau_{IN}}{C_2} + a_{Delay}^{Fast\ (2)} + b_{Delay}^{Fast\ (2)} \cdot \tau_1 + c_{Delay}^{Fast\ (2)} \cdot C_L = A_{Delay}^{Slow} + B_{Delay}^{Slow} \cdot \tau_{IN} + C_{Delay}^{Slow} \cdot (\tau_{IN})^{1/2} + C_{Delay}^{Slow} \cdot C_L \quad (24)$$

where C_2 is the input capacitance of the second stage and τ_1 is the output transition time of the first stage which is assumed to be a constant. More precisely, the temperature induced variation of τ_1 is assumed to be small enough to be neglected.

Even if expressions (23) and (24) have been developed considering an And2 gate, they do constitute mathematical templates of the T dependency of two stage complex gates. The propagation delay sensitivity to either the supply voltage or the temperature may also be developed for more complex gate following the same reasoning.

Table I: Different process options

V_T \ Tox	Standard	High
Standard	P1_SVT	P1_HVT
High	P2_SVT	P2_HVT

V. Validation

In order to validate the proposed V_{DD} and T aware timing analysis technique, we did several validations at both cell and path levels. All the validations were performed on a 90nm process. Several process options were available for specific design purposes such low power design, high speed design, low leakage design. Table I gives the names of the different process options we considered during the validation.

A-Cell (Library) level validation

To validate the proposed approach we calibrated the mathematical templates of T and V_{DD} dependencies for all the combinatorial cells of the four different libraries. These calibrations were performed considering the usual worst case corner for timings (T=125°C, V_{DD}=0.9V) as the reference point. We then computed the performances of all the combinational cells at different temperature and supply voltage values for different controlling (τ_{IN}) and loading conditions (C_L). We finally compared the extrapolated values to the simulated values. The considered libraries containing around 600 different cells, we therefore investigated an enough important population of comparison points (up to 90K points) to plot distributions.

In a first validation step, we applied our approach to evaluate the cell performances working under temperature of -40°C; the supply voltage being kept constant (0.9V). We then compared the results obtained to that reported in the corresponding timing library file. The accuracy obtained was satisfactory since more than 90% of the errors were contained between the -5% to 5% range.

In a second validation step, we applied our approach to evaluate the performances of our standard cells supplied by 1.1V rather than 0.9V; the temperature being kept constant and equal to 125°C. As for temperature the population distribution obtained for the P1_SVT and P2_HVT have demonstrated the accuracy of the approach. Indeed, 90% of the comparisons points were contained in the -5% to 5% range.

B-Path level validation

The mathematical templates being validated at cell level, we applied them on several critical paths extracted from real designs. More precisely scripts have been developed to interface primetime resulting in the timing analysis flow represented on fig.4.

In a first step a basic timing analysis is performed using PrimeTime for the corner chosen as the reference during the calibration of the derating templates. A timing report is then generated by the tool for the considered paths.

In a second step, all the timings are re-computed for the T and V_{DD} values considered. This timing update cannot be done directly and care must be taken to account of the input ramp effect. We thus first update all the output transition time processing from the first gate to the last gate.

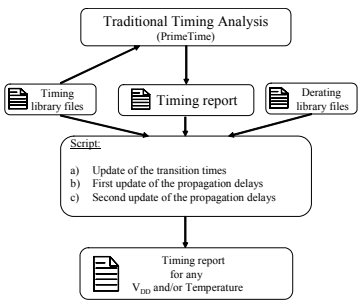

Figure 4. Alternative timing analysis flow

In a third step, all the propagation delay values are recomputed considering the new input ramp values but without applying any derating factors related to the T or V_{DD} changes. In other words, only the effects of the input ramp variations induced by the temperature and biasing changes are considered. The new delay values are computed using the traditional timing library files. This step corresponds in fig.4 to the first update of the propagation delay values.

The final propagation delay values are finally obtained during *the fourth step*. The latter consists in derating the propagation delay values obtained in the third step to take into account the sensitivities of the propagation delay to the temperature and supply voltage. This step corresponds to the second update of the propagation delay values.

We put this alternative timing analysis flow into practice on several combinational paths extracted from real circuits designed with different process options (Table I). In order to validate the proposed method we compared the timings computed with our timing engine to that obtained with Eldo.

We report below some comparison results obtained for ten different paths extracted from a circuit designed in both P1 and P2 (The worst case processes were used). We successively simulated the propagation delays of the ten paths for the following operating conditions: (V_{DD}=0.9V T=125°C), the reference, (V_{DD}=0.9V and T=-40°C) and finally (V_{DD}=1V, T=125°C).

Table II sums up the results obtained for the ten paths supplied by 0.9V and submitted successively to temperature equal to 125°C and -40°C. The accuracy of the calculated propagation delay values is satisfactory.

It appears clearly that the temperature dependency of the paths designed in P1 is limited compared to that of those designed in P2. This can easily be understood considering the number of cells which exhibit a negative temperature coefficient. For the paths designed with the P1 process, it appears that some cells have a negative temperature coefficient while others have a positive coefficient. Therefore a temperature increase implies an increase of the propagation delay of some cells and decrease for others cells leading to a weak path temperature sensitivity value (0.7ps/°C to 1ps/°C). For the P2 process, the statement is completely different since most of the gates have a negative temperature dependency: the temperature sensitivity is greater (-2ps/°C to -4ps/°C) and the worst case corner is therefore observed at T=-40°C.

Table III sums up the results obtained for the ten paths designed in P2 submitted to a temperature equal to 125°C and successively supplied with 0.9V, 1V and 1.1V. The accuracy of the calculated propagation delay values is satisfactory validating the proposed temperature and supply voltage TA technique. As expected the supply voltage dependency of timing performance is more important than the temperature one. Indeed it ranges for the P2 process between -9ps/10mV and -15ps/10mV for the paths under consideration. At cell level we did observe supply voltage coefficient values ranging between -0.3ps/10mV to 2ps/10mV depending on the design conditions. Note that the supply voltage range [0.9V-1.3V] investigated during this validation step include low voltage values below the normal operation condition of process P2. Note that in the normal operation conditions [1.1V-1.3V] the temperature inversion does not occur, even while using the P2 process.

VI. Application to Voltage drops

As discussed earlier our alternative timing analysis technique can be applied in many situations involving special temperature and voltage conditions. In this section, we investigated the impact of voltage drops on timings. More precisely we ran our engine and Eldo tool to compute the timings of several critical paths extracted from a real design. This has been done considering supply voltage values reported by VoltageStorm tool. Fig.5 gives the results obtained, with our engine, with PrimeTime and Eldo, for nine critical paths. As shown, the accuracy between our timing engine and Eldo is satisfactory (errors <2%) but this does not constitute the more interesting result. Note that the paths considered during this analysis were impacted by Voltage drops of typical amplitudes ranging between 2% to 5% of the nominal supply voltage value.

For such paths, a timing margin ranging between 9% and 12% of real path delays can be saved using more realistic V_{DD} values wrt to a worst case analysis. This corresponds to a timing margin reduction of about 90%. These results demonstrate that considering the supply voltage as a global environmental variable during the timing analysis constitutes an important source of pessimism.

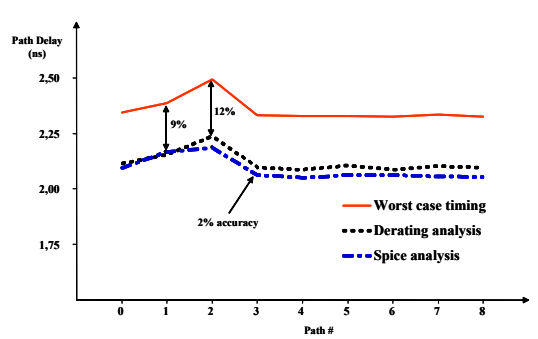

Figure 5. Timing margin reduction obtained considering more realistic V_{DD} values

VII. Conclusion

In the nanometer era the performances are strongly temperature and supply voltage dependent. Consequently, the timing verification step has become extremely complex. To facilitate this

step, we have introduced an alternative timing analysis technique to allow designer to juggle with several temperature and supply voltage values. The proposed technique is non-linear k-factor method. We have applied our alternative timing analysis technique to several data paths extracted from real designs in order to validate it. The obtained results have demonstrated the accuracy of the proposed method and its ability for capturing the reversal of temperature dependency phenomenon. Application of this technique has demonstrated that timing margins as large as 12% of the 'real' path propagation delays can be saved considering more realistic supply voltage values.

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Table II: Simulated and calculated path delay values

	P1				P2			
	Delay Eldo (ns)		Delay Cal. (ns)		Delay Eldo (ns)		Delay Cal. (ns)	
	125°C/0,9V	-40°C/ 0,9V	-40°C/ 0,9V	Error	125°C/ 0,9V	-40°C / 0,9V	-40°C / 0,9V	Error
P0	2,598	2,479	2,464	-1%	5,661	6,164	6,091	-1%
P1	2,546	2,427	2,435	0%	5,471	5,954	5,889	-1%
P2	2,524	2,432	2,443	0%	5,495	6,177	6,060	-2%
P3	2,712	2,507	2,589	3%	5,809	6,278	6,286	0%
P4	2,379	2,204	2,262	3%	4,522	4,86	4,865	0%
P5	2,370	2,199	2,252	2%	4,567	4,943	4,935	0%
P6	2,403	2,229	2,299	3%	4,689	5,049	5,056	0%
P7	2,384	2,215	2,279	3%	4,542	4,887	4,886	0%
P8	2,385	2,206	2,263	3%	4,532	4,864	4,878	0%
P9	2,394	2,224	2,288	3%	4,739	5,133	5,131	0%

Table III: Simulated and calculated path delay values (P2_SVT)

Paths	**Delay Eldo (ns)**			**Delay Calc. (ns)**		**Error (%)**	
	125°C/ 0.9V	**125°C/1V**	**125°C/1.1V**	**125°C/1V**	**125°C/1.1V**		
P0	5,660	4.321	3,499	4.442	3,702	3%	6%
P1	5,471	4.193	3,406	4.300	3,562	3%	5%
P2	5,495	4.174	3,363	4.287	3,531	3%	5%
P3	5,809	4.459	3,626	4.592	3,810	3%	5%
P4	4,522	3.586	2,983	3.634	3,076	1%	3%
P5	4,567	3.614	2,955	3.655	3,082	1%	3%
P6	4,689	3.683	3,043	3.764	3,178	2%	4%
P7	4,542	3.599	2,989	3.635	3,064	1%	3%
P8	4,532	3.595	2,980	3.641	3,081	1%	3%
P9	4,739	3.708	3,055	3.791	3,190	2%	4%