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Abstract

In this paper, we present an exhaustive study on the influence of resistive-open defects in pre-charge circuits of SRAM memories. In SRAM memories, the pre-charge circuits operate the pre-charge and equalization at a certain voltage level, in general Vdd, of all the couples of bit lines of the memory array. This action is essential in order to ensure correct read operations. We have analyzed the impact of resistive-opens placed in different locations of these circuits. Each defect studied in this paper disturbs the pre-charge circuit in a different way and for different resistive ranges, but the produced effect on the normal memory action is always the perturbation of the read operations. This faulty behavior can be modeled by Un-Restored Write Faults (URWFs) and Un-Restored Read Faults (URRFs), because there is an incorrect pre-charge/equalization of the bit lines after a write or read operation that disturbs the following read operation. In the last part of the paper, we demonstrate that the test of URWFs is more effective in terms of resistive defect detection than that of URRFs and we list the necessary test conditions to detect them.

Keywords: Memory testing, dynamic faults, resistive-open defects, pre-charge circuits.

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Analysis and Test of Resistive-Open Defects in SRAM Pre-Charge Circuits [*]

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In this paper, we present an exhaustive study on the influence of resistive-open defects in pre-charge circuits of SRAM memories. In SRAM memories, the pre-charge circuits operate the pre-charge and equalization at a certain voltage level, in general Vdd, of all the couples of bit lines of the memory array. This action is essential in order to ensure correct read operations. We have analyzed the impact of resistive-opens placed in different locations of these circuits. Each defect studied in this paper disturbs the pre-charge circuit in a different way and for different resistive ranges, but the produced effect on the normal memory action is always the perturbation of the read operations. This faulty behavior can be modeled by Un-Restored Write Faults (URWFs) and Un-Restored Read Faults (URRFs), because there is an incorrect pre-charge/equalization of the bit lines after a write or read operation that disturbs the following read operation. In the last part of the paper, we demonstrate that the test of URWFs is more effective in terms of resistive defect detection than that of URRFs and we list the necessary test conditions to detect them.

1. Introduction

Memory density will continue to grow over the next years according to Moore's Law. This is confirmed by the SIA Roadmap which forecasts a memory density approaching 94% of System on Chip (SoC) silicon area in the next ten years [SIA05]. Moreover, memory will continue to be used as a process development vehicle for new digital technologies. Therefore, memories are becoming the main contributor of the overall SoC yield loss. Consequently, efficient test solutions and repair schemes for memories are needed.

Memory test solutions are generally based on functional fault models such as stuck-at, transition and coupling faults [Goo98, Ada03]. However, these faults models are nowadays insufficient to test the effects produced by some defects that may occur in VDSM (Very Deep Sub-Micron) technologies. Improvements in manufacturing process in terms of memory density have led to the development of new fault models, which are tightly linked

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to the internal memory structure. These fault models need specific test solutions. Moreover, the presence of resistive-open defects is becoming more and more important, due to the ever-growing number of interconnections between the layers. In particular, it is reported in [Nee98] that open/resistive vias are the most common origin of test escapes in deep-submicron technologies.

Recent researches show that resistive-open defects in VDSM technologies more and more frequently involve dynamic faults [Goo00, Al01]. These faults can be sensitized only by performing more than one operation in sequence and traditional tests are not made to detect them [Ham03]. In our recent studies we have analyzed dynamic faults in different parts of SRAM memories. In particular we have studied the faults occurring in the address decoders [Dil03, Dil04a] and in the core-cells [Dil04b, Dil05]. In both cases we have investigated the electrical causes of the dynamic faults and we have proposed efficient March procedures to detect them.

In this paper we propose an analysis of dynamic faults produced by the presence of resistive-open defects in the pre-charge circuits of SRAM memories. We have introduced resistive-open defects in some locations of a pre-charge circuit and we have performed electrical simulations in order to evaluate their effects. We have analyzed the functional influence of each single defect in the memory operation. We have demonstrated that all the defects involve a certain imbalance of the voltage level of the bit lines (BL and BLB) connected to the defective pre-charge circuit. This imbalance disturbs the correct action of the read operations. The fault models associated to the analyzed defects are URWF (un-Restored Write Fault) and URRF (Un-Restored Read Fault). In the last part of the paper, we evaluate the capability of both fault models and show that the detection of URWF is more effective than URRF to detect smaller resistive defects. We also report the necessary conditions to detect URWF and URRF as well as the existing test algorithm.

The rest of the paper is organized as follows. In Section 2, we describe in detail the pre-circuits. Section 3 gives experiments relative to the resistive-open defects in a pre-charge circuit: analysis of the incidence of each defect, experimental conditions and simulation results. In Section 4, we study the test of fault models relative to the defect injection. Conclusions and perspectives are given in Section 5.

2. Introduction on pre-charge circuits

In this section, we introduce some elements on SRAM pre-charge circuits. In all SRAM memories, for each cell column in the cell array there is a couple of bit lines, BL and BLB. Each couple of bit lines is connected to a pre-charge circuit. The function of this circuit is the pull-up at Vdd of the two bit lines every time the column is not selected and, in particular, before the read operations. In fact, for the read operations, the two bit lines, connected to the cell to be read, have to be at a certain voltage level, generally Vdd, and perfectly equalized. A typical pre-charge circuit is depicted in Figure 1. It is composed by two PMOS transistors, that when are in state *on*, connect the bit lines among them and to Vdd.

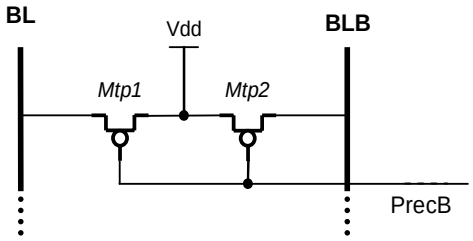

Figure 1: Two-transistor pre-charge circuit

Nowadays, the two-transistor pre-charge structure proposed in Figure 1 has been substituted by a three-transistor configuration depicted in Figure 2. With the redundant transistor Mtp1, this structure allows a lower sensitivity to the presence of resistive-open defects. This is demonstrated in the following.

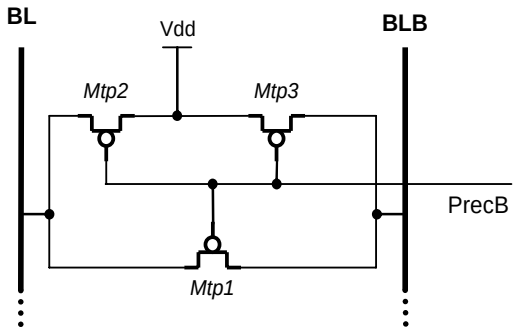

Figure 2: Three-transistor pre-charge circuit

The pre-charge circuit, depicted in Figure 2, circuit used three PMOS transistors with the single command signal PrecB. Transistors Mtp2 and Mtp3 connect the bit lines with the Vdd source for the pull-up. Transistor Mtp1 connects the two bit lines for their equalization. In many cases, when one of the two bit lines is already at Vdd, Mtp1 helps the pull-up of the other bit line.

Now, we describe with some details the normal action of the pre-charge circuit and its role in the memory operation. As mentioned above, in the memory structure there is a pre-charge circuit for each couple BL/BLB, as we can observe in the simplified scheme of Figure 3 that depicts a portion of an SRAM memory array. In the normal operation of the memory, the pre-charge circuit is most of the time activated and its action is to set the voltage level of each couple of bit lines at a certain value, Vdd for most of memories and also for Infineon 0.13µm embedded SRAM memories.

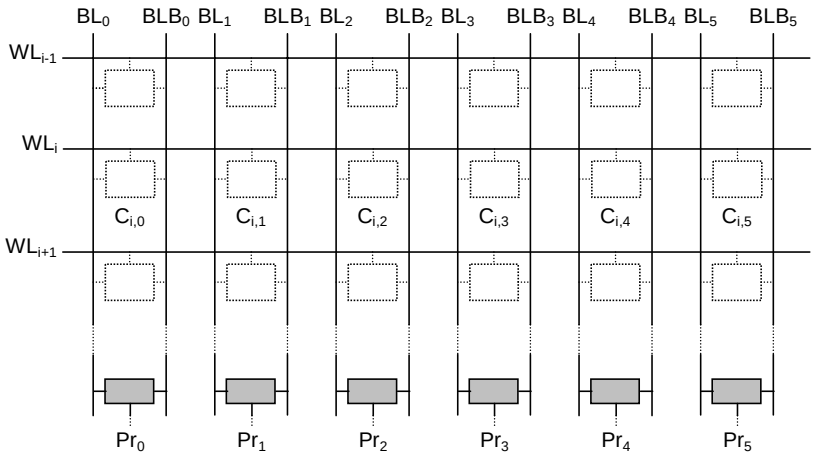

Figure 3: A portion of an SRAM cell array with pre-charge circuits

The fact that each bit line couple (BL and BLB) has to be exactly at Vdd level, is required for a correct read operation. In fact, when a read operation is operated on a certain cell, the pre-charge circuit is turned off on the two bit lines belonging to the selected cell. At this point, these bit lines are floating and charged at Vdd and the read operation can start. The read operation begins when the Word Line enable (WLe) signal allows the connection of the cell with its two bit lines. At this moment, one node of the cell is at the logic '1' (Vdd) and the other is at the logic '0' (0v). During the read operation, one of the two bit lines is partially discharged till to reach the voltage level Vdd - ΔBL with $\Delta BL = V_{BL} - V_{BLB}$. A sense amplifier detects this different voltage level between the two bit lines and gives the corresponding logic value. The read value is a logic '0' when BL is partially discharged (Vdd - ΔBL) and BLB remains at Vdd. A logic '1' is read in the opposite case.

Consequently, it is crucial that before any read operation the two bit lines connected to the cell were perfectly charged at Vdd and equalized. Any voltage difference between the two bit lines before the read operation may produce an incorrect read value, because the read operation itself is based on a ΔBL detection done by the sense amplifier. For this reason, the pre-charge circuit has not only Mtp2 and Mtp3 that feed their relative bit lines with a pull-up effect, but also transistor Mtp1 that ensure the equalization of the two bit lines.

3. Resistive-open defect in the pre-charge circuit

In this section we analyze the effects induced by resistive-open defects on the normal function of the pre-charge circuit. We consider the presence of only one defect for each analysis because the occurrence of multiple defects is unlikely to occur in a so small circuit.

As shown in Figure 4, five resistive-open defects (Df1 to Df5) have been placed in different locations of the analyzed circuit. We do not consider all possible locations because of the symmetry of the structure. In particular we have chosen the right part of the circuit for the asymmetric defects (Df1, Df3 and Df4). Defects Df2 and Df5 are symmetric, even if they may produce also asymmetric effects. Defect Df4' is not considered in the simulations because it produces effects very close to defect Df4. In fact, they are both placed in the same current path that feeds bit line BLB.

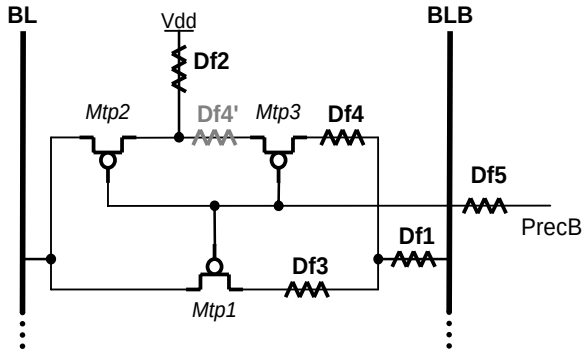

Figure 4: Resistive-open defects injected into the pre-charge circuit

3.1. Defect incidence analysis

Now, we analyze how the different defects in the pre-charge circuit can disturb the correct operation of the memory. We can first classify all the defects in two main categories:

- **Symmetric defects:** *In this group we consider defects Df2 and Df5 that produce a delay in the pre-charge of one of the two bit lines.*
- **Asymmetric defects:** *In this group we consider defects Df1, Df3 and Df4 that contribute to an asymmetric delay only in the pre-charge of BLB.*

As mentioned above, the asymmetric defects produce similar effects if they are placed on the left side of the circuit (the BL side). Each defect affects the memory behavior as follow:

- **Defect Df1:** This defect is asymmetric and without any doubt it is the most effective cause of faulty behavior because its action not only prevents the correct pull-up of BLB, but also blocks the equalizer effect of transistor Mtp1. Conversely, in presence of defect Df1, Mtp1 contributes to feed the asymmetric charge of BL.
- **Defect Df2:** This defect is symmetric and prevents the correct charge flow from the alimentation Vdd to the two bit lines. Defect Df2 may cause a faulty behavior when, before the pre-charge action, a bit line is at Vdd and the other is at 0v, for example we consider V_{BL} = Vdd and V_{BLB} = 0V. In this case

there is a delay in the flow of the charge from Vdd to BLB and at the end of the action there is a starting ΔBL already before the read operation. The effect of the defect on the read operation is strongly reduced by the presence of transistor Mtp1. In fact, even if the Vdd level is not reached by both bit lines, Mtp1 ensures their equalization useful for a correct read.

- **Defect Df3:** This defect is asymmetric and implies some problems in terms of pre-charge and equalization. In fact, if Mtp2 and Mtp3 were not very large, the action of Mtp1 could be crucial. When the initial state is V_{BL} = Vdd and V_{BLB} = 0V and the pre-charge is acted, the sole transistor Mtp3 may not be sufficient to pull-up BLB to Vdd. In a defect free circuit, the charge furnished by transistor Mtp2 helps the pull-up of BLB through transistor Mtp1 (BL is already at Vdd). Moreover, when the two transistors Mtp2 and Mtp3 are activated, they contribute to the equalization of the bit lines. This fact explains that the memory can behave correctly even in presence of defect Df3. It could be different for of very high operation frequency or in presence of smaller transistor size. In these cases the pull-up time could be not sufficient to set correctly both bit lines at same voltage level.
- **Defect Df4:** This defect is asymmetric and disturbs the correct pull-up of BLB. The effect of Df4 is partially reduced by the presence of transistor Mtp1 that contribute to pull-up the bit line at lower voltage level (BLB), taking the charge from Mtp2 and the opposite bit line (BL), already at Vdd. In practice, the two bit lines are charged by the sole transistor Mtp2, but BL could be more charged than BLB, because the current flows only through one transistor (Mtp2) and not two (Mtp2 and Mtp1). The comments given for defect Df3, in terms of frequency and transistor size, are still valid for Df4.
- **Defect Df5:** This defect is symmetric and implies a faulty behavior of the memory. This defect may represent the resistive effect of the connection of the pre-charge command signal. The main difference with defect Df2 is that in this case there is a double delay action: the delay in the pull-up acted by transistors Mtp2 and Mtp3 and the delay in the equalization effect done by transistor Mtp1. The faulty behavior may appear for high values of resistance because the defect is placed at the gates of the pre-charge transistors. No bias current enters in the PMOS transistor gate, thus the resistive defect has to be large enough to generate a sufficient delay that may involve a faulty behavior.

This analysis shows that each defect disturbs the pre-charge circuit in a different way, but the produced effect on the normal memory function is always the perturbation of the read operations. In fact, the defects involve an incorrect pre-charge/equalization of the bit lines after a write or read operation that disturbs the following read operation.

3.2. Experimental results

In order to validate the previous analyses, we have performed electrical simulations of the pre-charge circuit implemented in Infineon 0.13µm embedded SRAM memories, using the Infineon internal SPICE-like simulator. We have considered a reference 8Kx32 memory structure, organized as an array of 512 word lines by 512 bit lines. In order to reduce the simulation time, the simulations have been performed using a simplified version of the memory circuit that includes a reduced set of core-cells and all peripherals of the memory as sense amplifiers, write drivers, output buffers, the column and row address decoders and the pre-charge circuits. The working conditions chosen for all the simulations are the same for every defect, and are relative to the following parameters:

- *Process corner:* *Typical*
- *Supply voltage:* *1.5V*
- *Temperature:* *27°C*
- *Cycle time:* *3 ns*
- *Resistance values have been swept from a few Ωs up to several MΩs since a large range of possible values have been reported [Rod02].*

In this sub-section we present the experimental results obtained with the parametric simulations. For each defect, we have operated both w0r1 and r0r1 sequences on two cells belonging the same bit line. The results are summarized in Table 1. The first column lists the resistive-open defects. The second gives the faulty effects and the minimum resistance values that involve the faulty behavior. Note that, fault models related to defect injection reported in Table 1 are independent of PVT conditions. Only the minimum defect size from which we can observe the fault will change for other PVT conditions.

Defect	Fault models	Minimum resistance
Df1	URWF/URRF	2 kΩ / 4kΩ
Df2	No fault (low BLs voltage)	-
Df3	No fault (weak ΔBL)	-
Df4	No fault (weak ΔBL)	-
Df5	URWF/URRF	35 kΩ / 250 kΩ

Table 1: Summary of simulations with related fault models and corresponding minimum detected resistance

The first analysis of Table 1 shows that the pre-charge circuits are sensible only to defects Df1 and Df5. These defects produce a faulty behavior from a certain resistive value. Defect Df2 involves an incorrect pull-up of the bit lines, which does not disturb enough the read operation. In fact, although the Vdd is not reached, the redundant pre-charge structure ensures a good equalization that allows a successful read operation. In presence of Df3 and Df4, at the end of the pre-charge action there is an incorrect ΔBL, which is not large enough to imply a faulty behavior of the memory. These results show that the three-transistor pre-charge structure (with the redundant transistor Mtp1) is less sensitive to resistive-open defects than the two-transistor configuration.

The two fault models, relative to defects Df1 and Df5 are URWF and URRF [Ada97]. Their definitions are the following:

- **Un-restored Write Fault (URWF)**: *the pull-up of the two bit lines is not completely acted after the state reached with a **write** operation. Consequently the following read operation of an opposite data in a cell of the same column is not correctly acted.*
- **Un-restored Read Fault (URRF)**: *the pull-up of the two bit lines is not completely acted after the state reached with a **read** operation. Consequently the following read operation of an opposite data in a cell of the same column is not correctly acted.*

These two fault models can be classified as **dynamic faults** [Goo00, Al01, Ham03]. In fact, for their sensitization the **test patterns** are composed by sequences of two operations:

- *URWF test pattern:* wD on cell C_x, $r\overline{D}$ on cell C_y; where $D \in \{0, 1\}$ and $\overline{D}$ its complementary value; cells C_x and C_y belong to the same column.
- *URRF test pattern:* rD on cell C_x, $r\overline{D}$ on cell C_y; where $D \in \{0, 1\}$ and $\overline{D}$ its complementary value; cells C_x and C_y belong to the same column.

As example, in Figure 5 we report the waveforms obtained with the simulations of a pre-charge circuit affected by defect Df1, with the detection pattern of URRF (Figure 5.a) and the detection pattern of URWF (Figure 5.b). For both cases we have chosen for defect Df1 the same resistive value.

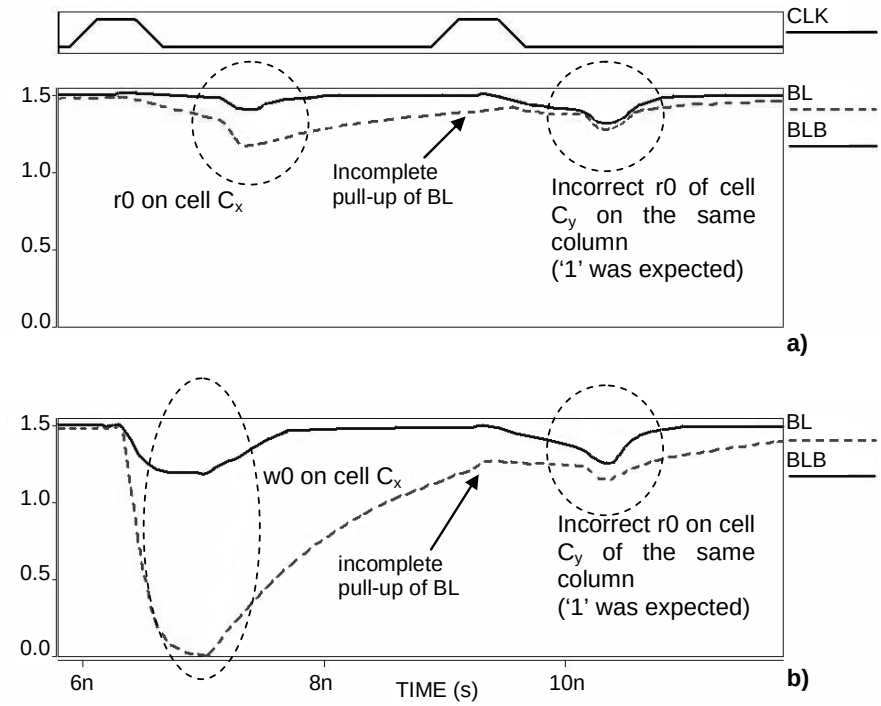

Figure 5: Simulation with defect Df1 in the pre-charge circuit a) URRF and b) URWF

Figure 5.a (URRF): A logic '0' is previously stored in cell C_x. A r0 is operated on cell C_x. At the end of this operation the pre-charge circuit operates the pull-up of the bit lines connected to C_x, in particular BL that is lower than Vdd due to the r0 operation. At the end of pre-charge action, bit line BL is not at Vdd as expected, because of presence of defect Df1. Consequently, the following read operation on cell C_y, belonging to the same column and containing a logic '1', is incorrect. In fact, $\Delta BL = VBL - VBLB < 0$ corresponds to a r0, while a logic '1' was expected.

Figure 5.b (URWF): A w0 is acted on cell C_x. At the end of this operation the pre-charge circuit operates the pull-up of the bit lines connected to C_x, in particular BL that is at logic '0' after the w0 operation. At the end of pre-charge action, bit line BL is not at Vdd as expected, because of presence of defect Df1. Consequently, the following read operation on cell C_y, belonging to the same column and containing a logic '1', is incorrect. In fact, $\Delta BL = V_{BL} - V_{BLB} < 0$ corresponds to a r0, while a logic '1' was expected.

4. Test of pre-charge dynamic faults

In this section, we describe in detail the conditions that are useful for the sensitization and the observation of URRFs and URWFs. We demonstrate which of them is more effective in terms of resistive defect detection. In the second part of this section, we propose an analysis on the frequency dependence for the pre-charge faults test. In the last part, we present an existing March test solution for URWF detection.

4.1. Sensitization and observation conditions

In this section we discuss with more detail the conditions required for the sensitization and the observation of the URRFs and URWFs that are caused by the resistive-open defects Df1 and Df5 in the pre-charge circuit. In order to make an easier presentation of the involved electrical phenomena, it is practical to consider a global delay fault produced on the pull-up of the one of the two bit lines; in particular for our example we choose BLB. This simplification is allowed because the resistive-open defects Df1 and Df5 cause URRFs and URWFs

by producing a delay in the pull-up of one bit line. Moreover, in the case of defect Df1, this defect has its homologue on the other side of the pre-charge circuit, where it presents identical consequences, but requiring inversed detection sequences.

As mentioned in the previous section, the requirement to detect the pre-charge faulty behavior is the operation of a read action just after a faulty pull-up of BLB (BL in the symmetric case). In fact, the incorrect balancing of the two bit lines involves a starting ΔBL (= δ) value that may disturb the correct reading. In order to emphasize the delay in the pull-up of BLB, it is useful that, just before the read operation, BLB is pulled-down as more as possible. This is possible by acting an r1 or w1 operation on a cell connected to the considered bit lines before the r0 operation (see Figure 6).

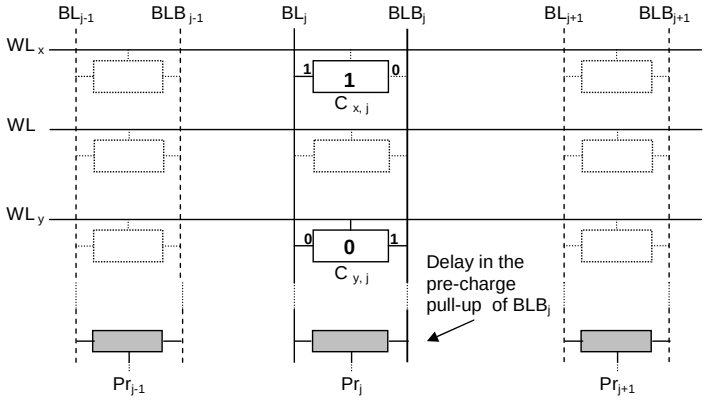

Figure 6: Scheme for URWFs and URRFs sensitization

We first act a w1 (or r1) on the cell $C_{x,j.}$ At the end of this operation BL_j is at Vdd and BLB_j is close to 0v, and the pre-charge circuit operates the pull-up of BLB. When the following r0 operation is acted on the cell $C_{y,j}$, the pull-up of BLB is not completed because of the faulty action of the pre-charge circuit. Consequently, at the beginning of this read operation the two bit lines are not equalized. In fact V_{BL} = VDD and V_{BLB} = VDD - δ. During the r0 operation BL is discharged by the cell $C_{y,j}$ left node, reaching:

$$V_{BL} = VDD - \Delta BL \quad (1)$$

On the other side, BLB is partially charged by the right cell node (that is at Vdd) reaching:

$$VBLB = VDD - \delta + \gamma \quad (2)$$

The read operation is acted by a sense amplifier that detects the differential voltage between the two bit lines. In Infineon 0.13µm memories for a correct read operation this difference has to be at lest 80mv. In particular for a correct r0 it is necessary that:

$$V_{BL} - V_{BLB} = \Delta BL < -80 \text{ mV} \quad (> +80 \text{ mV for a r1}) \quad (3)$$

In the case of a faulty pre-charge circuit at the end of the r0 operation, using the expressions (1) and (2), we have the following result:

$$VBL - VBLB = (VDD - \Delta BL) - (VDD - \delta + \gamma) = \delta + \Delta BL - \gamma \quad (4)$$

When the value of δ is of the same order or larger than ΔBL, the condition for a correct read operation may be not respected, and in particular we can have two different cases:

- ***Uncertain read***: - 80 mV < V_{BL}-V_{BLB}< 80 mV, the voltage difference is not close to the *safety* value given in expression (3), and it is in a range that does not allow the sense amplifier to operate a sure detection.
- ***Incorrect read***: V_{BL} - V_{BLB} > 80 mV, the read value is a logic '1' instead of the expected logic '0'.

As mentioned before, there are two fault models relatives to this faulty behavior that depend from the sequence used for sensitization and observation. The first is the URRF, whose detection sequence is r0 (r1) operated on a cell and r1 (r0) on another cell connected to the same bit line. The second is the URWF, whose detection sequence is w0 (w1) operated on a cell and r1 (r0) on another cell connected to the same bit line.

We have performed SPICE simulations in order to evaluate the effectiveness of the detection sequences. The result that clearly emerges from the simulation is that the sequences relative to the URWF are more effective than those relative to URRF. This result is easily visible in waveforms of Figure 7 that depict an example of simulation of the two sequences r0/r1 (URRFs sensitization sequence) and w0/r1 (URWFs sensitization sequence) with a pre-charge circuit affected by a defect symmetric to Df1. The operation conditions are the following:

- *Process corner:* *Slow*
- *Supply voltage:* *1.35V*
- *Temperature:* *125°C*
- *Df1 value:* *100 Ω < RDf1 < 10kΩ*

These conditions are different to the ones used in Table 1 as here we want also to highlight the worse case PVT corner, *i.e.* PVT conditions allowing the detection of the smallest resistive value of the defect. Compared to data of Table 1 considering typical PVT conditions, here we obtain a minimum resistance for Df1 about 430Ω and 700Ω for URWF and URRF respectively.

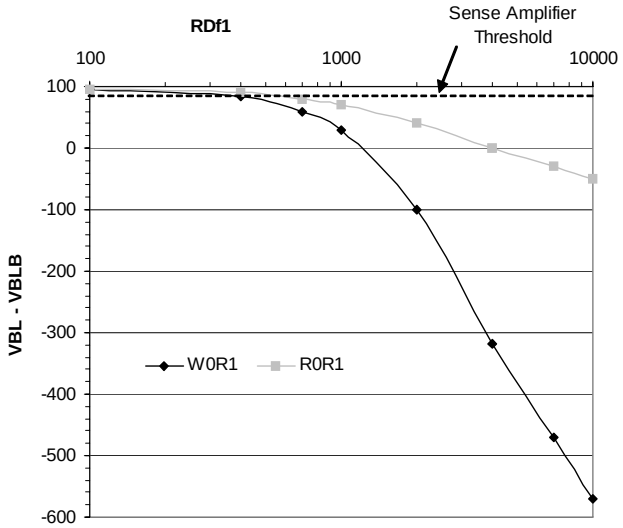

Figure 7: Parametric simulation of the sequences w0r1 and r0r1, in presence of defect Df1

In Figure 7, the curves show that for similar resistive value the points relative to the W0R1 sequence correspond to V_{BL} - V_{BLB} value less close to the *safety* area (V_{BL} - V_{BLB} > 80 mV) than the equivalent points of the R0R1 sequence. We have obtained similar results for other conditions and also for defect Df5.

On the base of these data we can state that the most performing test procedures are those that use the sensitization of URWFs. The others that use the URRF sensitization can be also used, but they are effective only for a higher resistive range.

4.2. Influence of the frequency in pre-charge fault test

As some other memory faults caused by the presence of resistive-open defects in an SRAM, URWFs and URRFs are the consequence of signal delay or delay of some circuit elements to reach a certain state; in this case, the state of charge (voltage level) of the bit-lines due a faulty function of the pre-charge circuit. For this reason, it is useful to investigate the dependence of the fault occurrence in relation with the clock cycle period. For this purpose, we have performed SPICE simulations on SRAM memory, considering the test patterns for URWFs and URRFs, checking the occurrence of faulty memory behavior for different clock cycle periods. The operation conditions are the following:

- *Process corner:* *Slow*
- *Supply voltage:* *1.35V*
- *Temperature:* *125°C*
- *Df1 value:* *100 Ω < RDf1 < 10kΩ*

As for Figure 7, these conditions are relative to the worst case, *i.e.* they allow the detection of the smallest resistive value of the defect.

From these simulations, we can observe that the sequences relative to the URWF test are more effective for shorter clock cycle period, *i.e.* for higher operation frequency. This result is easily visible in the graph in Figure 8 that depicts an example of simulation of the test sequence W0R1 with a pre-charge circuit affected by a defect symmetric to Df1.

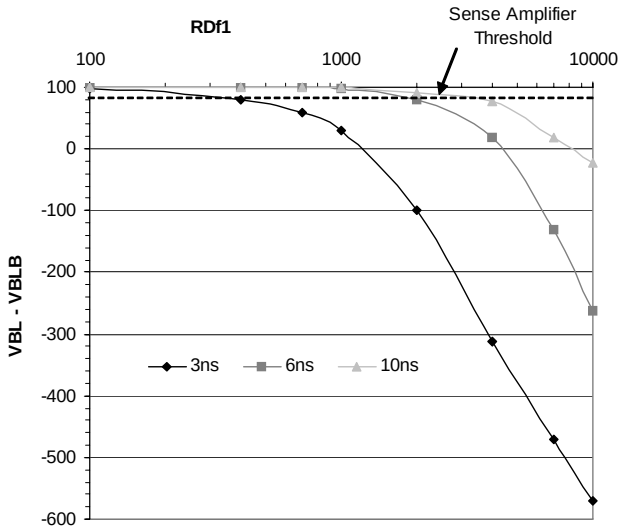

Figure 8: Parametric simulations of the test sequence w0r1, in presence of defect Df1, at different frequency

In Figure 8, the curves show that for similar resistive value the points, relative to higher frequency (shorter clock cycle period), correspond to V_{BL} - V_{BLB} value less close to the *safety* area (V_{BL} - V_{BLB} > 80 mV) than the equivalent points at lower frequency. We have obtained similar results for other conditions and also for defect Df5. The analysis of the results shows that the observation of URWFs and URRFs is more effective at higher

frequencies (shorter clock cycle period). Consequently, an important condition to obtain the best test efficiency is to perform the test at-speed.

4.3. Existing test solution for URWFs

In the literature, there are some march-like algorithms that allow the detection of URWFs and that are consequently able to cover the presence of the defects in the pre-charge circuits. Among these, we consider the test pattern proposed in [Ada97, Nig98]. We have shown in the previous sections that the URWF detection requires writing a certain data D in a cell and reading its complementary value $\overline{D}$ exactly during the next memory access in another cell belong the same pair of bit line. The March-like test proposed in [Ada97, Nig98] has complexity 5N and is a particular implementation of March MATS+ (see Figure 9).

$$\Updownarrow(w0)\ \Uparrow(r0, w1)\ \Downarrow(r1, w0)$$
$$M_0 \qquad M_1 \qquad M_2$$

Figure 9: MATS+ algorithm

The first element M_0 operates a w0 on all the cells of the memory. The second element M_1 is not implemented as a normal March test, but with the particular addressing order bit line after bit line. This means that, for a 1-bit transition of the column address decoder, all the possible transitions on the row address decoder are exploited. This is allowed by the first degree of freedom of March test [Nig98]. Figure 10 shows the process of element M_1 for three addresses, belonging to the same bit line couple. The sensitization phase is enabled by the couple of operations w1 on cell at the address A_i and r0 on cell at the address A_{i+1}. The observation phase corresponds to the r0 operation.

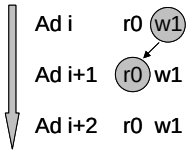

Figure 10: Process of the element $\Uparrow(r0, w1)$

As demonstrated in the previous sections, this element is able to detect only a part of the possible URWFs and, in particular, those that are induced by the symmetric resistive-open defects and the asymmetric resistive-open defects placed on the right side of the pre-charge circuit. For the test of the URWFs caused by the left-placed resistive-open defect, the element M_2 is required. The process of this element is similar to element M_1 and the sensitization phase is done by the couple of operations w0 on cell at the address A_i and r1 on cell at the address A_{i+1}, as shown in Figure 11.

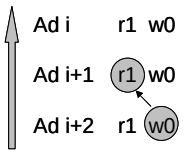

Figure 11: Process of the element $\Downarrow(r1, w0)$

Many other March-like test algorithms can detect URWFs and URRFs, as March C-, as long as they contain write/read operations and an addressing order row by row.

5. Conclusions and perspectives

In this work we have performed the characterization and analysis of the effects of resistive-open defects in the pre-charge circuit of SRAM memories. We have found that all the considered defects disturb the pull-up of at least one of two bit lines connected to the pre-charge circuit. The consequence of this missing complete pull-up may involve an unbalanced voltage level of the two bit lines. This condition disturbs the read operation of the cells connected to the affected bit lines. The fault models relative to this faulty behavior are Un-restored Write fault and Un-restored Read fault, which have been detected only for defects Df1 and Df5. The circuit is less sensible to the presence of defects Df2, Df3 and Df4. In the last part of the paper we have analyzed the effectiveness of the test patterns to cover the two fault models and we have demonstrated that the URWF pattern is the most effective. We have also presented the necessary test conditions to detect them. The next step in this work will be to develop new March-like algorithms targeting resistive-open defects in other parts of SRAMs (sense amplifiers, write drivers, etc.).

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