Scan Cell Reordering for Peak Power Reduction during Scan Test Cycles

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Abstract. *Scan technology increases the switching activity well beyond that of the functional operation of an IC. In this paper, we first discuss the issues of excessive peak power during scan testing and highlight the importance of reducing peak power particularly during the test cycle (i.e. between launch and capture) so as to avoid noise phenomena such as IR-drop or Ground Bounce. Next, we propose a scan cell reordering solution to minimize peak power during all test cycles of a scan testing process. The problem of scan cell reordering is formulated as a constrained global optimization problem and is solved by using a simulated annealing algorithm. Experimental evidence and practical implications of the proposed solution are given at the end of the paper. For ISCAS'89 and ITC'99 benchmark circuits, this approach reduces peak power during TC up to 51% compared to an ordering provided by an industrial synthesis tool. Fault coverage and test time are left unchanged by the proposed solution.*

1 Introduction

While many techniques have evolved to address power minimization during the functional mode of operation, it is now mandatory to manage power during the test mode. Circuit activity is substantially higher during test than during functional mode, and the resulting excessive power consumption can cause structural damage or severe decrease in reliability of the circuit under test (CUT) [1-4].

The problem of excessive power during test is much more severe during scan testing as each test pattern requires a large number of shift operations that contribute to unnecessarily increase the switching activity [2]. As today's low-power designs adopt the approach of "just-enough" energy to keep the system working to deliver

the required functions, the difference in power consumption between test and normal mode may be of several orders of magnitude [3].

In this paper, we first discuss the issues of excessive peak power consumption during scan testing. As explained in the next section, peak power consumption is much more difficult to control than average test power and is therefore the topic of interest in this paper. We present the results of an analysis performed on scan version of benchmark circuits, showing that peak power during the test cycle (i.e. between launch and capture) is in the same order of magnitude than peak power during the load/unload cycles. Considering that i) logic values (i.e. test responses) have to be captured/latched during the *test cycle* (TC) while no value has to be captured/stored during the load/unload cycles, and ii) TC is generally operated at-speed, we highlight the importance of reducing peak power during TC so as to avoid phenomena such as IR-drop or ground bounce that may lead to yield loss during manufacturing test.

In order to reduce peak power during the test cycles, a straightforward approach would consist in reducing the resistance of the power/ground nets by over sizing power and ground rails. This solution has the advantage to be simple to implement and has limited side effect, *i.e.* low area overhead. However, this solution requires early in the design flow an estimation of the increase in power consumption during test with respect to power consumption during functional mode. As test data are generally not available at the early phases of the design process, this solution may not be satisfactory in all cases.

Therefore, we propose a possible solution based on scan cell reordering. Scan reordering has already been shown to be efficient to reduce power during test [5, 6, 7]. From a set of scan cells and a sequence of deterministic test vectors, a heuristic process provides a scan chain order that minimizes the occurrence of transitions and hence the peak power during TC. As reducing peak power during all test cycles of the test session - while maintaining each vector under the limit - is shown to be more important than targeting only one or few vectors exceeding a power limit, the problem has been formulated as a constrained global optimization problem. Considering its exponential nature, we have proposed a heuristic based on simulated annealing (SA) which provides good results. For ISCAS'89 and ITC'99 benchmark circuits, this approach reduces peak power during TC up to 51% compared to an ordering provided by an industrial synthesis tool. Fault coverage and test time are left unchanged by the proposed solution.

The rest of the paper is organized as follows. In the next section, we discuss peak power issues during scan testing. In Section 3, we analyze peak power during the test cycles of scan testing and we highlight the importance of reducing this component of the power. In Section 4, we first describe how peak power is estimated in the proposed approach, and we present the scan reordering technique proposed to solve this combinatorial optimization problem. In the last part of Section 4, practical implications of this approach are discussed. Results obtained on benchmark circuits are reported in Section 5. Finally, Section 6 concludes the paper and gives the perspectives of this study.

2 Peak power issues

Power consumption must be analyzed from two different perspectives. Average test power consumption is, as the name implies, the average power utilized over a long period of operation or a large number of clock cycles. Instantaneous power or peak power (which is the maximum value of the instantaneous power) is the amount of power required during a small instant of time such as the portion of a clock cycle immediately following the system clock rising or falling edge. In [4], it is reported that test power consumption tends to exceed functional power consumption in both of these measures.

Average power consumption during scan testing can be controlled by reducing the scan clock frequency – a well known solution used in industry. In contrast, peak power consumption during scan testing is independent of the clock frequency and hence is much more difficult to control. Among the power-aware scan testing techniques proposed recently (a survey of these techniques is given in [8] and [9]), only a few of them relates directly to peak power. As reported in recent industrial experiences [3], scan patterns in some designs may consume much more peak power over the normal mode and can result in failures during manufacturing test. For example, if the instantaneous power is really high, the temperature in some part of the die can exceed the limit of thermal capacity and then causes instant damage to the chip. In practice, destruction really occurs when the instantaneous power exceeds the maximum power allowance during several successive clock cycles and not simply during one single clock cycle [3]. Therefore, these temperature-related or heat dissipation problems relate more to elevated average power than peak power. The main problem with excessive peak power concerns yield reduction and is explained in the sequel.

With high speed, excessive peak power during test causes high rates of current (di/dt) in the power and ground rails and hence leads to excessive power and ground noise (V_{DD} or Ground bounce). This can erroneously change the logic state of some circuit nodes and cause some good dies to fail the test, thus leading to unnecessary loss of yield. Similarly, IR-drop and crosstalk effects are phenomena that may show up an error in test mode but not in functional mode. IR-drop refers to the amount of decrease (increase) in the power (ground) rail voltage due to the resistance of the devices between the rail and a node of interest in the CUT. Crosstalk relates to capacitive coupling between neighboring nets within an IC. With high peak current demands during test, the voltages at some gates in the circuit are reduced. This causes these gates to exhibit higher delays, possibly leading to test fails and yield loss [10]. This phenomenon is reported in numerous reports from a variety of companies, in particular when at-speed transition delay testing is done [3]. Typical example of voltage drop and ground bounce sensitive applications is Gigabit switches containing millions of logic gates.

3 Analysis of peak power during scan

During scan testing, each test vector is first scanned into the scan chain(s). After a number of load/unload clock cycles, a last shift in the scan chain launches the test vector. The scan enable (SE) signal is switched to zero, thus allowing the test response to be captured/latched in the scan chain(s) at the next clock pulse (see Figure 1). After that, SE switches to one, and the test response is scanned out as the next test vector is scanned in.

There can be a peak power violation (the peak power exceeding a specified limit) during either the load/unload cycles or during TC. In both cases, a peak power violation can occur because the number of flip-flops that change value in each clock cycle can be really higher than that during functional operation. In [10], it is reported that only 10-20 % of the flip-flops in an ASIC change value during functional mode, while 35-40 % of these flip-flops commutate during scan testing.

In order to analyze when peak power violation can occur during scan testing, we conducted a set of experiments on benchmark circuits. Considering a single scan chain composed of *n* scan cells and a deterministic test sequence for each design, we measured the current consumed by the combinational logic during each clock cycle of the scan process. We pointed out the maximum value of current during the *n* load/unload cycles of the scan process and during TC (which last during a single clock cycle). Note that current during TC is due to transitions generated in the circuit by the launch of the deterministic test vector V_n (see Figure 1).

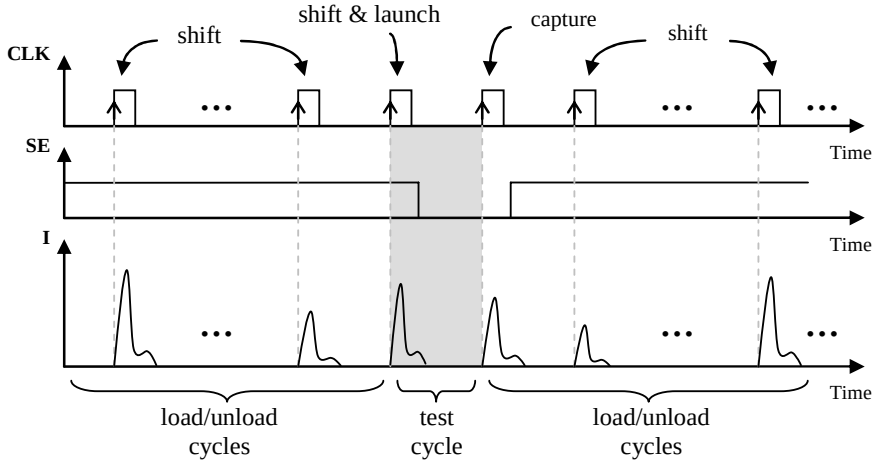

Figure 1. Scan testing and current waveform

Identification of peak power violation cannot be done without direct comparison with current (or power) measurement made during functional mode. However, this would require knowledge of functional data for each benchmark circuit. As these data are not available, the highest values of current we pointed out are not

necessarily peak power (current) violations. There are simply power (current) values that can lead to peak power (current) violation during scan testing. Reports made from industrial experiences have shown that such violations can really occur during manufacturing scan testing [3] [4].

The benchmarking process was performed on circuits of the ISCAS'89 and ITC'99 benchmark suites. We report in Table 1 the main features of these circuits. We give the number of scan cells, the number of gates, the number of test patterns and the fault coverage (FC) for each experimented circuit. All experiments are based on deterministic testing from the ATPG tool "TetraMAX™" of Synopsys [11]. The missing faults in the FC column are the redundant or aborted faults. Primary inputs and primary outputs were not included in the scan chain, but were assumed to be held constant during scan-in and scan-out operations. Random initial logic values were assumed for the scan flip-flops.

Table 1. Features of experimented circuits

Circuit	# cells	# gates	# patterns	FC (%)
b04s	66	512	58	99.08
b09	28	129	28	100
b10	17	155	44	100
b11s	31	437	62	100
b12	121	904	94	100
b13s	53	266	30	100
b14s	245	4444	419	99.52
b17	1415	22645	752	98.99
s298	14	119	29	100
s420	16	218	72	100
s526	21	193	56	100
s713	19	393	36	100
s1196	18	529	137	100
s1488	6	653	117	100
s5378	179	2779	151	100
s9234	228	5597	161	99.76
s13207	669	7951	255	99.99
s38417	1636	22179	145	100

Results concerning peak power consumption are given in Table 2. We have reported the peak power (expressed in milliWatts) consumed during the load/unload cycles (second column), and that consumed during TC (third column). These values are a maximum over the entire test sequence. Power consumption in each circuit was estimated by using PowerMill® of Synopsys [12], assuming a power supply voltage of 2.5 Volts and technology parameters extracted from a 0.25µm digital CMOS

standard cell library. These results show that peak power consumption is always higher during the load/unload cycles than during TC. This result was quite predictable as the number of clock cycles during the load/unload phase is much more than one. More importantly, these results show that even if peak power is higher during the load/unload cycles, peak power during TC is in the same order of magnitude. This may lead to problematic noise phenomena during TC whereas these phenomena do not impact the load/unload process. Let us consider again the IR-drop phenomenon. As discussed earlier, it is due to a high peak current demand that reduces the voltages at some gates in the CUT and hence causes these gates to exhibit higher delays. The gate delays do not affect the load/unload process as no value has to be captured/stored during this phase. Conversely, the gate delays can really affect TC because the values of output nodes in the combinational logic have to be captured in the scan flip-flops. As this operation is generally performed at-speed, this phenomenon is therefore likely to occur during this phase and negatively impact test results. We can therefore conclude that taking care of peak power during TC and trying to minimize the switching density of the circuit during this phase are really relevant and requires new development of dedicated techniques.

Table 2. Peak power during scan testing

Circuit	**Peak power consumption (mW)**	
	load/unload	*test cycle*
b04s	77.50	59.60
b09	34.43	30.48
b10	27.88	23.71
b11s	50.42	41.27
b12	113.84	101.46
b13s	61.09	52.92
b14s	395.55	319.83
b17	1009.96	962.23
s298	30.06	29.83
s420	48.15	27.87
s526	47.88	45.26
s713	23.57	18.76
s1196	66.89	10.03
s1488	81.86	76.83
s5378	197.76	179.66
s9234	359.68	339.88
s13207	445.82	402.70
s38417	1028.25	977.52

4 Scan cell ordering to reduce peak power

Considering the fact that minimizing peak power during TC is needed, we propose a possible solution based on scan cell reordering. From the set of scan cells and a pre-computed sequence of deterministic test vectors, a heuristic process provides a scan chain order that minimizes the occurrence of transitions and hence the peak power during TC.

4.1 Estimating peak power during TC

In the previous section, we reported that peak power during TC is due to transitions provoked in the circuit by the last scan shift that launches the deterministic test vector (Figure 1). In order to count the number of transitions generated during TC, and hence estimate the peak power consumption, we use a transition metric that has been shown to be strongly correlated to the switching activity at internal nodes of the CUT [13]. It consists in considering the pair of scan vectors (V_{n-1}, V_n), where V_{n-1} is the vector preceding test vector V_n, and count the number of bits that have changed value between the two vectors (i.e. the Hamming distance). This metric is a good way to accurately estimate the power consumed during TC and hence avoid time-consuming and size limited simulations during the search process. Actually, this metric can be simplified as it amounts to count the number of bit differences (0-1 or 1-0) in vector V_n of length *n*. So, it means that only one vector (the test vector V_n) among the *n* scan vectors has to be considered for peak power estimation during TC.

Note that for an exact estimation, we should also consider the extra bit difference that can occur when the first bit of a test vector differs from the last bit of the previous output response. However, as the number of bits in each test vector V_n is much greater than one for real-size circuits, this possible extra bit difference can be neglected.

4.2 Problem formulation

The problem of reordering scan cells to minimize peak power during TC can be tackled from two different perspectives. First, we can try to minimize peak power only for test vectors (among the *l* deterministic test vectors of the test sequence) that exceed a specified limit. This is a local optimization problem. In this case, the main difficulty consists in minimizing peak power for the vectors exceeding the limit without producing new “violation” vectors. The second way to tackle this problem is to try to minimize peak power during TC for all vectors of the test sequence while maintaining each vector under the limit. This is a constrained global optimization problem. In this case, the main difficulty consists in getting a significant reduction in peak power for all vectors while satisfying the constraint on the “violation” vectors. In Section 3, we reported that reducing peak power during TC is more important to avoid yield loss than to prevent temperature-related problems. This means that reducing peak power during all test cycles - while maintaining each vector under the limit - is more important than targeting only one or few vectors exceeding a power

limit. For this reason, we decided to search a solution for the constrained global optimization problem. Considering its exponential nature, we have proposed a heuristic solution that uses features of simulated annealing and solves the problem in a polynomial time. This solution is detailed below.

4.3 Scan cell reordering by simulated annealing

Scan cell reordering consists in determining the order in which the scan cells of a scan chain have to be connected to minimize the occurrence of transitions during all test cycles. It can be demonstrated that this combinatorial optimization problem is NP-hard - the number of possible solutions is n! where *n* is the number of scan cells in the scan chain. Due to its exponential nature, this problem cannot be solved by an exact method. Heuristics based on local search or evolutionary methods have therefore to be used [14].

We developed and implemented a heuristic solution based on Simulated Annealing (SA). SA has been used in various combinatorial optimization problems and has been particularly successful in circuit design problems [15]. As its name implies, SA exploits an analogy between the way in which a metal cools and freezes into a minimum energy crystalline structure (the annealing process) and the search for a minimum in a more general system. SA major advantage over other methods is its ability to avoid becoming trapped at local minima. The algorithm employs a random search which not only accepts changes that decrease a cost function f, but also some changes that increase it.

The different steps performed by the SA heuristic are represented in the flow chart of Figure 2. Inputs to this algorithm are a set of scan cells and the deterministic test vectors generated assuming a given order of these scan cells in the scan chain. The output is an ordered scan chain with minimum peak power during the test cycles. The algorithm starts by randomly generating a set of solutions and select the best one s_{opt} that satisfies the local constraint. The best solution is the one with the lowest cost $f(s_{opt})$ expressed as the number of bit differences over the entire test sequence. Then, the algorithm follows the two following main steps. First, a local search is made to find better solutions from the current optimum solution. Next, in order to escape from local minima, a global search is made in which solutions better than s_{opt} ($\Delta f < 0$) are accepted when the local constraint is satisfied, and solutions worse than s_{opt} ($\Delta f > 0$) can be accepted with a certain probability $p=\exp(-\Delta f/T)$. The temperature T is decreased during the search process so that the probability of accepting worse solutions gradually decreases.

Some definitions are now given to clarify the flow chart of Figure 2.

- *Generate new solution*: build a scan chain with a new order of the scan flip-flops.
- *Assess a solution*: count the number of bit differences in each vector of the deterministic test sequence. The cost of a solution is obtained by summing these numbers.
- *Verify local constraint*: verify if all the test vectors are under the power limit with the current ordering solution.

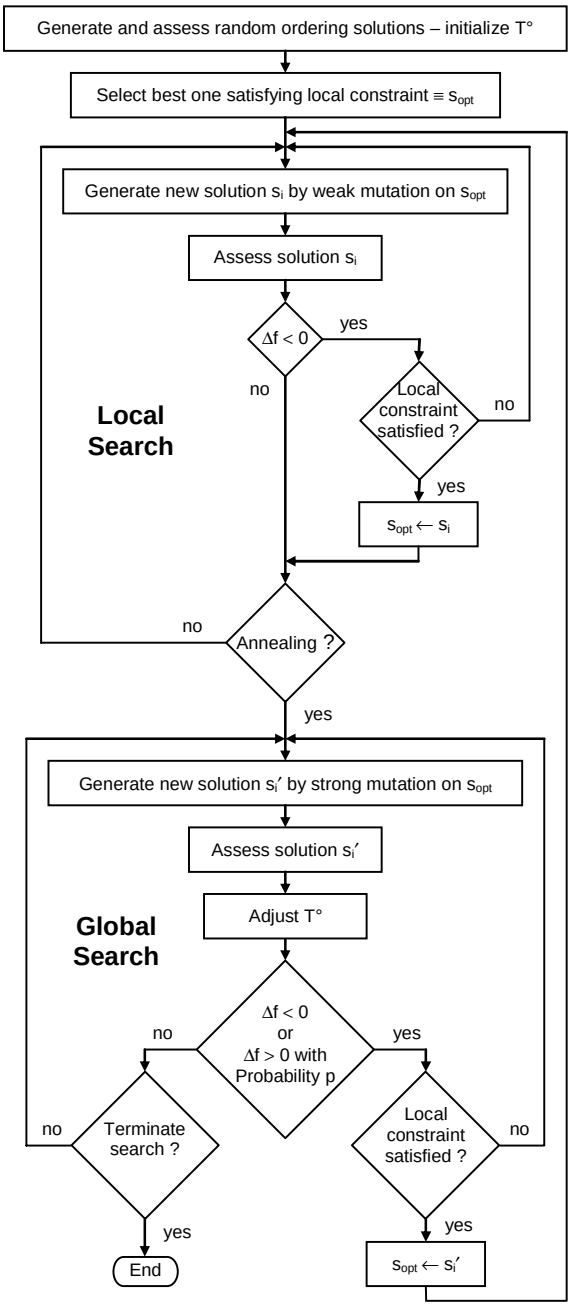

Figure 2. Scan reordering flow chart

- *Δf or verify the global constraint*: compare the cost of the current solution (s_i or s_i') with that of the best current solution s_{opt}. $\Delta f = f(s_i) - f(s_{opt})$.
- *Weak-mutation*: transposing few cells in the scan chain.
- *Strong-mutation*: transposing many cells in the scan chain.
- *Annealing*: is applied if no improvement of the best current solution s_{opt} is obtained after a given number of iterations.
- *Terminate search*: occurs after a given number of iterations in the algorithm has been done or after a solution with a predefined minimum cost has been found.

4.4 Practical implications

Compared with existing low power scan techniques, our solution offers numerous advantages. The proposed approach works for any conventional scan design - no extra DfT logic is required – and both the fault coverage and the overall test time are left unchanged. However, several practical implications of this solution have to be discussed.

First, the heuristic procedure does not explicitly consider constraints such as the placement of scan in and scan out pins or the existence of multiple scan chains with multiple clock domains in the CUT. In this case, the proposed technique has to be modified to allow these constraints to be satisfied. For example, scan chain heads and tails may be predefined and pre-assigned in the case of constraints on scan in and scan out pin position. This kind of pre-assignment may be important to avoid long wires between external scan/out pins and scan chain heads/tails.

In the case of circuits with multiple scan chains and multiple clock domains, which are common in industrial designs, almost no modification of the proposed technique is required. Actually, each scan chain can be considered separately and the heuristic procedure has to be applied successively on each scan chain.

In fact, the most important practical aspect which has to be addressed is the impact on routing. In VDSM technologies, routing is becoming a dominant factor in area, performance and power consumption. In traditional DfT flows, scan routing is also one of the main concerns when designing a scan chain. After scan synthesis, connecting all the scan cells together may cause routing congestion during the place-and-route stage of the design flow, resulting in area overhead and timing closure issues. To avoid congestion problems, scan chain optimization is traditionally used after placement. Formally, scan chain optimization is the task of finding a new order for connecting the scan elements such that the wire length of the scan chain is minimized. Several scan chain reordering solutions have been proposed recently to address the above stated problems [16, 17].

The main drawback of the scan ordering technique proposed in this paper is that power-driven chaining of scan cells cannot guarantee short scan connections and prevent congestion problems during scan routing. In this context, the use of a power-driven scan ordering technique, though efficient, is questionable. To avoid this situation, several solutions can be proposed depending on the DfT level at which the peak power problem is considered. First, if scan reordering can be performed before scan synthesis (in this case, flip-flop placement is not already done), the solution is

to consider a DfT synthesis tool that can accept a fixed scan cell order (produced by our heuristic) and from which it can optimally place and route the scan resources. Now, if scan reordering cannot be done before scan synthesis (in this case, flip-flop placement is known and fixed), a solution to consider routing is to apply a clustering process as the one developed in [7] that allows to design power-optimized scan chains under a given routing constraint. In this case, the routing constraint is defined as the maximum length accepted for scan connections. Results given in [7] have shown very good tradeoff between test power reduction and impact on scan routing. Note that in all situations, ATPG is done earlier in the design flow.

5 Experimental results

The goal of the experiments we performed has been to measure the reduction in peak power obtained during TC from the proposed scan cell ordering process. The results are summarized in Table 3.

Table 3. Peak power saving in the CUT during TC

Circuit	Industrial Solution	Proposed Ordering Technique	
	peak [mW]	*peak [mW]*	*reduct. (%)*
b04s	35.96	29.43	18.2
b09	18.91	9.22	51.2
b10	14.38	12.53	12.8
b11s	29.03	24.03	17.2
b12	82.13	63.73	22.4
b13s	39.97	27.60	30.9
b14s	197.17	172.87	12.3
b17	949.47	837.70	11.8
s298	17.11	13.16	23.1
s420	14.63	10.78	26.3
s526	25.79	20.02	22.4
s713	10.20	8.17	20.0
s1196	4.98	4.03	19.0
s1488	42.42	38.68	8.8
s5378	150.86	118.85	21.2
s9234	247.32	200.74	18.8
s13207	405.56	337.03	16.9
s38417	993.22	746.08	24.9

For each circuit, we report the peak power during TC obtained first from an ordering provided by an industrial tool and next with the proposed ordering technique. For the evaluation in both cases, we used the deterministic test sequences presented in Table 1 assuming random initial logic values for the scan flip-flops. The industrial ordering has been performed by using the layout synthesis tool Silicon Ensemble® of Cadence Design System [18]. In the context of our study, this synthesis tool allows first to perform scan insertion in the design corresponding to the experimented circuit and next the placement and routing of flip-flops in the design with respect to delay and area constraints. For each circuit, the design and the ordering of the scan chain have been carried out with a random placement of the scan-in and scan-out pins. Peak power is expressed in milliWatts and the values reported for each circuit are a mean of peak power (or instantaneous power) consumed during each test cycle of the scan process. Note that these values differ from those in Table 2 which represent a maximum over the entire test sequence.

The last column in Table 3 shows the reduction in peak power dissipation expressed in percentages. These results on benchmark circuits show that peak power reduction up to 51% can be achieved with the proposed ordering technique. Concerning computing CPU time, ordering solutions are obtained in less than 10 seconds for small circuits up to 2 minutes for big circuits. Simulations have been performed on a Sun Solaris 9 workstation with 2 gigabytes of RAM.

By reducing the number of transitions during TC for minimizing peak power consumption, we need to take care of the possible reduction in defect coverage, particularly for timing related defects. For this purpose, we have measured the transition fault coverage of the test sequence applied to each CUT with and without power-aware reordering. Results are listed in Table 4.

Table 4. Transition fault coverage

Circuit	**Non-Robust Transition Fault Coverage**	
	without reordering	*with power-aware ordering*
b11s	62.94	66.78
b12	64.61	61.07
b13s	63.60	64.95
b14s	69.10	66.05
b17	48.08	47.06
s1196	17.98	18.88
s1488	58.75	62.46
s5378	64.83	64.10
s9234	52.67	52.50
s13207	69.3	72.02
s38417	78.5	77.6

As can be seen, the non-robust transition fault coverage achieved when power-aware scan (bit) ordering is done (third column in Table 4) is roughly the same than that obtained without any power consideration (second column). This can be explained by the fact that our SA heuristic reduces the *mean* of peak power over all test cycles - while maintaining each vector under the limit. By this way, it may occur that the switching activity during some test cycles with a very low initial value is increased, thus compensating the decrease obtained on test cycles with a very high initial value. Anyway, results reported in Table 4 prove the efficiency of our technique to maintain initial defect coverage level.

In addition to these evaluations, we have performed another set of experimentation to measure the effectiveness of the proposed reordering technique on the peak power reduction during load/unload cycles. As previously, results are summarized in Table 5.

Table 5. Peak power saving in the CUT during load/unload cycles

Circuit	Industrial Solution	Proposed Ordering Technique	
	peak [mW]	*peak [mW]*	*reduct. (%)*
b04s	58.07	53.85	7.3
b09	29.05	26.09	10.2
b10	21.37	20.1	5.9
b11s	40.55	37.94	6.4
b12	97.89	82.45	15.8
b13s	49.49	46.78	5.5
b14s	335.8	329.7	1.8
s298	22.33	21.47	3.9
s420	21.5	19.57	9.0
s526	36.15	31.6	12.6
s713	18.39	18.23	0.9
s1196	36.53	36.85	-0.9
s1488	55.0	54.44	1.0
s5378	167.23	157.99	5.5
s9234	322.15	317.86	1.3

Results show that the proposed reordering solution provides a small reduction (about 5.7% in average) of the peak power during load/unload cycles and some time an increase as for the s1196. Such results were quite predictable as the reordering solution target only the TC. Based on this statement, our future work will therefore focus on the setting up of a new peak power technique allowing peak power reduction during TC but also during load/unload cycles.

6 Conclusions and future works

In this paper we have proposed a reordering technique for peak power reduction during the test cycle. Peak power reduction during TC up to 51% is achieved that avoid possible noise phenomena as ground bound and IR-drop.

As mentioned before, the main drawback of the scan ordering technique proposed in this paper is that power-driven chaining of scan cells cannot guarantee short scan connections and prevent congestion problems during scan routing. In addition, the proposed reordering technique does not enough reduce the peak power during load/unload cycles. Direction for the future of this work will be on power-aware test pattern modification. Recent studies and improvements made to ATPG tools have led to power-sensitive ATPG options, to create relatively low-power patterns for scan shifting. For example, wherever possible, ATPG can minimize internal state transitions during scan shifting by filling adjacent flip-flops with the same state, instead of using random fill. Evaluations have shown up 50 percent power reduction achieved with this approach. A similar approach targeting peak power reduction during TC will therefore be developed.

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