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A Comparative Study of Conditioning Architectures for Convective Accelerometers

O. Leman, F. Mailly, L. Latorre and P. Nouet

Microelectronic Dept. LIRMM – UMR 5506

University of Montpellier

Montpellier – France

Contact : mailly@lirmm.fr

Abstract— In this paper, we compare three different conditioning and readout electronics for CMOS convective accelerometers. The work is based on both characterization results and high-level simulations. The three following architectures are evaluated: (i) a simple amplifier, (ii) a chopper stabilized amplifier, and (iii) an innovative 1st-order thermal sigma-delta modulator. Experimental data are obtained using the hybrid combination of a $0.8\mu\text{m}$ CMOS integrated sensor and discrete electronics. Behavioral simulations were carried-out under Matlab®/Simulink® using small-signal models. The sensor model includes performance-limiting thermal phenomena and $1/f$ noise contributions. Previous studies describing the modeling of thermal sigma-delta modulators do not address device noise modeling, since most of the time, the performance of those modulators are limited by quantization noise. In our case, we show that the performance is limited by both the noise in the devices and the quantization noise.

I. INTRODUCTION

The measure of a temperature gradient in the neighborhood of a hot wire has been used for decades in several applications such as anemometers. More recently, this principle has been applied to inertial sensing in silicon devices [1]. These convective accelerometers are low-cost, shock-resistant due to the nonexistence of moving parts. Their fabrication only requires low-cost bulk etching techniques and their integration on standard technology such as CMOS is now common [2]. In modern consumer applications, seismic-mass based sensors are still leading the market. These are mature devices with very good sensing performance and low power consumption resulting from capacitive sensing strategy.

Although convective accelerometers are promising in terms of fabrication cost and integration compatibility, their performances and their power consumption are still to be improved. This study addresses conditioning and readout architecture for thermal devices with focus on these issues.

Three schemes are therefore compared: two well-known amplification techniques and a new application of the thermal sigma-delta modulator principle. Architectures are evaluated on a $\pm 2g$ measurement range and 1-20Hz bandwidth in terms of sensitivity and resolution. As the power consumption of the thermal device directly rules its sensitivity, it is assumed that a better resolution of the conditioning chain would somewhat allow for power reduction in the sensing element. The Matlab®/Simulink® environment is used to simulate the system performance, while an experimental validation is provided for each case.

Part II of the paper describes the sensor prototype. A special focus is given to the modeling approach. Note that the small-signal modeling of the thermal accelerometer including a noise implementation represents a major contribution of this work, allowing the computation of SNR within Matlab®. Part III presents the three readout architectures under comparison with both experimental and simulation results.

II. THE SENSING DEVICE

A. Working Principles

The sensor is based on three resistors, thermally isolated from the substrate by means of a wet-etched cavity. Such structure is shown in Fig. 1.

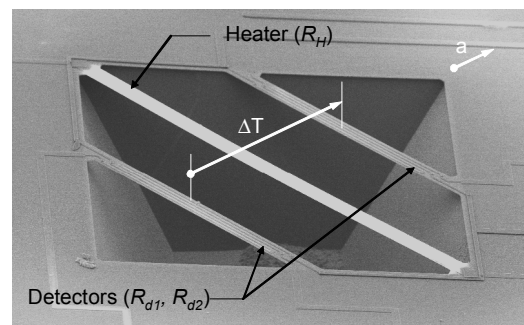


Figure 1. SEM picture of the sensing part including a central heating bridge and two lateral positive temperature coefficient detectors.

Central resistor is heated up by Joule effect. This creates a thermal gradient in the surrounding gas (air). For symmetry reasons, when no acceleration is applied, the two lateral detectors measure the same temperature. When acceleration is applied perpendicular to the bridges length, convective effects deform the temperature gradient, and a temperature difference can be measured between the two detectors using a simple conditioning circuit such as a Wheatstone bridge.

B. Modeling

An extended behavioral modeling of the convective accelerometer has been previously detailed [3]. In order to study the performance of various conditioning circuitry with an assumption of a small differential signal, this model has been derived into a small-signal model that includes initial biasing conditions into a global sensitivity parameter K_{MEMS} . This model is shown in Fig. 2. It includes the thermal time constants (τ and τ_D), the transfer function of the Wheatstone bridge (S_{Wheat}) and the noise sources in the two detectors. It also features an amplifier stage that actually exists in our silicon prototype and which is implemented in the model in order to compare simulation results with experimental data.

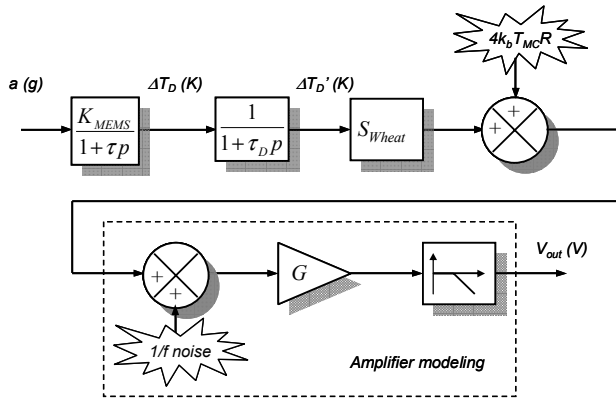


Figure 2. Small signal model of the complete sensor

C. Prototype features

The considered sensing part (see fig.1) is composed of a $500 \times 500 \mu\text{m}$ silicon bulk-etched square cavity and three suspended bridges which have a high equivalent thermal resistance $R_{th} = 15200 \text{K/W}$. The sensor features a bandwidth of 16Hz and a sensitivity of $69 \mu\text{V/g}$ using 21mW as heating power. It implements a resistive Wheatstone bridge with two resistive thermal detectors ($R_0 = 50 \text{k}\Omega$) and a low Johnson noise floor of $451 \mu\text{g}/\sqrt{\text{Hz}}$. It gives an intrinsic resolution of about 2mg (before amplification).

An on-chip, general purpose amplifier was integrated as readout interface, with a significant 1/f noise. The noise spectrum at the output of the CMOS sensor die exhibits a corner frequency of about 2 kHz. The Matlab® model of the sensor chip was calibrated using a noise simulation performed in the microelectronic design environment (Cadence®).

III. CONDITIONING CIRCUITS

The three different architectures are evaluated using spectral analyses. Each one is implemented using a sensor test-vehicle and discrete electronics, in order to verify simulation results validity.

A. Simple Amplification

An external amplifier is added to the sensor chip to raise its sensitivity to 1V/g. Noise performance of this solution depends on the first amplifier stage. Here it is a standard CMOS instrumentation amplifier based of non-optimized operational amplifiers from the foundry library.

Obtained resolutions are 31.6mg with Cadence and 30.2mg with Matlab, while The sensitive element features a 2mg intrinsic resolution on the same 1-20Hz bandwidth. A 42.7mg resolution was measured on the physical chip, which is close to the simulation results. Moreover, the amplifier offset and its variations in time make this architecture impractical, due to the very low signal level.

B. Chopper Stabilized Amplifier

In order to remove the low-frequency parasitic effects, a modulation scheme was developed. Signal is first amplitude-modulated to be amplified above the noise corner frequency, and then reconstructed using a synchronous demodulator. A similar architecture was studied in [4].

However, the intrinsic noise floor of the sensor can't be reached since this architecture folds high frequency white noise components over in the signal spectrum. According to previous work, the obtained resolution should be about 1.5 times the resolution of the sensing part ($675 \mu\text{g}/\sqrt{\text{Hz}}$). In our case, simulations under Matlab give a $1.07 \text{mg}/\sqrt{\text{Hz}}$ noise floor while characterization result is $1.55 \text{mg}/\sqrt{\text{Hz}}$. Fig.3 shows the obtained output signal spectra for both the simple amplifier (black) and the modulation scheme (gray) with an input signal of 1g (rms) at 10Hz. It clearly shows that modulation avoids 1/f noise limitations and then improves the resolution.

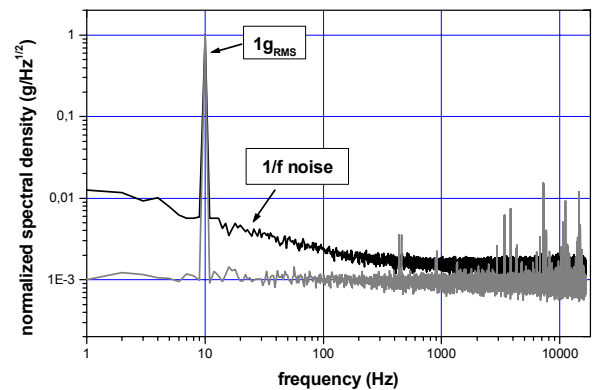


Figure 3. Simulated output spectra of the sensor, for the chopper stabilized amplifier (shaded) and for the simple amplifier (black).

C. Thermal Sigma-Delta modulator

A closed-loop architecture was finally developed using the self-heating of the detectors (under biasing) as a regulation opportunity. Acceleration-induced temperature difference is compensated by differential joule dissipation, using a differential biasing of the Wheatstone bridge. This scheme requires a time scheduling of reading and feedback phases.

The power dissipated in a bridge under normal biasing is:

$$P_0 = Vdd^2 \left(\frac{R_D}{(R_D + R_{ref})^2} \right) = 125 \mu W$$

With $Vdd = 5V$, and the equivalent power of the full-scale acceleration-induced temperature difference is:

$$\frac{2g K_{MEMS}}{R_{TH}} = 8.947 \mu W$$

A pulsed feedback scheme [5] was chosen, thus creating a first order thermal sigma-delta modulator as shown in Fig. 6. Similar architectures were developed in the field of anemometers [6] with separated sensing and feedback elements.

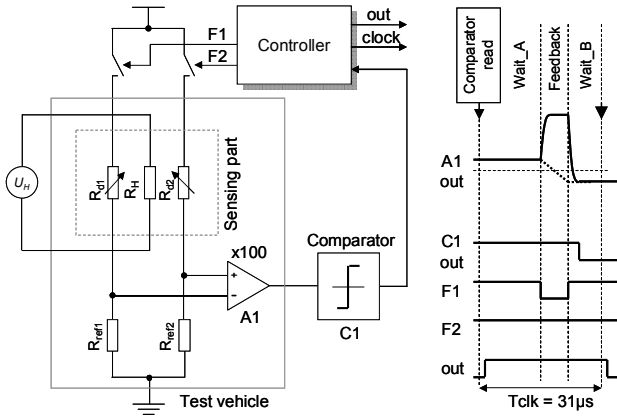


Figure 4. Thermal sigma-delta modulator principle, with a direct-digital output.

Two switches control the biasing of the Wheatstone bridge branches. The regulation is obtained by opening (off) the switch of the “hot” detector while leaving the switch of the “cold” detector closed (on). The differential biasing power between the two detectors is then P_0 .

Timing diagram is depicted in Fig. 6. for a clock cycle $Tclk$. The duty cycle ratio $\alpha = T_{Feedback}/Tclk$ allows to adjust the compensation power ($P_{Comp} = \alpha \cdot P_0$) to obtain the desired sensitivity and full-scale range. The first phase WAIT_A can be sized to control α . Then the feedback pulse comes as a compensation of the thermal mismatch. Finally, the WAIT_B phase is inserted before the reading period, to avoid parasitic transient signals from the amplifier A1.

Fig. 5. represents the small-signal equivalent model of the modulator. The sensor model was modified to compute acceleration transduction as a differential heat exchange ΔP_D instead of the temperature difference ΔT_D :

$$\Delta P_D = \frac{K_{MEMS}}{R_{th}} \frac{a}{1 + \tau p}$$

where R_{th} is the thermal resistance of a suspended bridge.

In this first-order thermal sigma-delta modulator, the loop filter is the electro-thermal response of the suspended bridges. This first order low-pass filter acts as an integrator above its cutoff frequency (48Hz) and has a static gain of $R_{th} = 15200K/W$.

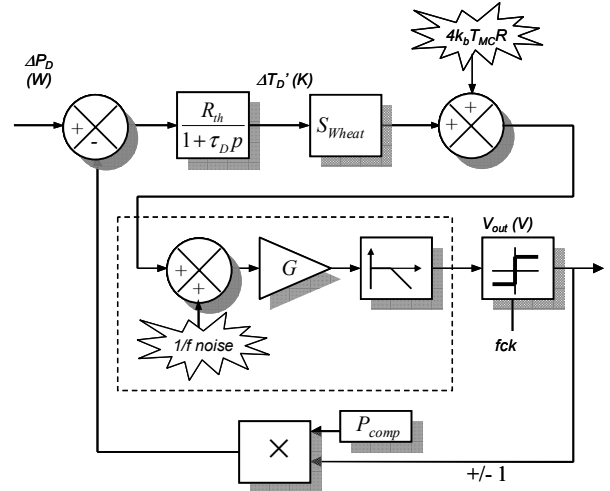


Figure 5. Thermal sigma-delta modulator signal model

The study of the modulator is based on spectral analyses of the output bitstream. With a 32768Hz clock (2^{15}), we can see in Fig. 7. the effect of the 1/f noise of the on-chip amplifier on the signal-to-noise ratio in the signal bandwidth. Actually, this architecture suffers from the same problems as the simple amplifier, due to the presence of the instrumentation amplifier.

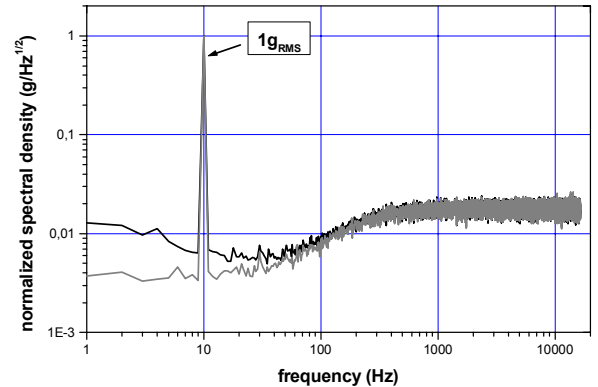


Figure 6. Simulated output spectrum of the thermal sigma-delta modulator, with (black) and without (shaded) Ficker noise.

The calculated resolution is 34.1mg, slightly worse than the simple amplifier, since there's a little quantization noise contribution in the upper part of the 1-20Hz signal band.

The same simulation without flicker noise gives a 16.9mg resolution, which is limited by the quantization noise. Such improvement can be achieved using a correlated double sampling (CDS) technique, similar in practice to the chopper stabilized amplifier.

This modulator was studied experimentally using $T_{clk} = 31\mu s$. Taking $T_{feedback} = 1\mu s$ gives a sensitivity of 25% of the full scale per g (i.e. the average voltage of the 0-5V bitstream is 1.25V/g. This corresponds to $P_{Comp} = 4\mu W$, close to the 8.947 μW calculated power.

The spectral analysis of the bitstream processed using a digital oscilloscope (see Fig. 7) is very close to that predicted by the simulation model. The resolution computed from this spectrum, 23.7mg, is close to the 34mg obtained from the simulation.

Fig. 8 shows the resolution of the modulator architecture versus its clock frequency. We see that it reaches a limit above 16kHz, due to the flicker noise of the integrated amplifier. If we assume an ideal first amplification stage (i.e. without flicker noise), the resolution at high clock rates above 1MHz is still limited by the quantization noise. A higher order modulator, characterized by a more efficient quantization noise shaping, would be more adequate, since it would require lower, affordable clock frequencies.

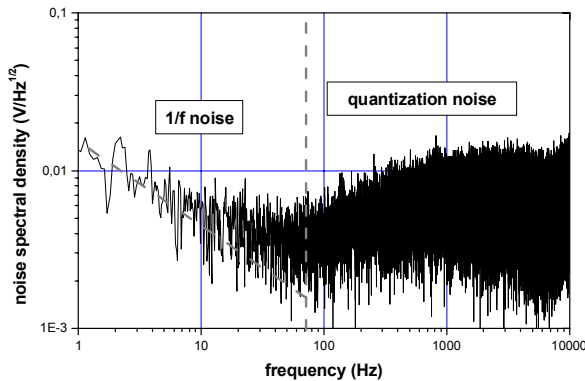


Figure 7. Bitstream spectrum of the experimental modulator

IV – CONCLUSIONS

Three different conditioning and readout architectures are studied as conditioning solutions for a CMOS convective accelerometer. The study is based on behavioral simulation under Matlab® and experimental validations.

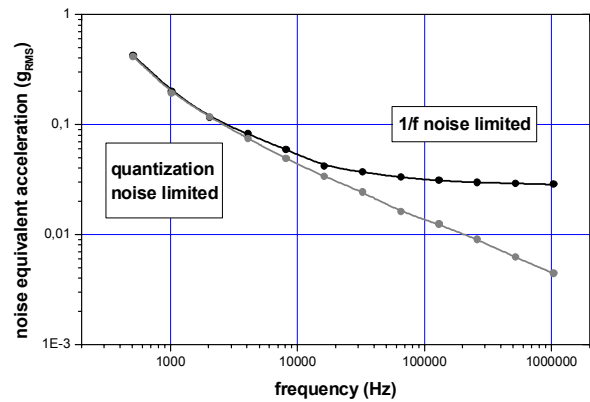


Figure 8. Simulated resolution of the modulator versus clock frequency with (black) and without (shaded) Flicker noise.

It is shown that a standard CMOS instrumentation amplifier, exhibiting strong 1/f noise and offset, is not appropriate to achieve a good sensitivity. An improvement technique is then proposed, based on a modulation scheme to remove the low-frequency noise. Resolutions very close to the intrinsic sensor performance are then reached.

Finally, a first order thermal sigma-delta modulator principle is investigated. It allows a dynamic full-scale range adjustment and a direct-digital output. This feedback architecture suffers from the integrated amplifier imperfections in the same way as the simple amplifier architecture. Finally, we show that a first order modulator architecture without flicker noise limitations would require very high clock rates to reach the sensors performance; a higher order modulator would therefore be a good alternative.

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