# Academic Network for Microelectronic Test Education

Franc Novak, Anton Biasizzo, Yves Bertrand, Marie-Lise Flottes, Luz Balado, Joan Figueras, Stefano Di Carlo, Paolo Ernesto Prinetto, Nicoleta Pricoli, Hans-Joachim Wunderlich, et al.

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F. NOVAK, A. BIASIZZO
*Jozef Stefan Institute, Jamova 39, 1000 Ljubljana, Slovenia. E mail: franc.novak@ijs.si*

YVES BERTRAND, MARIE-LISE FLOTTES
*Centre de Ressources de Test du CNFM (CRTC), and Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM), University of Montpellier,161 rue Ada, 34392 Montpellier Cedex 5, France*

L. BALADO, J. FIGUERAS
*Electronic Engineering Department, Technical University of Catalunya, Diagonal, 647, P9, 08028 Barcelona, Spain*

S. DI CARLO, P. PRINETTO
*Politecnico di Torino, Dipartimento di Automatica e Informatica,Corso Duca degli Abruzzi, 24, I-10129 Torino, Italy*

N. PRICOPI, H-J. WUNDERLICH
*Institut für Technische Informatik, Pfaffenwaldring 47, Universität Stuttgart,D-70569 Stuttgart, Germany*

J-P. VAN DER HAYDEN
*Agilent Technologies France, 1, rue Galvani, 91745 Massy Cedex, France*

*This paper is an overview of the activities performed in the framework of the European IST project EuNICE-Test (**Eu**ropean **N**etwork for **I**nitial and **C**ontinuing **E**ducation in VLSI/SOC **Test**ing) using remote automatic test equipment (ATE)), addressing the shortage of skills in the microelectronics industry in the field of electronic testing. The project was based on the experience of the common test resource centre (CRTC) for French universities. In the framework of the EuNICE-Test project, the existing network expanded to 4 new academic centres: Universitat Politècnica de Catalunya, Spain, Politecnico di Torino, Italy, University of Stuttgart, Germany and Jozef Stefan Institute Ljubljana, Slovenia. Assessments of the results achieved are presented as well as course topics and possible future extensions.*

**Keywords:** microelectronic circuit test; remote on-line test; digital test; mixed-signal test; memory test, automatic test equipment; test education.

## INTRODUCTION

INCREASING COMPLEXITY of VLSI circuits makes the testing problem more and more difficult. Test costs are rapidly rising, in some cases they account for almost 40% of the total cost. These costs are expected to continue to increase. According to the estimate of the Semiconductor Industry Association [1] stated in 1999 and confirmed in the 2003 edition, we may expect that by 2014, the costs of testing a transistor will exceed the costs of its manufacturing. The set-up costs for each individual unit-under-test (UUT) including development of test program and the design and construction of the interface between the UUT and test system represent one of the major recurring costs of automatic testing [2]. Beside conforming to design-for-test principles and introducing standardised test solutions in the products, highly qualified test engineering staff is imperative to shorten test programming time and consequently keep the overall test costs within reasonable limits.

In recent years, however, the microelectronic industry has faced a shortage of microelectronics engineers having sufficient skills in test development. A part of the problem lies in the fact that university-trained engineers receive very little or even no exposure to the subject during university studies [3, 4]. The situation calls for combined efforts involving industry and universities to define the initial and continuing educational contexts in the area of testing, and support it with hierarchically structured knowledge acquisition ranging from introductory courses to in-depth test case studies on target industrial applications. In Europe, the EuNICE-Test project [5] was launched in 2001 with the goal to build an academic network for test engineering education using remote test facilities (Agilent 83K tester

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located at CRTC in Montpellier). As reported in [6], the project has fulfilled the objectives by establishing five centres of competence that are able to deliver training courses in the field of test engineering using a high-performing industrial ATE. This paper summarises the main activities of the project and gives some details on the performed courses and the lessons learned, which might improve future training.

## EuNICE-Test MISSION

The EuNICE-Test project aims at educating microelectronics students in IC testing through the implementation of dedicated training courses on high-performance ATEs. This is done by allowing the academic and industrial partners of the consortium to remotely access the CRTC hosted by LIRMM (Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, France). CRTC test tools include up-to-date/high-tech testers (e.g. Agilent 83000 F330t ATE for testing digital and mixed-signal integrated circuits) that are fully representative of real industrial testers as used on production test-floors.

EuNICE-Test, a two-year European IST project (completed in September 2003), is mainly based on the French CRTC experience. CRTC is a common test resource centre created in early 1998. Equipped by Agilent Technologies with Agilent 83000−F330t VLSI tester, it allows microelectronics students and engineers from different French academic centres to get familiar with characterisation/production tests. The electrical test of a given device can be executed remotely from individual academic sites, with technical assistance of test engineering staff at the tester site in Montpellier. In the frame of EuNICE-Test project coordinated by CRTC, the network has expanded in 2001 to a European level, including four new academic partners: Universitat Politècnica de Catalunya, Barcelona (UPC), Politecnico di Torino (Polito), University Stuttgart (UST) and Jozef Stefan Institute Ljubljana (JSI). Agilent Technologies is the key industrial partner providing up-to-date equipment and specific education on clearly identified hot test topics (digital, mixed-signal and memory test).

Fifty percent of the project costs were covered by the EC. The costs included the equipment in remote centres, training of trainers and performing the courses in the first two years. The remote centres acquired free Agilent Software Evaluation License for the Agilent SmarTest software. This license allows an unlimited number of concurrent users. Since the software is available only for a Hewlett-Packard platform an HP Unix workstation/ server with HP-UX operating system is required in each remote centre.

## PERFORMED ACTIVITIES

The trainers of each academic partner first attended digital test courses on the Agilent 83K tester of CRTC in Montpellier. Next, these trainers gave the same training course to their students, simultaneously in each centre in Stuttgart, Torino, Barcelona and Ljubljana. Digital test course implementation is shown in Table 1.

Project partners then attended specialised test training courses: memory test (UST, Polito) and mixed-signal test (UPC, JSI), and then organised a specialised training of their students.

Teaching staff in academic centres includes professors and their assistants, teaching courses in design automation. Research institutes and laboratories employed researchers with similar experience. The teams have been involved in electronic tests for years and are active members of IEEE Test Technology Technical Council (TTTC).

Efficient performance of test courses required extensive preparatory work:

- preparation of an introductory course in which the main issues of electronic tests necessary for the understanding of the subsequent courses are reviewed;
- preparation of course materials and laboratory exercises;
- distribution of course materials at least one week before the course for the students to be prepared for exercises;

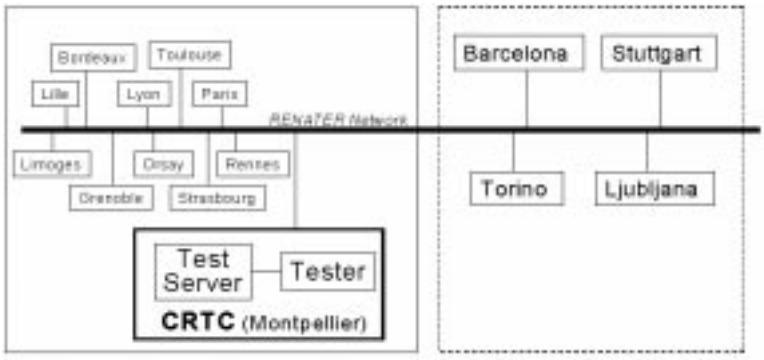


Fig. 1. Network for test education.

Table 1. Digital test course implementation in academic centres

| Centre | # Students | # Groups | # Students per group | # Days | # Hours Per student (Lecture + Labs) | # Trainers |
|---|---|---|---|---|---|---|
| UPC | 10 | 5 | 2 | 6 | 18 + 24 | 3 |
| POLITO | 25 | 6 | 4 (or 5) | 16 | 22 + 14 | 2 |
| JSI | 21 | 2 × 5 | 2 (or 3) | 6 | 6 + 9 | 2 |
| UST | 13 | 6 | 2 (or 1) | 10 | 20 + 20 | 2 |
| Total | 69 | | | | | 9 |
| LIRMM | 20 | 10 | 2 | 6 | 18 + 24 | 3 |
| France | 160 | | | | | 24 |

- preparation of course time schedule including reservation of Agilent 83000 tester (preferably one month in advance to assure the availability of the tester on the required date);
- installation of Agilent test software and establishment of the communication between the host computer and the remote system (as described in the following section).

After the official project finished in 2003, activities in test engineering education in the centres continued. In January 2004, for instance, JSI performed a digital test course for a group of postgraduate students of the University of Ljubljana and a mixed-signal test course was performed in April/May 2004. This paper aims to describe to readers our experience and lessons learned. There follows a description of the courses provided and comments on them. The mixed-signal test course performed at JSI and memory test course performed at University of Stuttgart are more detailed since they refer to specific features which are normally not included in the general electronic test courses during university studies.

## COURSE DESCRIPTION

*Basic digital test course*

The course requires for the attendees to have some basic knowledge in the area of electronic tests. The course starts with the Agilent 83000 tester hardware and software overview.

The major components of the Agilent 83000 tester (Fig. 2) are introduced: mainframe, test head and workstation. The mainframe contains memory, timing generator and power supply modules. The test head contains pin electronics and parametric measurement units. Pin electronics consists of several input/output (pin connection) test channels (i.e., driver/receiver pairs), timing generator and waveform composer used to build the signals (i.e., test stimuli) to the DUT (Device Under Test). The workstation serves as controller for the test system.

The next step in the course summarizes Agilent HP83000 software. The structure of test data is discussed, together with the data manager software used for test data manipulation. Basic steps in test

Fig. 2. Agilent 83000 F330t tester: test head (left), mainframe (centre) and workstation (right).

preparation are outlined: DUT pin configuration, voltage and current levels, timing and organisation of test vectors. The target DUT is introduced (in our case the 74ACT299, an 8-bit universal shift/storage register with tristate outputs) and the above items are determined. Functional test is defined. In the remote access operation, the user at a remote centre (e.g. Ljubljana) establishes connection with the workstation, transfers test data to the workstation and runs a functional test of the DUT inserted in the test head of Agilent HP83000. The AC and DC behaviour of the device is tested and results are analysed and discussed.

The Agilent 83000 test software can be executed with active connection to the tester (on-line) and by stand-alone (off-line) mode. The ability to run the software off-line enables test preparation at remote locations without the actual connection to the tester. The software runs on the HP-UX operating system and several users can simultaneously develop test applications (several program instances). However, only one instance of the software can be connected to the tester. Off-line application instances can be used to simultaneously prepare tests for different projects. In addition, the remote execution of the software is also possible. The software is graphic application built on top of the X Window System and additional steps are required to enable the communication between the host computer and the remote system. In our case we used a *SSH* (**S**ecure **SH**ell) which provides a secure connection as well as the tunnelling of X applications.

*Logistic concerns*

The Agilent test software is a relatively lightweight application and an entry level HP workstation can be used for up to a few dozens of simultaneous users as long as it has sufficient memory (64MB per user). On the other hand, the remote execution proved to be more time consuming. The main reasons are:

- The bandwidth of the Internet communication is much lower than the bandwidth of the intranet and is also time dependant.
- Tunnelling of the X Window System application over SSH incorporates the encryption of the data stream which in turn reduces the throughput of the communication channel.

To circumvent this drawback the best strategy is to:

- locally develop complete test procedures, which are saved in the data files;
- compress the data files and transfer them to the remote location;
- connect to the remote tester site, uncompress the test procedure data files;
- execute the test procedure.

The above steps were simplified by automating the compression, transfer and decompression of test data files with simple scripts and shell functions. Student groups (typically 2 students per group) developed the test procedures locally and when the tests were fully prepared they transferred the data and entered the queue for remote execution.

*Mixed-signal test course*

The course starts with general lectures (1–3 from the basic digital test course) followed by:

1. *Fundamentals of analogue testing*. A brief summary of the sampling theory is given with special consideration of the Nyquist criterion, aliasing and under-sampling. Averaging as a method of noise reduction is described. Later on coherent sampling is introduced. The frequency domain analysis is presented followed by a short description of the Discrete Fourier Transform. Next, Fast Fourier Transform is introduced and the necessary conditions for its calculation. The leakage effect as a result of improper sampling is demonstrated. Windowing technique as one possible method for reducing leakage is mentioned.
2. *The analogue testing to determine the static and dynamic performance parameters of the circuit.* Static performance parameters specify the static transfer characteristics of the circuit. Basic parameters are: differential non-linearity (DNL), integral non-linearity (INL), gain error, offset error and gain mismatch. Dynamic performance parameters are also called distortion parameters. They are: total harmonic distortion (THD), signal-to-noise plus distortion (SND), signal-to-noise ratio (SNR), spurious free dynamic range (SFDR)
3. *Description of analogue instruments* provided by the Agilent HP83000 tester for the purpose of mixed-signal testing (in this particular case) include: Smart Waveform Instrument, Smart Waveform Generator, Smart Video Sampler and Smart Capture Memory. The connection of the analogue instruments with the circuit under test and synchronisation of the instruments is also described.
4. *Introduction to the mixed-signal features of the HP83000 software.* DSP Memory Manager is used for DSP (digital signal processor) configuration which is embedded in analog instrument (1 DSP per channel). The Mixed Signal Tool Panel is used for waveform generation as well as for the analysis of the captured waveforms. Analogue test functions perform the measurement of the circuit under test in accordance with the specifications given in the Data Sets and calculate required performance parameters. The resulting performance parameters can be visualised by the Mixed Signal Tool Panel.
5. *Description of the mixed-signal test exercise.* For the mixed-signal test exercise the digital/analogue converter (DAC) test is chosen. An AD7524 D/A converter is selected as a case study. It is an 8-bit CMOS DAC with input

latches. The measurements are performed using SVS instrument. The static performance parameter (DNL and INL) as well as dynamic performance parameters (THD, SND and SNR) are evaluated.

*Memory test course*

The goal of this course is to jump-start the young engineers to a new level of practical test expertise. Methodologies and solutions for addressing the field of memory test issues are presented and practical experiments are conducted on selected case studies using the Agilent 83000 ATE. The memory test course provided:

- understanding of basic memory device architecture;
- understanding of ATE memory test system architecture;
- methods of detecting various faults within memory devices;
- guidelines for producing quality test programs with maximum throughput.

In the following paragraphs the contents of each teaching unit are highlighted:

1. *Introduction to memory test*. In this teaching unit, the theory behind memory test is discussed. The general functional model of a memory is presented and the differences between various types of memories are clarified. Possible faults occurring in a memory device are classified (Table 2) and for each class of the memory faults some algorithms for detecting such faults are presented (Table 3).

The algorithms are extensively studied with respect to their advantages, disadvantages, fault coverage and running time. The following information accompanies the explanation of each test algorithm:

- flow chart—indicating the sequence of read/write of 0's/1's operations (for simplicity, a $4 \times 4$ memory with one cell per address was considered).
- sample code used to generate the pattern,
- graphics to illustrate the relationship between address and data,

fault coverage and pattern's execution time calculation.

2. *Introduction to the tester.* The lesson starts with a survey of the Agilent 83000's test processor per-pin architecture and of the Algorithmic Pattern Generator (APG) software. Using per-pin APG, the test patterns are generated from sequencer subroutines loaded into vector memory (instead of the individual vectors). As these routines require only a fraction of the space a set of vectors would, much larger test patterns are generated using the same vector memory. Furthermore, 'Bitmap Memory' and 'Fail Memory' tools are introduced. These tools are useful for debugging, which makes the job of analyzing test data easier and more productive.
3. *A review of timing.* In this teaching the HP83000's timing system is described together with the firmware commands for the timing setup. Typically, a memory test is performed with different frequencies. The students create the timing file that matches the physical waveforms of the DUT (in our case, the memory device IDT71V256SA, $32K \times 8$ SRAM).
4. *Scrambling and bit inversion.* Scrambling ensures that the device is tested topologically. For generating memory test patterns, the software must be aware of the relationship between the physical (topological) and logical addresses, and how the word in each address is arranged. Some memories have regions with inverse logic on their cell array (i.e. logical '0' in such regions is represented by a physical '1'). The APG can take bit inversion into account when it is described by a 'bit inversion table'.
5. *Setting up a memory test.* In this lesson a practical memory test is performed. The DUT is the low power 3.3V CMOS Fast SRAM 256K ($32K \times 8$), IDT71V256SA from Integrated Device Technology Inc. The procedure starts with the functional description of the device (Pin Configuration, Levels and Timing) using the Agilent 83000 'General Setup' window. Then, the students have to specify in a dedicated 'Memory Setup' window the details about the memory test such as the pins of the port, the way the read/write cycles work and others. The procedure continues with the test definition i.e. setting up any scrambling and/or bit inversion, the test region, test pattern, test range, labels and sub-labels, etc. The last step consists of setting up the vectors by using the 'Vector Setup' window. The device is tested using two methods: first by selecting one of the standard library patterns (March) and secondly by creating a fully-customized pattern based on one of the original library patterns (see APG-ALPAD).

Table 2. Functional memory faults

| Name | Functional fault |
|---|---|
| SAF | Stuck-at fault |
| TF | Transition fault |
| CF | Coupling fault |
| NPSF | Neighborhood pattern sensitive fault |
| AF | Address decoder fault |

Table 3. Test algorithms

| Algorithm | Faults detected |
|---|---|
| Checkerboard | Some: SAF, CF, TF, AF |
| Galpat | All: SAF, CF, TF, AF |
| March | All: SAF, AF; Some: TF, CF |
| Solid | Some: SAF, CF, TF, AF |

6. *Getting Results.* Electrical (parametric) tests and the functional (logic behaviour) tests of the DUT are performed. Each team uploads the test data (using secure shell) to the Agilent 83000 ATE's workstation, located at CRTC in Montpellier. After the on-line test, the results are downloaded and analyzed. The average time each team needed for the on-line test procedure was about 15 minutes. The electrical test sends the results of the test to the following result windows: 'Error Map', 'State List' and 'Timing Diagram'. The functional test (memory analysis test) sends the results to the 'Fail Memory' and 'Bitmap' windows. Test results are analysed in order to identify the failures of the memory device.
7. *APG-ALPAD (Algorithmic Language for Pattern Description*) is used to customize patterns, offering high-level programming capabilities. Such algorithmic descriptions are commonly used when generating tests for embedded memories. The syntax of ALPAD is very similar to C. The students programmed customized algorithms for memory test using ALPAD. For instance the students needed to create a test algorithm according to the following description, as an exercise: Write in the memory cells alternating 1's and 0's; Read the memory cells in the order: 1, 2, 3, etc.

## EFFECTS OF THE COURSES AND ACHIEVED RESULTS

Trainers worked in a multicultural environment, with students having different backgrounds, strengths and weaknesses. They tried to eliminate these differences by designing a balanced teaching approach that addresses the learning needs of all of them. The courses were taught in a manner that emphasised active and co-operative learning. The teams worked independently on well-defined tasks and learned by trial-and-error. Through non-trivial but easy to understand examples, the trainers illustrated the difficulties and pointed out traps that can make test programming a nightmare. The students showed high interest in the laboratory exercises and positively assessed the acquired experience. Quantitative assessment other than the number of the students that participated in the courses is difficult since the situations differ from country to country. In Stuttgart, for example, the total number of trained students was 27. Part of them continued with internships in companies such as IBM and Agilent Technologies. In Ljubljana, the attendees of the digital course were already employed in electronic companies in Slovenia. Discussions during the course and later individual consulting referred mainly to the specific current test problems in their companies and their possible solutions. Most of them have had some experience only on relatively simple dedicated testers.

Experience shows that the opportunity to access and run on-line a test program on a real industrial ATE highly motivates students, although most of them lack the in-depth knowledge of testing. Their interest can be further encouraged if they can visit a real production plant. University of Stuttgart (UST), for example, is located in a big industrial area. That facilitated visits to different companies owning a test sector (engineering test and/or production test) e.g. Agilent Technologies Böblingen, IBM Hulb and Robert Bosch Reutlingen. Thus, students had the opportunity to familiarise themselves with the Agilent 83000 tester as it is in reality. The experts provided both theoretical and practical demonstrations and valuable information for the students' complete training as future test engineers. At IBM Hulb engineering research laboratories, the experts presented the phases of electrical wafer test (e.g. wafer probing technology, wafer emission microscopy, etc.). Visiting Robert Bosch Reutlingen, the students were introduced to the atmosphere of the production test floor (e.g. wafer testing in clean rooms using Teradyne wafer testers).

Although far from comprehensive these courses offer a unique opportunity to experience the complexity of testing modern electronic devices. The attendees gain basic insights into individual steps in test program preparation, test execution and evaluation of test results on a modern ATE. Besides developing skills in electronic testing, the experience is also helpful to the designers to give proper care to the design-for-test issues, and to the design managers to choose a test strategy and make the right decisions in ATE investments.

## LESSONS LEARNED

The average time of accessing the Montpellier ATE is acceptable even if strongly depending on the network traffic. It is advisable to select on-line connections in the time intervals where network traffic is low. Besides, a considerable part of the lessons can be prepared using only local resources. During the reserved time slots of the remote access of the tester, tester occupation time can be minimised by properly coordinated tasks shared among the student teams.

Backgrounds on industrial test practice are not sufficiently covered in the existing courses. The present format in industrial test techniques mainly targets ATE facilities (i.e., gives the information on how to run AC/DC test functions individually or in a test flow but does not give explanation on why or when to perform a given test function). In the future, the training should be more comprehesive.

For successful mixed-signal test training, students have to be familiar with sampling theory and basics of signal processing. Both static and dynamic parameter evaluation is essential for such understanding. Recent experience indicates that

more time for theoretical lectures on the above issues should be given in future courses. For the memory training, students should have some basic knowledge of memory types (i.e., static random access memory, dynamic random access memory) and architectures.

Performed test courses may be further improved by the exchange of information, teaching materials and consultations among the established EuNICE-Test centres. Furthermore, extensions of activities in the following areas are being considered:

- *Digital testing:* development of specific lectures and labs in order to allow students to explore a large set of test-related activities such as test pattern generation, fault simulation, Design-for-Testability through engineering tests using remote ATE facilities.
- *Mixed-Signal testing:* development of case studies in ADC/DAC testing. In particular both (i) the histogram-based technique needed to derive static parameters, and (ii) the Fast Fourier Transform based technique needed to catch dynamic parameters, are planned to be taught.
- *Memory testing:* development of lectures and remote labs on the typical memory testing techniques using different repair methods like Redundancy Repair.

## 'ADDED VALUE' OF COOPERATION

Besides test courses, established contacts among the centres foster several other activities ranging from exchange of information, consulting, joint experimental work of Ph.D. theses up to bilateral research projects. For example, a Ph.D. student at Jozef Stefan Institute, Ljubljana, working on the problem of built-in self-test of field programmable logic arrays (FPGA) is collaborating with LIRMM, Montpellier, in the area of structural testing of FPGA, considering the effects of single-event upset faults extensively studied at Politecnico di Torino. Another example is a bilateral French-Slovenian project 'Design-for-test techniques based on IEEE 1149.4' with collaborating partners LIRMM and Jozef Stefan Institute.

## CONCLUSIONS

Test engineers are responsible for developing and implementing cost-effective methods of testing and troubleshooting electronic devices and systems. A test engineer defines test parameters, develops test plans, designs test fixtures, prepares and runs tests and diagnostic programs and analyses test data. In addition, test engineers provide testability advice in the design of the new products and guidance in the completion of projects to ensure that user requirements and other objectives are met. The job of a test engineer also requires the ability to adapt to heterogeneous technical environments and ATE systems. Such a profile requires skill, which can only be gained by intensive, specialised training and long-term experience.

The analysis of university programs performed in the early 90's [3] has revealed the necessity of integrating testing and testability issues into standard electrical engineering curriculum. Now, when the complexity of VLSI technology has reached the point where more than 100 million transistors are placed in a single chip and when design tools enable different complex cores including DSP, DAC, extensive memory blocks and different peripheral controllers to be placed in a single system-on-chip, additional efforts are required to meet the growing needs of the industry. New design techniques impose problems that can only be mastered by a thorough experience in both the design and test areas. The EuNICE-Test network provides extensive initial test training curriculum, thus largely contributing to test engineering education. In perspective, the network can be extended including new academic centres. The description of the performed activities shows that integration of testing theory and practice into the electrical engineering curriculum is a complex task requiring considerable efforts in setting up the test resources and training personal on one side, and broad knowledge background of students (including general electronics, sampling theory, signal processing, etc.) on the other. Even if not involved in the EuNICE-Test network the reader may find in the paper useful hints and guidelines to emulate the project or organise courses in order to improve skills in electronic testing.

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**Franc Novak** is head of the Computer Systems Department at the Jozef Stefan Institute, Ljubljana, and associate professor at the Faculty of Electrical Engineering and Computer Science, University of Maribor. His research interests are in the areas of electronic testing and diagnosis, fault-tolerant computing, and design for testability of analogue circuits. Novak has an MS (1977) and a Ph.D. (1988) in electrical engineering, both from the University of Ljubljana.

**Anton Biasizzo** is a researcher at Jozef Stefan Institute since 1991. He received the B.Sc., M.Sc., and Ph.D. degrees from the University in Ljubljana in 1991, 1995, and 1998, respectively. He contributes to European research projects in the fields of renewable energies and electronic test. His research interests include efficient algorithms for sequential diagnosis, model based diagnosis, design-for-test and built-in self-test techniques.

**Marie-Lise Flottes** received the Ph.D. degree in microelectronics in 1990 from the University of Montpellier. She is currently researcher at CNRS (French National Research Center), and in charge of the Microelectronics Department of the LIRMM Laboratory (Montpellier, France). Her research interests include various aspects of digital testing with special emphasis on design-for-test, test management at system level and test of secure designs. She has co-authored more than 100 papers and a book on systems testing. She contributed to several European research projects and managed industrial research contracts.

**Yves Bertrand** is a professor at the University of Montpellier. He works at the Microelectronics Department of LIRMM Laboratory. He is author or co-author of more than 200 papers. His research interests are design-for-test and built-in self-test for digital and mixed-signal circuits, design and test of medical implantable stimulators. In 1997, he created the CRTC (Common Test Resources Centre, for all the French academic centres) and initiated the first network for test engineering education via the internet. He is presently the dean of the Faculty of Sciences of Montpellier.

**Luz Balado** received the degree in Industrial Engineering in 1980 from the Universitat Politècnica de Catalunya (UPC) and the Doctor degree in Electronic Engineering in 1986. She is presently Associate Professor at the Electronic Engineering Department of the UPC where she teaches Electronics and Electronic Instrumentation and is involved in the Microelectronics and Test research Group. Her main research interests are design and test of digital and mixed-signal circuits and defect modeling.

**Joan Figueras** received his Industrial Engineering degree from the Universitat Politecnica de Catalunya (UPC), Barcelona, and the M.Sc. and Ph.D. degrees from the University of Michigan. Since 1983 he is a professor at the Electronics department of the UPC with research and teaching responsibilities in the area of digital systems and VLSI design and test. His research interests include new design and test techniques in low power design and high speed electronics.

**Stefano Di Carlo** received a M.Sc. in Computer Engineering in 1999 and a Ph.D. in Information Technologies, in 2004 both from Politecnico di Torino. Since 2004 he is a research assistant in the Department of Automation and Information Technology at Politecnico di Torino. His research interests include design-for-test techniques, system-on-chip testing, built-in self-test, and memory testing. He is a Golden Core Member of the IEEE Computer Society.

**Paolo Prinetto** was born in Gassino Torinese, Italy, on March 17, 1953. He received the M.S. in Electronic Engineering in 1976 from the Politecnico di Torino, Italy. Since 1990 he is full professor of Computer Engineering at the same University, and, since 1998, joint professor at the University of Illinois at Chicago. His research interests cover testing, test generation, BIST and dependability. He is a Golden Core Member of the IEEE Computer

Society and the elected chair of the IEEE Computer Society Test Technology Technical Council (TTTC) from.

**Nicoleta Pricopi** obtained in 1996 a MSc in physics of materials from the est University Timisoara, Romania. For five years she worked as a scientific researcher in physics and in the same time she started a second faculty. In 2000 she obtained a B.Sc. in Computer Engineering from the Politehnica University Timisoara, Romania. For four years (2001–2005) she was employed as scientific researcher at Universität Stuttgart, Institut für Technische Informatik.

**Hans-Joachim Wunderlich** received the Dipl.-Math. degree in mathematics from the University of Freiburg, Germany, in 1981, and the Dr. rer. nat. (Ph.D.) degree in computer science from the University of Karlsruhe in 1986. From 1996 on he is with the University of Stuttgart where he currently holds the position of a full professor and is head of the Division of Computer Architecture. He is an author and co-author of four books and more than 100 papers in the field of test, BIST, and fault tolerance.

**Jean Pierre van Der Heyden** received his Diploma of University of Technology at Lille in 1977. In 1978 he joined Hewlett Packard working in the area electronic manufacturing test. From 1993 to 1997 he was at Integrated Test Measurements company (subsidiary of Cadence) as application engineer. He is back in 1997 at Hewlett Packard as European project manager for semiconductor business. Since 1999 he is also subcontracting program manager for the semiconductor test business at Agilent Technologies.