Analyzing the Logic Behavior of Digital CMOS Circuits in Presence of Simultaneous Switching Noise

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Abstract

This paper analyzes the logic errors in digital circuits due to the presence of Simultaneous Switching Noise (SSN). It is demonstrated that 2 conditions must be fulfilled in order to guarantee the correct logic behaviour of a digital circuits. The first condition called 'Minimum Switch Condition' is proved to be fulfilled whatever the amount of SSN in the power and ground lines. The second condition called 'Signal Coherence Condition' is proved to be fulfilled within power coherent logic blocks. However the interface between non-coherent logic blocks may originate logic dysfunction.

1. Introduction

As technology scales into the nanometric range, noise is becoming a very important issue. Power and ground bounce in the power and ground distribution network is one of the main contributors to the overall circuit noise. Power and ground bounce, also called Simultaneous Switching Noise (SSN), usually designates some kind of fluctuations in the power and ground voltages due to currents flowing through inductances and capacitances of the power and ground network, bonding pads and package pins. Figure 1 gives a representation of these parasitic components for a typical package pins [1,2,3,4]. In this example, two parasitic cells have to be used, each includes a capacitance (C) in parallel with a resistance (R) and an inductance (I).

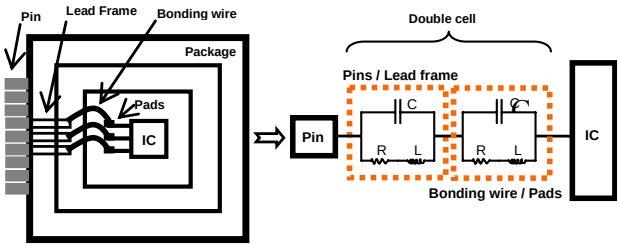


Figure 1: The double parasitic cell

It was first considered that SSN was originated by the simultaneous switching of the IO buffer pads because of their very large size and associated large current. For this reason, the first studies have focused on SSN due to IO buffers. In this context, specific design techniques have been proposed and developed that allow to significantly reduce the amount of power and ground bounce [5,6].

However, modern high speed circuits contain a large number of gates that may switch simultaneously with a very high clock rate. Indeed, when a so large number of logic cells are simultaneously turned ON or OFF, very large and fast variations of current in the inductances may create fluctuations in the power and ground distribution lines. For these reasons, SSN in internal circuitry in modern chip has to be considered [7]. To illustrate this situation the C432 benchmark circuit is simulated electrically using SPICE and using a 130nm technology with 1.2 Volt of power voltage. Figure 2 gives the equivalent simulated model where the double parasitic cell of figure 1 has been used in the power connection and another one in the ground connection.

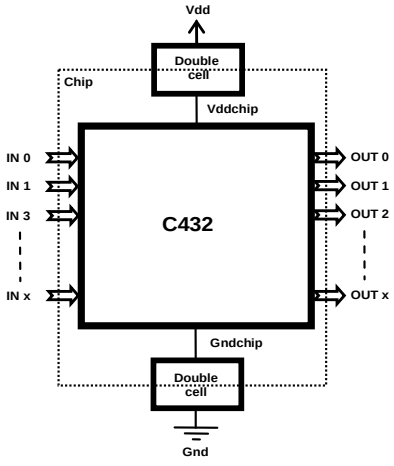


Figure 2: Simulation model of the C432

In this paper, the constant power and ground voltage outside the chip are respectively called VDD and GND, while the fluctuating power and ground voltage inside the chip are respectively called Vddchip and Gndchip. In figure 3, the simulation shows a very important SSN where we can observe fluctuations of Vddchip from 0.95V to 1.4V and fluctuations of Gndchip from -0.25V to 0.25V 5remember that correct value of Vdd is 1.2V and GND is 0V).

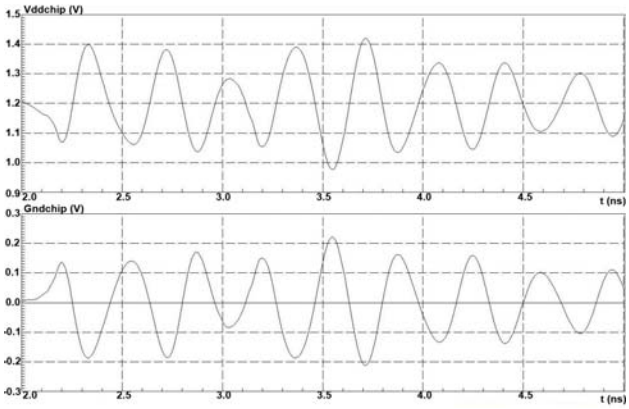


Figure 3: Simulated SSN of the C432

It is well known that SSN impacts the logic behavior of digital circuit as well as the timing behavior. This paper focuses on the logic behavior. The main contribution of this paper is an accurate analysis of the impact of SSN on the logic behavior of digital circuit. In section 2, previous works are revisited pointing out the main contributions and limitations. In section 3, it is demonstrated that 2 conditions have to be fulfilled for a digital circuit to perform its correct function. Section 4 analysis the first condition and section 5 the second conditions. Finally section 6 concludes the paper.

2. Previous works

Since ground bounce is becoming an important limitation in modern circuits, many researchers have focused on the problem of modeling the SSN, proposing design technique to reduce the SSN, or defining test technique to detect excessive SSN.

Through electrical simulations, earlier works are dedicated to the analysis and modeling of SSN created by IO buffers [1,2,3,4]. The possibility of reducing the level of noise by different design techniques such as decoupling capacitances is studied in some papers [3,5,6].

A few papers propose to model the substrate noise and the impact on analog circuitry [8,9].

Finally, several papers are more dedicated to test problems [7,10,11,13]. In these works, authors try to analyze the impact of ground bounce on the logic and timing behavior of digital circuit. The main motivation is first to understand how a digital circuit may exhibit a logic error or a timing error due to SSN. The second motivation is to generate test vectors to detect a possible error. In the test context, the test generation strategy is to maximize the amount of SSN to increase the probability of detection. Another motivation is to propose integrated sensor to monitor the Vddchip and Gndchip line to detect excessive noise [14].

Concerning the possibility of having logic errors, we observe that the main criterion used in the literature is the modification of the power voltage or ground voltage. A logic error may appear if:

- the power voltage is lower than a given limit,
- the ground voltage is higher than a given limit.

This criteria is discussed in the remaining of this paper.

3. Operating conditions of logic circuits

As explained in the previous sections, the current flowing through the parasitic inductances and capacitances of the power and ground lines creates fluctuations of the power and ground voltages. A straightforward consequence of these fluctuations is fluctuations on every node of the circuit including the internal logic nodes but also the input and output nodes.

Indeed, the fluctuations in the Vddchip (resp. Gndchip) node are directly reproduced on the output of every logic gates with a ON network of p-transistors (resp. n-transistors). As an example in figure 4, we plot one of the output nodes of the C432 benchmark circuit from simulation of figure 3, i.e. when the Vddchip and ground-chip are fluctuating. It is clear in figure 4 that the logic behavior is strongly impacted to the point where logic level '1' and '0' can not be discriminated. It seems absolutely impossible to recognize the different logic levels and so we could conclude that the circuit exhibits a very strong dysfunction.

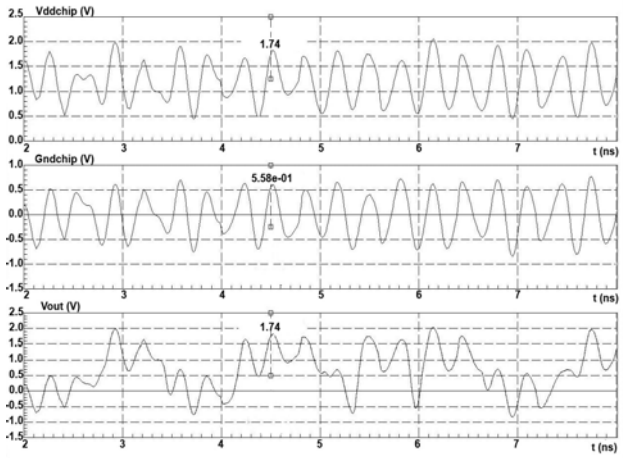


Figure 4: Simulated SSN in logic nodes

Despite of this extremely noisy behavior, we propose to try to analyze the behavior of this circuit. For this purpose, we first consider a noise free circuit with constant power and ground voltages, i.e. Vdd=Constant=1.2V and Gnd=Constant=0V. For the sake of simplicity, the demonstration is given for a simple CMOS inverter. But extension of the analysis to other logic gates is straightforward.

So, we consider a very classical CMOS inverter made of a p-transistor and a n-transistor respectively connected to Vdd=1.2V and Gnd=0V as represented in figure 5.a. In case of a noise free power and ground line, the logic

behavior of the inverter is given by its Transfert Function (TF) represented in figure 5.a. From the transfert function, we write:

a) 0<Vin<Vth => Vin is recognized as a logic '0'and Vout=Vdd=1.2V
b) Vth<Vin<Vdd => Vin is recognized as a logic '1' and Vout=Gnd=0V

where Vth is usually called the logic threshold and its value is around Vdd/2, i.e. half of the swing (Sw):

$$Vth \approx Sw/2 \quad \text{with} \quad Sw=Vdd-Gnd \qquad (1)$$

We consider now the same inverter but with noisy power and ground line. In this case, the inverter is no longer biased with constant Vdd and Gnd. Indeed, these voltages are fluctuating over time and so they are noted Vddchip(t) and Gndchip(t). In the general case, it can be observed in figure 3 that Vddchip(t) and Gndchip(t) are not in phase, and so they can have any kind of values. Assuming any value for Vddchip(t) and Gndchip(t) means that the swing is also fluctuating over time:

$$Sw(t) = Vddchip(t) - Gndchip(t) \qquad (2)$$

Previous works on low-voltage testing [17] have demonstrated that logic gates are able to perform their logic function if the swing is higher than a limit approximately given by the sum of the p- and n-transistor voltage thresholds Vtn and Vtp. This property allows us to give the first condition for a circuit to operate correctly under SSN.

***Minimum Swing Condition*: For a digital circuit made of standard CMOS gates and operating with SSN, the swing must be higher than the sum of the n- and p-transitor voltage threshold:**

$$\mathbf{Sw(t) > Vtn + |Vtp|} \qquad \mathbf{(3)}$$

At this point, it is interesting to note that several papers have proposed DFT techniques for SSN based on the implementation of sensors into the chip. The objective of the sensor is to deliver a signal when a high amount of SSN is detected internally into the chip. Sensors have been proposed that detect when the Vddchip become smaller than a limit voltage. From the above analysis, it clearly appears that the critical parameter is the swing and it is useless to monitor only the power line.

Assuming now that the first condition on minimum swing is fulfilled, we focus on the logic behavior of the noisy inverter. The logic behavior of the inverter is not constant in time, and so we introduce the concept of 'Instantaneous Transfer Function'. Considering for example time to=4.5ns in figure 3 where Vddchip(t0)=1.74V and Gndchip(t0)=0.55V, the ITF at time t0 of the inverter is given in figure 5.b. From the ITF of figure 5.b, we can propose the following general property:

a) Gndchip(t)<Vin(t)<Vth(t) => Vin(t) is recognized as a logic '0' and Vout(t)=Vddchip(t)
b) Vth(t)<Vin(t)<Vddchip(t) => Vin(t) is recognized as a logic '1' and Vout(t)=Gndchip(t)

where we define Vth(t) as the instantaneous logic threshold. Its value is around half of the instantaneous swing (Sw):

$$Vth(t) \approx Sw(t)/2 \qquad (4)$$

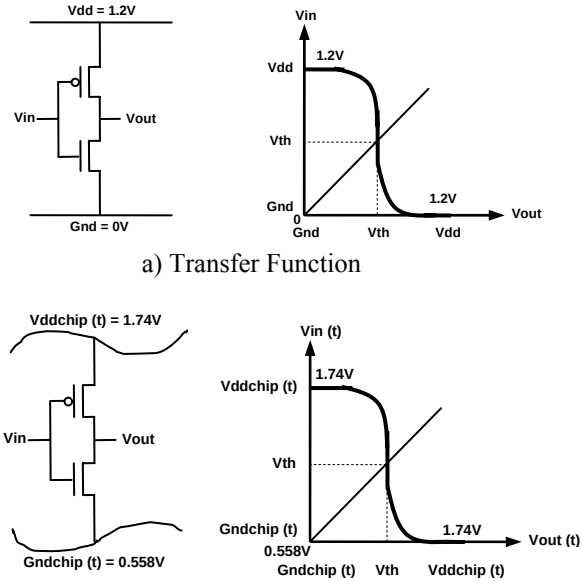


Figure 5: TF and ITF

We observe that there is no fundamental difference between a 'normal' TF in figure 5.a and an ITF in figure 5.b. Basically, a low input voltage gives a high input voltage and vice-versa.

In fact, the very critical point is the exact definition of what we call a low input versus a high input. The input voltage Vin(t) is compared to the logic threshold voltage Vth(t) which, in turn, depends on the power voltage Vddchip and the ground voltage Gndchip. The input voltage has to be in the range from Gndchip to Vddchip. In other words, we will say that the range of the input signal has to be coherent with the power and ground voltages.

This property allows us to give the second condition for a correct behaviour of a logic gate under SSN.

***Signal Coherence Condition*: A standard CMOS gate operating under SSN will perform its correct function if the input signal range is coherent with the power and ground voltage.**

$$\mathbf{Vin(t) \in \{Gndchip(t), Vddchip(t)\}} \qquad \mathbf{(5)}$$

It is obvious that an ideal CMOS circuit without SSN always fulfills the 2 operating conditions. The problem now is to analyze the behavior of the C432 in figure 3 and to determine if the 2 operating conditions are fulfilled or not inducing a complete loss of the functionality.

4. Minimum Swing Condition

The first condition expresses that a minimum swing is required to guarantee a correct bias of the logic gates. We can imagine that below some limits, the MOS transistors remain permanently OFF and cannot be turned ON, implying a loss of the functionality.

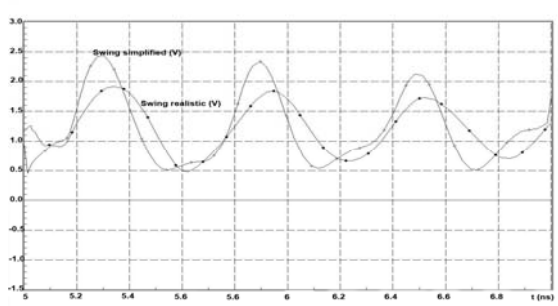
An analysis of the swing requires an accurate model of the Vddchip and Gndchip oscillations trying to determine the voltage minima and maxima. As already mentioned in section 2, many papers have been published on the matter of modeling the bouncing currents and voltages. Due to the complexity of the considered phenomena, a simplified model is usually considered.

A very common simplification consists in considering a simple inverter whose input signal is a clean, noise-free transition from 0V to Vdd [4,15,16]. In this simplified model, the authors consider that the n-transistor is completely ON and fully conducting. As a consequence, the bouncing current is quite important and the amplitude of the power and ground voltage oscillation is also important.

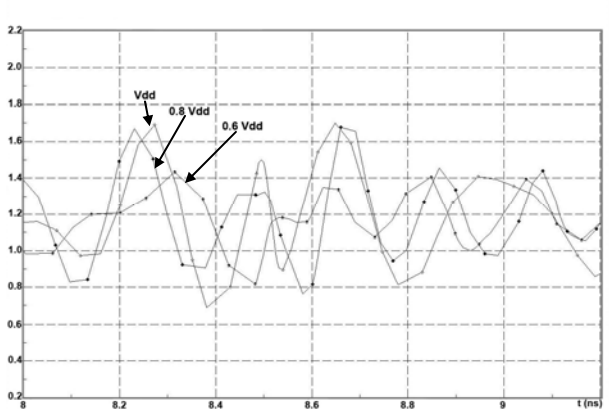
In a realistic situation, the input signal follows the power or ground oscillations implying that the amplitude of the input transition may be small. The bouncing current is modulated by the bouncing input voltage. In other words, the system creates a sort of feedback:

- the input step creates a bouncing current,
- the bouncing current creates a bouncing swing
- the bouncing swing creates a bouncing input
- the bouncing input modifies the bouncing current…

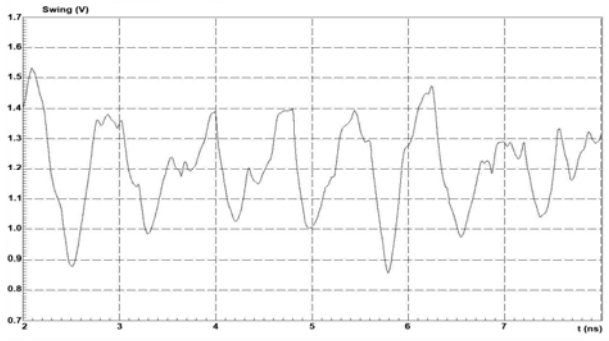
In figure 6.a, this situation is illustrated and we observe that the realistic bouncing swing with feedback is much smaller than the simplified bouncing swing without feedback. In fact, the feedback from the power and ground lines on the input signal is negative decreasing the amplitude of the SSN as we illustrate below.



a) Realistic vs simplified swing



b) Swing for different step amplitude



c) C432 overall swing

Figure 6: Minimum swing simulation

The negative feedback can be illustrated with the following simulations. In figure 6.b, we plot different swings for different amplitudes of the input transition. For smaller amplitude of the input transition, we obtain a larger swing. This demonstrates that the swing cannot decrease too much because of the reverse effect on the input of the inverter.

The previous demonstration can be extended to the whole circuit. And we plot in figure 6.c, the swing Sw(t) of the C432 benchmark circuit of figure 2 where the swing is never below 0.85V. Consequently, whatever the amount of SSN, the swing is higher than the Vtn+ $\left|$ Vtp $\right|$ limit. This leads to the following observation.

***Minimum Swing Observation*: Due to the negative feedback of the gate input signal, the swing of a circuit has never been observed lower than Vtn+ $\left|$ Vtp $\right|$ whatever the input vector and the amount of switching gates.**

At this point, it is interesting to note that several papers have proposed DFT techniques for SSN based on the implementation of sensors into the chip. The objective of the sensor is to deliver a signal when the swing becomes smaller than a predefined limit. From the above analysis, it clearly appears that the critical parameter is not the swing and it is useless to monitor it.

5. Signal Coherence Condition

The second condition expresses that the input signal of any gate must be in the same range than the power and ground voltages. A sort of coherence has to be respected.

A digital circuit is made of interconnected gates, and so the input signal of a given gate is the output signal of its driving gate. Considering the driving gate, when its output is high (resp. low), the p-transistor (resp. n-) network of the driving gate is ON connecting the power (resp. ground) line to its output. Consequently the output signal of the driving gate is just an image of the power (ground) voltage.

In case of power and ground line with SSN, the output signal of the driving gate is an image of the bouncing Vddchip(t) or bouncing Gndchip't).

As this point, we must distinguish two different situations:

- SSN within a coherent digital block,
- SSN between non-coherent digital blocks.

5.1. SSN within a coherent digital block

A coherent digital block is a set of logic gates with the same power and ground lines. Figure 7 illustrates this situation where the driving and driven gates have the same Vddchip and Gndchip lines. In this case, we have:

- the driven gate is biased by Vddchip(t) and Gndchip(t)
- the range of the output signal of the driving gate is from Gndchip(t) and Vddchip(t).

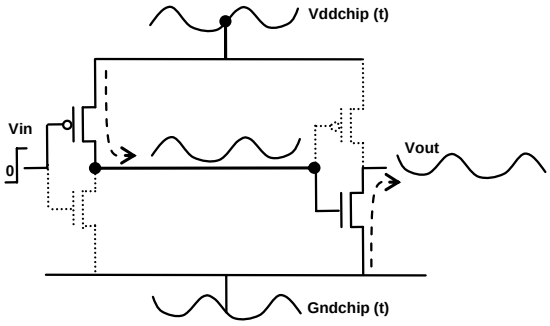


Figure 7: Coherent digital block

According to the ITF in section 3, the driven gate works correctly and perfectly interprets its input signal level. This is true at any time and for any gate in the coherent block. The following property can be written.

***Coherent Block Property*: For a standard CMOS gate operating into a coherent digital block, the input signal range is always coherent with the power and ground voltage whatever the amount of SSN.**

$$Vin(t) \in \{Gndchip(t), Vddchip(t)\} \quad (6)$$

This property surprisingly demonstrates that a coherent digital block performs its correct logic function whatever the amount of SSN. In order to validate this demonstration, the two following interesting experiments have been made.

First, the C432 benchmark circuit is simulated with the double parasitic cells in the same conditions than figure 4. Remember that in figure 4, the output signal was impossible to interpret. But in this case, we implement in the SPICE description an additional module which permanently compares the output signal to the instantaneous logic threshold Vth(t) evaluated as a function of Vddchip(t) and Gndchip(t); note that the module produces a 'clean 1' (resp. 'clean 0') if the output is higher (resp. smaller) than Vth(t). Figure 8 gives the result of the simulation with the noisy output signal and the 'clean' digital one.

Combinational Coherent Block Observation: In any case, whatever the input vectors used in the simulation, the clean signal perfectly corresponds to the fault free response of the circuit. This demonstrates that the coherent combinational circuit correctly performs its logic function.

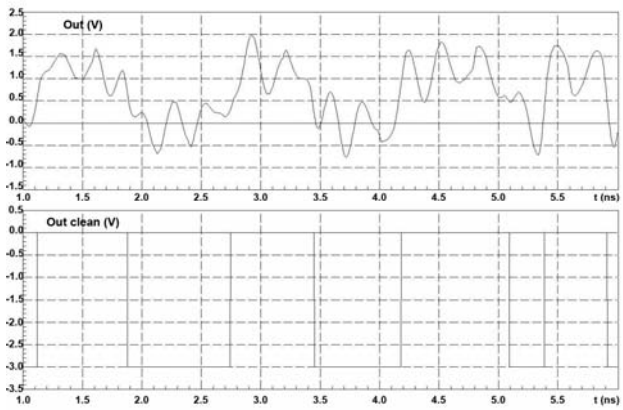


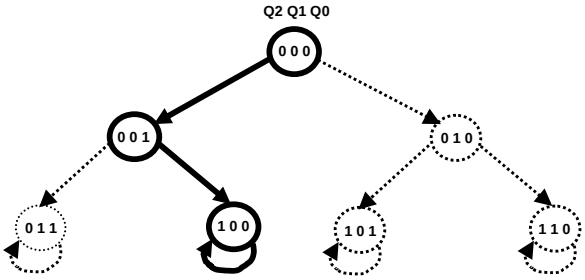
Figure 8: Cleaned output of the C432

Another very interesting simulation is performed with a sequential circuit. In this case we electrically simulate the state machine corresponding to the graph in figure 9. In this case a given input sequence of vector is applied to the input of the state machine. According to the graph, the correct final state of the machine should be state '100'. The machine is simulated with the double parasitic cells and so a high amount of SSN appears in all the logic nodes. In case of logic error due to the SSN, the final state of the machine will be different.

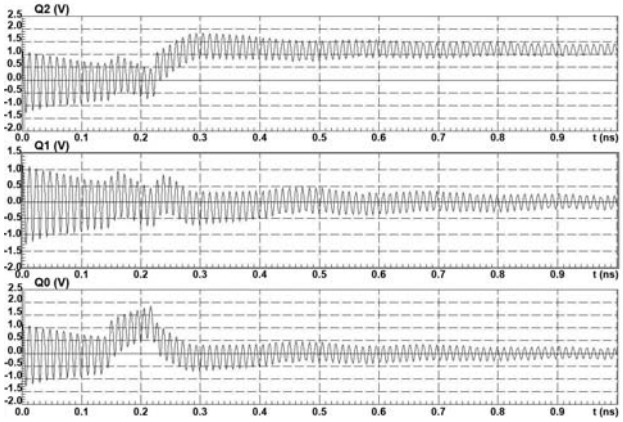
For a sequential machine, we do not need to clean the signals as for the previous example of combinational C432 circuit. Indeed, we apply the input sequence of vectors, the power and ground lines oscillate, and we just wait that the oscillations vanishes to check the final state.

In figure 9, it can be observed that the final state corresponds to the fault-free state.

***Sequential Coherent Block Observation*: In any case, whatever the input vectors used in the simulation, the final state of the machine perfectly corresponds to the state of the fault free machine. This demonstrates that the coherent circuit correctly performs its logic function.**



a) Graph



b) Final State

Figure 9: Sequential circuit simulation

5.2. SSN between non-coherent digital blocks

Non-coherent digital blocks are different blocks of logic gates with different power and ground lines. Figure 10 illustrates this situation where the driving and driven gates have different Vddchip and Gndchip lines. In this case, we have:

- the driven gate is biased by $Vddchip^2(t)$ and $Gndchip^2(t)$
- the range of the output signal of the driving gate is from $Gndchip^1(t)$ and $Vddchip^1(t)$.

In the driven gate, the input signal may not be coherent with the power and ground voltages. The gate may exhibit some logic error. From this analysis, we clearly identify the interface between non-coherent blocks as the source of logic errors.

***Non-Coherent Block Property*: In a standard CMOS circuit, signals interfacing non-coherent digital blocks are the potential source of logic errors in presence of SSN.**

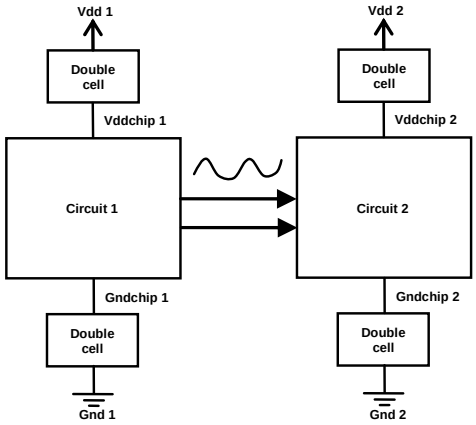


Figure 10: Non-Coherent digital blocks

This important property has a number of consequences in design and test:

- Concerning design, a special attention must be paid to the implementation in the circuit of different power domains. We imagine that specific cells could be designed to adapt the level of signal in the interfaces.
- Concerning DFT, integrated sensors could be of great help to check if the swings from different non-coherent blocks are compatible or not.
- Concerning test, vectors must be generated targeting logic errors originated at the block interfaces.

6. Conclusion

This paper analyzes the electrical behavior of digital circuits in presence of Simultaneous Switching Noise (SSN). It is first demonstrated that 2 conditions called the 'Minimum Switch Condition' and the 'Signal Coherence Condition', must be fulfilled in order to guarantee the correct logic behaviour of a digital circuits. The first condition is observed to be fulfilled even with large amount of SSN. The second condition called 'Signal Coherence Condition' is proved to be fulfilled within power coherent digital blocks. However the interface between non-coherent logic blocks is demonstrated to be the origin of logic errors. Design and test techniques targeting these interfaces have to be developed.

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