Explicit Evaluation of Short Circuit Power Dissipation for CMOS Logic Structures

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EXPLICIT EVALUATION OF SHORT CIRCUIT POWER DISSIPATION FOR CMOS LOGIC STRUCTURES

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ABSTRACT

For supply voltage standards such as Vdd > V_{TN} + |V_{TP} | short–circuit power dissipation significantly contributes to the total power dissipation in ICs. We propose a new alternative for the estimation of the short–circuit power dissipation, Psc, in CMOS structures. A first order calculation results in an explicit formulation for Psc, which clearly shows up the design and load parameters. Validations are performed on different configurations of inverters by comparison with HSPICE simulations. Discussions on the relative importance of short–circuit and dynamic power dissipation is given, together with considerations allowing an easy extension to gates.

I – INTRODUCTION

Design for low power implies facilities in exploring trade–offs between area performance and power. Area and performances of CMOS structures have been the subject of large investigations [1–3]. Power estimation of CMOS gates is considered in recent papers [4–6]. Due to the major difficulties in clearly defining the components involved in power estimation of CMOS structures, efforts on low power design address mostly alternatives at logical synthesis level [7].

Basically, three components of power have to be considered:

– one static component caused by junction leakage currents, which is negligible as long as

$V_{DD} > V_{TN} + |V_{TP}|$,

– two components arising during input signal transitions : the dynamic and the short circuit power dissipations.

Dynamic power dissipation, Pd, is the power necessary to charge and discharge the output load of the gate. It is given by :

$$Pd = \eta \ CL \ V_{DD}^2 . f \qquad (1)$$

where f is the clock frequency, η the gate activity and CL the output load, constituted of the gates connected to the output and of the parasitic capacitances :

$$CL(i) = \Sigma_j C_{IN}^j + Cwire + Cpar(i) \qquad (2)$$

where Cin, Cwire, Cpar respectively represent the gate input capacitance, the parasitic interconnect and diffusion capacitances of each gate (i).

If the dynamic power dissipation is independent of the input signal transition time, it depends upon the design of the logic gate (i) (the sizes of the transistors constituting the gate) through Cpar(i) and the design strategy used for the gates, through the active fanout term, $\Sigma_j C_{IN}^j$.

The short circuit power dissipation, Psc, is due to the simultaneous conduction of the P and N blocks, during the time spent by the input signal to vary from *VTN* to *VDD–|VTP|* (and vice versa), causing a direct current to flow between the supply rails. This short circuit current has been observed dependent on the input ramp, the load and transistor sizes of the gate. Different formulae [8–10] have been derived for Psc evaluation, with different accuracy levels, depending on the approximations used to model the currents and to estimate the input signal dependency. If these formulae can be used in computer programs for short circuit power estimation[11], they don't allow a direct comparison of dynamic and short circuit components with respect to design parameters.

We present here a first order formulation for short circuit power dissipation in CMOS inverters, showing up explicitely design and performance parameters, such as transistor widths, gate input and output rise and fall times, allowing a direct comparison of the power dynamic and short–circuit components.

Using a circuit technique proposed by Kang and Yacoub [12,13], we will first define a simulation reference for average short circuit power dissipation in CMOS inverters and illustrate the *Psc* dependencies with respect to the design parameters.

We will then propose an alternative definition for the short circuit power dissipation, through an equivalent short circuit capacitance, that we will validate with respect to the reference term defined in the preceding part.

In the same way that we proposed an explicit formulation for delays [14,15], used to modelize the time variation of the inverter input output voltages, we finally establish a first order evaluation of the short circuit power dissipation, showing clearly up the design and performance parameters. Validations are obtained with respect to the reference terms, for various configurations.

Discussion is then given on the extension to gates and the possibility of definition of low power design criteria.

II – SHORT CIRCUIT POWER DISSIPATION SIMULATIONS

We first define a reference for short circuit power dissipation in CMOS gates. We use for that SPICE simulations on the powermeter arrangement shown in figure 1, and proposed by Kang and Yacoub [12,13].

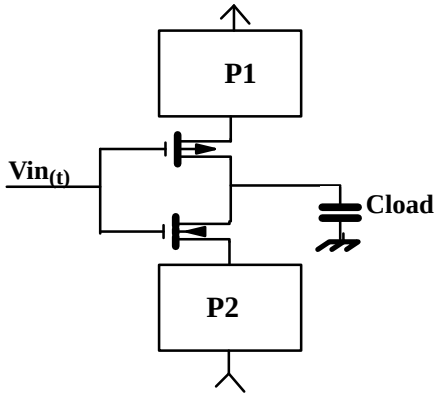

Fig. 1 : Circuit with the powermeters of [12,13] to simulate short–circuit power dissipation in CMOS inverters.

Let us consider a gate (i), controlled by a gate (i–1) delivering a periodic waveform of period T, with identical rise and fall times, defined as $2t_{LH}(i–1)$ and $2t_{HL}(i–1)$, respectively, as shown in figure 2. We assume that the period of the controlling signal is large enough to allow the output to reach a stable state before T.

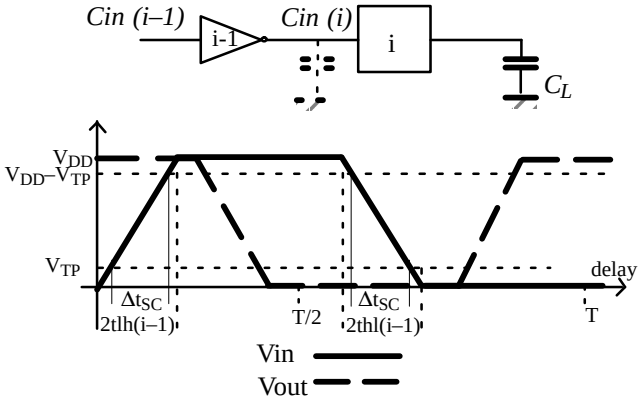

Fig.2 : Specifications of the input and output voltages used for power dissipation estimation.

Under those conditions the powermeter indications at time *T/2* and *T* reflect the short circuit and dynamic power dissipation in N and P blocks of the gate, as detailed below :

$$P_1\left(\frac{T}{2}\right) = (P_{SC})^{HL}$$
$$P_1(T) = (P_{SC})^{HL} + (P_d)^{LH} + (P_{SC})^{LH} \quad (3)$$
$$P_2\left(\frac{T}{2}\right) = (P_{SC})^{HL} + (P_d)^{LH}$$
$$P_2(T) = (P_{SC})^{HL} + (P_d)^{HL} + (P_{SC})^{LH}$$

Average short circuit power dissipation at T, is then directly obtained from the combination :

$$P_{SC}(T) = (P_{SC})^{HL} + (P_{SC})^{LH} \quad (4)$$
$$P_{SC}(T) = P_1(T) - P_2\left(\frac{T}{2}\right) + P_1\left(\frac{T}{2}\right)$$

We first simulate power dissipation in an inverter with different internal configuration ratio ($k=W_P/W_N$), load and input control conditions. Simulations are performed with HSPICE, the input signal period has been imposed equal to 200ns, much greater than the different switching times involved. The internal set up of the powermeter parameters has been chosen in agreement with the conditions defined in [12,13].

The resulting short circuit power dependency to the design parameters is illustrated in figures 3–5. Figures 3 and 4 give the Psc dependency to the load for different internal configuration ratio and input transition time values, respectively. The N transistor width of stage (i) has been used as a reference ($C_{N(i)}=5fF$ for all investigations). Figure 5 enlightens the Psc dependency to the input transition time for constant load. In order to clarify the comparisons we specify the different transition times involved by the different loads and control signals, as ratio of the circuit capacitances such as :

$C_L/C_{IN(i)}$ = ratio between the output load of inverter (i) and its input capacitance, represents the fanout factor of the $(i)^{th}$ stage and determines the output transition time.

$C_{IN(i)}/C_{IN(i–1)}$ = ratio between the input capacitance of $(i)^{th}$ and $(i–1)^{th}$ stages, represents the fanout factor of the $(i–1)^{th}$stage and determines the input transition time on the $(i)^{th}$ stage.

These capacitance ratios have been recognized significative and are widely used to represent trends of switching times [4,14].

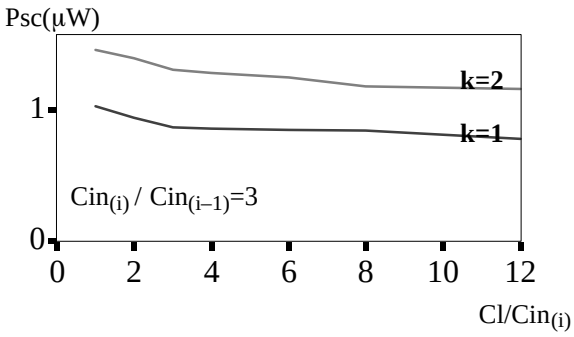

Fig3 : Short–circuit power dependency to the load for different internal configuration ratio values and a constant input voltage ramp defined by $Cin_{(i)}/Cin_{(i–1)} = 3$ ($2thl_{i–1} = 2tlh_{i–1}=0.4ns$).

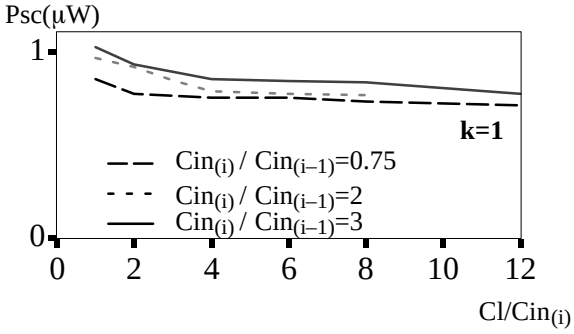

Fig.4 : Short–circuit power dependency to the load for different input voltage ramps ranging from 0.1 to 0.4ns ($Cin_{(i)}/Cin_{(i-1)}$=0.75–3, respectively), the internal configuration ratio is chosen equal to the value corresponding to the lowest power dissipation.

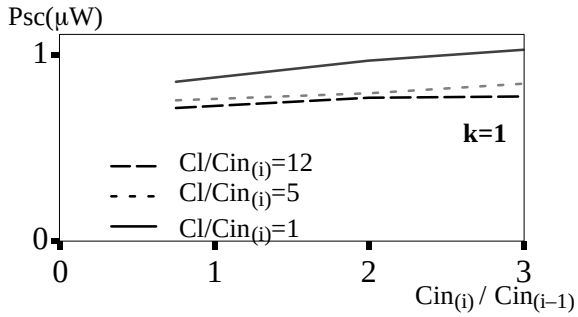

Fig.5 : Illustration of the short–circuit power dependency to the input transition time for constant load.

We observe that Psc dissipation decreases when the load increases, and Psc increases with the internal configuration ratio value increase ie with the strength of the transistors in short circuit (fig. 3) as expected. Psc also increases with the input transition time increase ie when the ratio $C_{IN(i)}/C_{IN(i-1)}$ increases (fig. 4). This trend is enlightened in figure 5 where we plot for constant load the Psc variation with the duration of the input ramp. These variations, initially observed by Veendricks [8], are illustrated here with respect to the design parameters and represent the trends to be reproduced by any short circuit power dissipation modelization. This is what we will try to get in the next part. To conclude this part, figure 6 represents for different transition times the load dependency of the ratio *Psc / Pd* (with $\eta=1$). This illustrates the relative influence of the short circuit component, which, for specific design conditions, is far to be negligible.

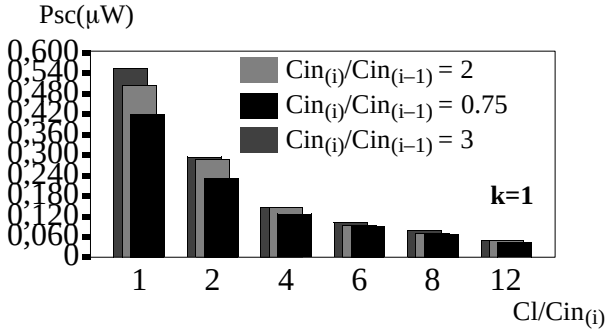

Fig.6 : Illustration of the ratio (Psc/Pd) dependency to the load for different input transition times .

III – EQUIVALENT MODEL FOR AVERAGE SHORT CIRCUIT POWER EVALUATION

As shown in the preceding part, the ratio *Psc / Pd* can give indications on available design trade offs for low power. For a given operating frequency and power supply, the dynamic power depends on the total load capacitance involved. This capacitive load, constituted of the layout parasitic and almost of the gate input capacitances, is a direct consequence of the synthesis and design choices : it completely controls the speed performance of the design.

In order to easily compare *Psc* and *Pd* we propose here an alternative to modelize short circuit power dissipation through an equivalent short circuit capacitance.

Physically the short circuit power dissipation is produced by the current flowing from V_{DD} to ground, through P and N blocks, during the time spent by the input voltage to vary from V_{TN} to $V_{DD}-|V_{TP}|$. Let us call Δtsc this time interval. We can equivalently consider this current conduction process as a charge transfer:

$\Delta Q1 = I_{LH} . \Delta tsc$ for the input rising edge ($I_{LH} = I_P$),(5)

$\Delta Q2 = I_{HL} . \Delta tsc$ for the input falling edge ($I_{HL} = I_N$),

where I_{LH} and I_{HL} represent the average short circuit currents evaluated in N and P transistors respectively.

Let us define $\Delta Q = \Delta Q1 + \Delta Q2$ the total charge transfer during a period of the input signal. An expression for an equivalent short circuit capacitance can then be obtained from:

$$C_{SC} = \Delta Q / \Delta V \qquad (6)$$

where $\Delta V = V_{DD} - V_{TN} - |V_{TP}|$ represents the input voltage swing during Δtsc.

Note that C_{SC} has no physical meaning, and is just an equivalent way to represent the charge transfer. An interesting expression is then obtained in writing short circuit power dissipation in the same way than the dynamic one, using the C_{SC} parameter. This results in :

$$P_{SC} = \eta\, C_{SC}\, V_{DD}^2 \cdot f \qquad (7)$$

where the different coefficients have been defined in the introduction.

To validate this result, we replace the powermeters of figure 1 by amperemeters and simulate the short circuit current for the different conditions examined in the preceding part. From these simulated values of currents it is then easy to calculate *CSC* and *PSC* from equ. 6 and 7.

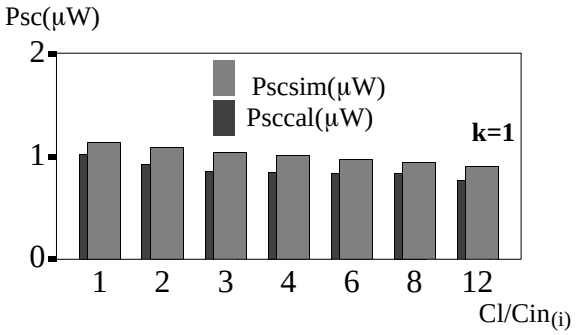

Fig.7 : Comparison between the short–circuit power values calculated from the simulated values of the average currents (Psc_{cal}) and the simulated values of the short–circuit power (Psc_{sim}).

In figure 7 we compare the values of the short circuit power calculated (equ. 7) from the simulations of average currents, to the values obtained in the preceding part from the simulations through the powermeters. The good agreement

obtained confirms the validity of the preceding approach in defining equivalent short circuit capacitance.

The next step consists now in calculating the values of C_{SC}. It is for that just necessary to calculate the average value of the short circuit current crossing N and P transistors (for input falling and rising edges respectively).

Let us give here some details about this calculation, we choose the input rising edge as an example.

We calculate $<I_P(t)> = I_{LH}$ as follows :

$$I_{LH} = \frac{1}{\Delta_{SC}} \left(\int_{t_{(V_{IN}=V_{TN})}}^{t_{I'}} I_{Plin}(t)dt + \int_{t_{I'}}^{t_{(V_{IN}=V_{DD}-|V_{TP}|)}} I_{Psat}(t)dt \right) \quad (8)$$

where the summations are bounded by the significative times of the short circuit operating mode.

Taking for convenience the origin of times at the beginning of the short circuit (t for $V_{IN} = V_{TN}$), equation (8) leads to :

$$I_{LH} = \frac{1}{\Delta_{SC}} \left(\int_{t_0}^{t_{I'}} I_{Plin}\ (\ t\ )\ dt + \int_{t_{I'}}^{t_{END}} I_{Psat}\ (\ t\ )\ dt \right) \quad (9)$$

To solve this equation, input/output waveforms and current laws must be considered.

In order to get practical expressions we consider, as shown in figure 2, linear input/output waveforms with slopes defined by the loading factors, as discussed in part II, such as:

$$V_{IN} = V_{TN} + \frac{V_{DD}}{2\ t_{LH(i-1)}}\ .\ t$$

$$V_{OUT} = V_{DD} \left(1 - \frac{t}{2\ t_{HL(i)}} \right) \quad (10)$$

Bounds t_I' and t_{END} are then easily calculated from the conditions :

$$|V_{GSP}| - |V_{TP}| = |V_{DSP}| \quad \text{for } t_I\text{'},$$

$$t(V_{IN}=V_{DD} - |V_{TP}|) - t(V_{IN}=V_{TN}) \quad \text{for } t_{END}. \quad (11)$$

From equ.10 & 11 we directly obtain :

$$t_{I'} = \frac{2\ (1 - b)\ t_{LH(i-1)}}{1 + \frac{t_{LH(i-1)}}{t_{HL(i)}}}$$

$$t_{END} = \Delta\ t_{SC} = 2\ (1 - b)\ .\ t_{LH(i-1)} \quad (12)$$

with $b = (\ |V_{TP}| + V_{TN}\ ) / V_{DD}$.

For the current expressions we use the standard Shichman and Hodges model, which appears to be sufficient for average calculations, short channel effects being later introduced through calibration coefficients on the effective mobility length ratio as discussed in [16].

After some tedious but not complicated calculations, equ. 9 gives :

$$< I_p(t) > = \frac{\beta_P}{6}\ V_{DD}^{\ 2}\ (1 - b)^2\ \frac{t_{LH(i-1)}}{t_{LH(i-1)} + t_{HL(i)}} \quad (13)$$

and an equivalent form for the average short circuit current calculated during the input falling transition is given in 14 :

$$< I_N(t) > = \frac{\beta_N}{6}\ V_{DD}^{\ 2}\ (1 - b)^2\ \frac{t_{HL(i-1)}}{t_{HL(i-1)} + t_{LH(i)}} \quad (14)$$

where β_N and β_P are the usual conductance factors ($\beta_{N,P} = \mu\ Cox\ (\ W / L\ )_{N,P}$)

Using these equations it is then easy to evaluate from equ.5–7 the short circuit power as :

$$P_{SC} = \eta f \frac{V_{DD}^{\ 4}(1 - b)^2}{6} \left(\frac{\alpha_1' \beta_P t_{LH(i-1)}}{t_{LH(i-1)} + t_{HL(i)}} + \frac{\alpha_1'' \beta_N t_{HL(i-1)}}{t_{HL(i-1)} + t_{LH(i)}} \right)$$

where the b value is limited to the range $b < 1$.

As shown in [14] the slope factors between brackets can be expressed as a function of design and loading parameters such as :

$$\frac{t_{HL(i)}}{t_{LH(i-1)}} = \frac{\alpha_2' \frac{C_L}{C_{N(i)}}}{\frac{\mu_N}{\mu_P}\ \frac{(1+k)_i}{k_{(i-1)}}\ \frac{W_N}{W_{N(i}}} \quad (16)$$

$$\frac{t_{LH(i)}}{t_{HL(i-1)}} = \frac{\alpha_2'' \frac{\mu_N}{\mu_P}\ \frac{C_L}{k_i\ C_{N(i)}}}{\frac{(1+k)_i\ W_{N(i)}}{W_{N(i-1)}}} \quad (17)$$

where k is the internal configuration ratio, C_L the output load of the cell under consideration and $W_{N(i)}/W_{N(i-1)}$ characterizes the input slope.

As given in equations 15 and 16, the short circuit power dependence on design parameters appears explicitly and the trends obtained correspond to the simulated one derived in part II :

– no P_{SC} for b greater than 1 ie for $V_{DD} < V_{TN} + |V_{TP}|$,

– for constant input transition time ($t_{HL,LH(i-1)} = Ct$), P_{SC} decreases when the load increases ($t_{HL,LH(i)}$ *ie* C_L increases), P_{SC} increases with the increase of configuration ratio values (k, β_N ,β_P), and with the input transition time increase ($t_{HL,LH(i-1)}$ or $W_{N(i)} / W_{N(i-1)}$).

This partly confirms the interest of this approach.

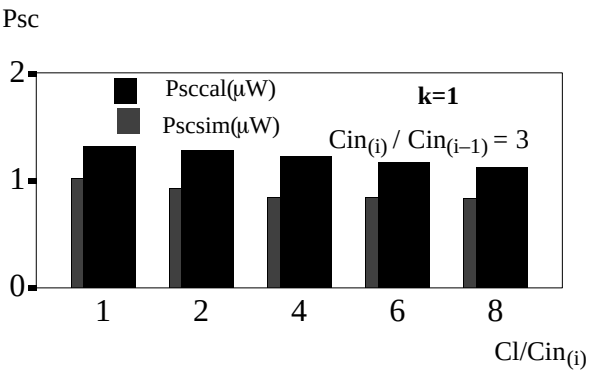

Fig.8 : Comparison of the values of the short–circuit power dissipation calculated (Psccal eq.15), to the values obtained from simulations (Pscsim), the input voltage ramp is 0.4ns and the internal configuration ratio=1.

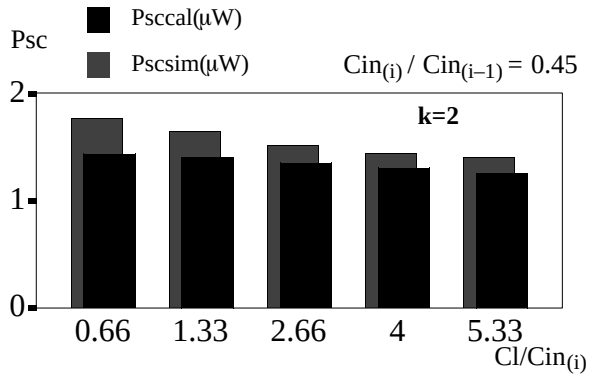

Fig.9 : Comparison of the values of the short–circuit power dissipation calculated (eq.15) to the values obtained from simulations, the input voltage ramp is 0.3ns and the internal configuration ratio = 2.

Figures 8 & 9 give a more complete validation in comparing for different internal configuration ratios the values of the short–circuit power dissipation calculated from eq.15 to the values of the short–circuit power dissipation obtained in part II.

Let us remind here that simulations have been performed with a 1.2μm process. In order to correct the approximation level used to obtain the explicit expression for Psc, we use calibration coefficients on :

– β_P, β_N ($\alpha 1$), to take into account the short channel effects in the definition of effective mobilities and transistor length,

– tlh(i) & thl(i) ($\alpha 2$), to take into account the input slope effects [15].

Results shown on fig.8 & 9 have been obtained with : $\alpha 1$=1.4, $\alpha 2$ = 0.09 for the P transistor, and $\alpha 1$ = 0.5, $\alpha 2$ = 0.07 for the N transistor, these values being directly derived from calibration on small and large load configurations.

Despite the low approximation level used here, the agreement between calculated and simulated Psc values is quite good and justifies the effort made to get explicit expression.

IV – DISCUSSION AND CONCLUSION

In designing structures for low power applications, one of the main relevant features is the evaluation of the relative short–circuit and dynamic power dissipation contribution versus design and synthesis choices. This point is illustrated on fig.10 and 11, where we plot the ratio Psc / Pd dependency to the load for both calculated and simulated Psc values with respect to the cases shown on fig.8 & 9.

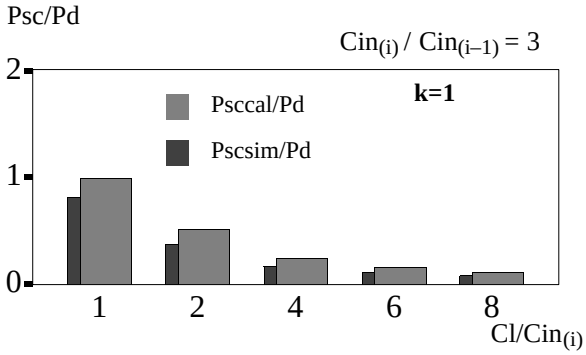

Fig.10 : Load dependency of the relative importance of the short–circuit power dissipation with respect to the dynamic one; calculated (Psccal) and simulated (Pscsim) values are compared for an input voltage ramp=0.4ns and an internal configuration value of 1.

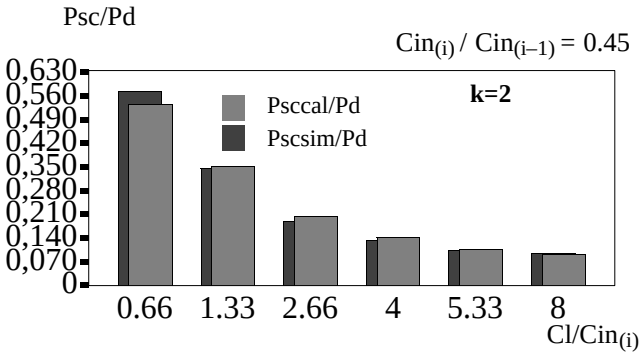

Fig.11 : Load dependency of the relative importance of the short–circuit power dissipation with respect to the dynamic one; calculated (Psccal) and simulated (Pscsim) values are compared for an input voltage ramp=0.3ns and an internal configuration value of 2.

For relatively fast input transition (ie : k=1, $Cin_{(i)}$ /$Cin_{(i-1)}$=3 represents medium load conditions for real cases) the short–circuit component is quite important if we consider load conditions such as Cl / $Cin_{(i)}$ < 3 which corresponds to a usual physical design fanout factor for speed.

Note here that we just considered configurations of invert-

ers. Extension to gates is straightforward : we only need to modify the short–circuit current expression. Since it corresponds to a "static" current, gates can be reduced to equivalent inverters that are easely defined by width of transistors (N or P) equal to the average width of the transistors (N or P) (or to the sum of the parallel transistor W for the critical cases) and length equal to the length of the transistors belonging to the parallel array or equal to the sum of the length for transistors belonging to the serial array.

Under those conditions the resulting equivalent inverter for a given gate will be defined with different internal configuration ratio : k<1 for Nor gates and k>1 for Nand gates. However, short channel effects will be more difficult to approximate especially in serial arrays of transistors and this part will be later extensively investigated. An interesting application will then be to evaluate alternatives in logical decomposition for speed trading serial transistors with logical depth.

As a summary we have proposed a new approach to calculate the short–circuit power dissipation in CMOS structures.We first defined a virtual short–circuit capacitance as an indicator of short–circuit power dissipation in CMOS inverters which appeared to be an efficient way of comparing short–circuit and dynamic power dissipation in terms of design parameters.Validations of this concept have been obtained through a standard measurement circuit technique for low power. And finally, using the concept of the equivalent short–circuit capacitance, and low level models for currents and variations of input/output voltages, calculations have been successful in obtaining an explicit formulation for the short–circuit power dissipation showing up clearly design, technology, load and control parameters.

We validate this expression for inverters in different situations by comparing calculated values of Psc to simulated ones. The quality of the results reinforce us in further investigations to gates and complex decomposition.

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