On-Chip Generator of a Saw-Tooth Test Stimulus for ADC BIST

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Abstract: In the context of analog BIST for A-to-D converters, this paper presents an implementation of an on-chip ramp generator. It is demonstrated that the proposed original adaptive scheme allows the internal generation of a highly saw-tooth signal with a very precise control of the signal amplitude. In addition, the implementation of the adaptive ramp generator exhibits a very low silicon area.

Key words: ADC testing, BIST, analog stimulus generation

1. INTRODUCTION

The use of Built-In Self-Test (BIST) for high volume production of mixed-signal ICs is desirable to reduce the cost per chip during production testing by the manufacturers. Within the past few years, analog and mixed-signal BIST have received the growing attention of industry and research community in order to alleviate increasing test difficulties. In particular, a number of papers deal with the problem of ADC and DAC testing.

For mixed-signal ICs with an ADC and a DAC, many of the proposed BIST techniques uses an all-digital approach [1-3] based on a reconfiguration in test mode such that the circuit appears all digital by connecting the analog output of the DAC to the input of the ADC, possibly via some analog block under test. Another all-digital BIST approach [4,5] exploits the digital signal processing (DSP) capabilities to determine characteristic parameters of the converters. Finally, an interesting approach has been proposed more recently, which is based on a polynomial-fitting algorithm to implement DAC and ADC BIST [6].

The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: 10.1007/978-0-387-35597-9_40

In case of mixed-signal ICs including solely an ADC, an original approach is detailed in [7], which relies on a reconfiguration in test mode that creates oscillation in the circuit. Measurements on these oscillations guarantee some tests. A more classical ADC BIST scheme implies the generation of an analog test stimulus and the digital processing of the ADC outputs. In this context, a specification-oriented approach is the only way to determine ADC parameters. A BIST module is proposed in [8] that partially overcomes this drawback since it permits to evaluate the converter linearity. Only the LSB is used for the determination of the linearity, the global functionality of the converter being tested with the comparison between the remaining bits and a counter clocked by the LSB. A more complete evaluation of the converter characteristics can be obtained by means of the histogram test method and BIST analyzers implementing this technique are presented in [9,10].

Concerning on-chip test stimulus generation, only a limited number of BIST solutions have been proposed. Original generators providing single or multi-tone analog signals are described in [11-13] to make frequency-domain test of converters. Time-domain testing is addressed in [14,15] with solutions for generating a precise analog ramp signal.

The objective of this paper is to develop an on-chip generator dedicated to linear histogram testing of ADCs. The histogram method is one of the most popular techniques for ADC testing in the industrial context. It actually relies on probabilistic methods to deduce the behavior of the circuit under test. The basic idea behind this approach is that the probability distribution behavior of the output signal is directly related to the input probability distribution through the circuit's transfer characteristic. The histogram method therefore involves the application of a given analog signal to the ADC input and the record of the number of times each code appears on the ADC outputs. Processing the measured data against a reference histogram then permits extracting the circuit's characteristics. To achieve statistically satisfactory results, this technique requires a lot of samples. However in practice, it is difficult to collect such a high number of samples applying a single ramp test stimulus. A multi-cycle approach is usually adopted which consists in sampling several cycles of the input signal within the test interval. In particular for linear histogram testing, the input test stimulus should be either a saw-tooth or a triangle signal. It is therefore the purpose of this paper to develop an on-chip saw-tooth generator. A drastic reduction of the testing costs would then be obtained since the ADC test can be performed on standard digital test equipment instead of a sophisticated and costly mixed-signal tester.

The paper is organized as follows. Section 2 gives the generator requirements needed to ensure accurate ADC characterization in terms of ramp linearity and amplitude control. The basic principles of the ramp generation are recalled in section 3 and the need of self-calibration to take into account parameter fluctuations is shown. Then our proposal for accurate self-calibration saw-tooth generator is described in section 4 and the calibration procedure is detailed. Also simulations are implemented that demonstrate the validity of our approach. Finally, the performance of the generator are analyzed and discussed in section 5.

2. GENERATOR REQUIREMENTS

One first obvious constraint concerns the silicon area since the generator has to be fabricated on the same IC as the circuit under test. The generator must occupy minimal silicon area so that the resulting overhead to the system is economically viable.

The second constraint concerns the quality of the test signal. Indeed, the histogram technique relies on the fact that the probability distribution behavior of the output signal is directly related to the input probability distribution through the circuit's transfer characteristic. The ADC characteristics are then extracted by comparison between the measured histogram and a reference histogram corresponding to the ideal input signal distribution. Obviously, the correct determination of these characteristics depends on the quality of the input signal whose probability distribution should be as close as possible to the ideal one. In particular, because Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are two key parameters of the converter measured with the histogram technique, the input signal should exhibit a quality exceeding that of the circuit under test in terms of linearity. Another important parameter of the input signal involved in the determination of the ADC characteristics is the amplitude of the test stimulus.

For illustration, figure 1 compares the histogram measured through a perfect n-bit converter in case of an ideal saw-tooth signal and a degraded saw-tooth signal containing linearity and gain errors. In the ideal case, we have a uniform distribution with an equal count for all codes, the value of this count being directly proportional to the number of samples (N) collected to build the histogram.

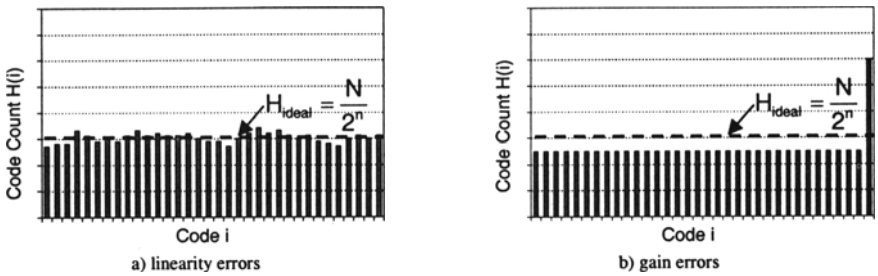


Figure 1. Influence of the errors on the input signal

In case of linearity errors included in the input saw-tooth signal, we can observe some variations in the code counts (figure 1.a). Even if these variations are due to non-idealities of the input signal, they will be considered as linearity errors of the converter when comparing the measured histogram to the ideal reference one. Consequently, it is clear that the input signal must exhibit linearity errors much lower than the DNL and INL values to be measured for the converter under test.

Ideally, the input signal should exactly cover the full scale range of the converter in order to obtain the ideal reference histogram. Now if we assume a variation in the amplitude of the saw-tooth signal, for instance an increase, we obtain the histogram of figure 1.b. In this case, we observe a uniform distribution for all codes but with a lower code count, and a much higher count for the last code. However, this histogram is very different from the ideal reference histogram demonstrating that that an increase of the input signal amplitude will strongly affect the measurement of the ADC characteristics.

These results clearly reveal that it is of crucial importance to be able to control the amplitude of the generated saw-tooth signal. This points out a specific requirement for the test generator in the context of a BIST solution. Because the saw-tooth signal is generated on-chip, unavoidable process variations have to be taken into account and the generator should be insensitive to these variations with regard to its amplitude.

As a summary, a practical saw-tooth generator for linear histogram testing of ADCs should respect some specific test constraints. It must be capable of generating a signal with quality exceeding that of the circuit-under-test in terms of linearity and should be insensitive to process variations with regard to the signal amplitude. These two features guaranty the test quality. In addition, it must occupy minimal silicon area so that the resulting overhead to the system is economically viable.

3. BASIC RAMP GENERATOR

3.1 Ramp generation principle

A very simple approach to generate a ramp voltage consists in charging a capacitor by a constant current. The simplified schematic of such a ramp generator is given in figure 2.a. It comprises in addition to the constant current source and the charging capacitor, a switch to control the duration of the ramp and a switch to initialize the structure.

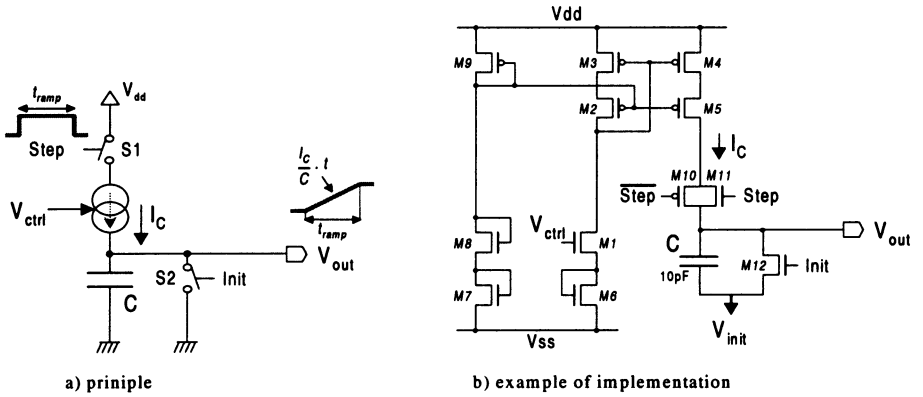


Figure 2. Voltage ramp generation

As an example of integrated circuit implementation, we consider the ramp generator described in figure 2.b. Transistor *M1* is the current source, transistors *M2* through *M5* form a cascode current mirror, transistors *M6* through *M9* correspond to biasing transistors and *C* is the charging capacitor. Transistors *M10-M11* operate as a switch to stop the charging of the capacitor when "*Step*" is at logic 0. Transistor *M12* is used to initialize the structure at a given predetermined voltage V_{init}, typically ground for a ramp with positive values only and a negative voltage for a symmetrical ramp around 0.

As a case study, this structure has been implemented with a charging capacitor of 10pF and a charging current of 0.3µA. It allows to generate a symmetrical ramp of 3V amplitude with a duration of 0.1ms using a negative initialization voltage of -1.5V. Iterating the ramp generation process therefore should permit to generate a saw-tooth signal with a frequency around 10kHz. This corresponds to the desired input signal frequency to be applied to the ADC for performing the histogram test.

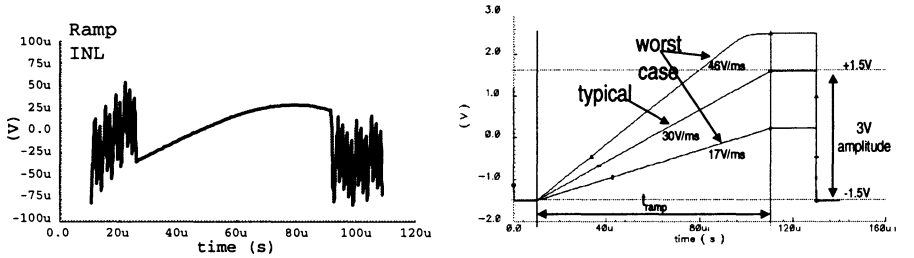
3.2 Performances of the basic ramp generator

As stated in the previous section, the quality of the generated ramp is a crucial point since the ramp has to be used as test stimulus for the ADC. In particular, the generated ramp should exhibit high-linearity and precise amplitude to be used for histogram testing.

So first, we determine the linearity of the generated ramp voltage. This linearity actually depends on the ability of the current source to deliver a constant current and we can expect good performance due to the use of the cascode current mirror. The basic ramp generator has been simulated using Hspice and results are detailed in figure 3.a with the ramp signal along with the corresponding INL.

We obtain a ramp signal of 3V amplitude with a duration of 0.1ms and we measure a maximum INL of 80µV. This corresponds to a slope distortion lower than 0.003%. The basic ramp generator therefore exhibits good linearity performance.

This linearity has to be compared to the resolution of the converter to be tested. We obtain a linearity higher than 15 bits for the ramp generator (considering a 3V input range). According to the requirement of at least 2bits better resolution for the test stimulus than for the converter-under-test, the basic ramp generator is therefore suitable to test a 12-bit ADC.



a) linearity b) slope variation

Figure 3. Linearity and slop variation of the basic ramp generator

Then we study the sensitivity of the basic ramp generator to process fluctuations. Since the duration of the ramp is controlled by the *Step* signal, the ramp amplitude actually depends on the slope of the generated ramp voltage. This slope is determined by the current source and capacitor values. Hence, the slope precision just depends on the ability of precisely controlling the value of the charging current and the value of the capacitor. However, it is extremely difficult to obtain a precise control of these values due to fluctuations in the manufacturing environment. To illustrate this point, various electrical simulations have been performed taking into account the

typical and worst case models provided in a CMOS 0.6µm technology. Simulation results are summarized in figure 3.b.

The extreme sensitivity of the structure to process variation clearly appears on these results. Indeed in the typical case, we obtain the desired ramp voltage with an amplitude of 3V for a ramp duration of 0.1ms, which corresponds to a ramp slope of 30V/ms. Looking at worst case simulation results, we observe that the final output voltage varies from 0.2V up to 2.5V, which corresponds to variations in the ramp slope as high as ±50%. This imprecision mainly comes from the uncorrelated variations of the current source and capacitor values. These results clearly demonstrate that the basic ramp generator suffers from very poor performance in terms of slope precision, which prevents its direct use as test stimulus generator for histogram testing of ADCs.

4. CALIBRATED SAW-TOOTH GENERATOR

In order to correct the inaccuracy of the basic ramp generator, the authors have developed an original adaptive scheme [15]. The basic principle consists in comparing the generated ramp voltage to a predetermined reference voltage and feeding back an adjustment signal so that the ramp voltage converges with the reference voltage within a given period. The general block-diagram of the corrective scheme comprises 3 blocks :

- the **ramp generator circuit** delivers a ramp voltage during a given period according to the *Step* signal,
- the **comparator** indicates whether the ramp voltage has reached the predetermined reference voltage during the period,
- the **ramp rate control circuit** provides the adjustment signal to the generator according to the comparison result.

Such a corrective scheme uses two reference values, i.e. a clock signal to define the ramp period (*Step*) and the reference voltage (V_{ref}). The goal is to adjust the current source value of the ramp generator to a proper value so that the ramp voltage converges with the reference voltage within the given period. The proposed implementation of the ramp rate control circuit is based on the use of a very simple capacitive structure. The idea is to progressively accumulate on a capacitor the amount of charge required to drive the proper analog control voltage. Due to this progressive accumulation, the process of ramping and adjusting the control voltage has to be iterated a number of times to complete the system calibration. It is therefore an iterative adaptive scheme.

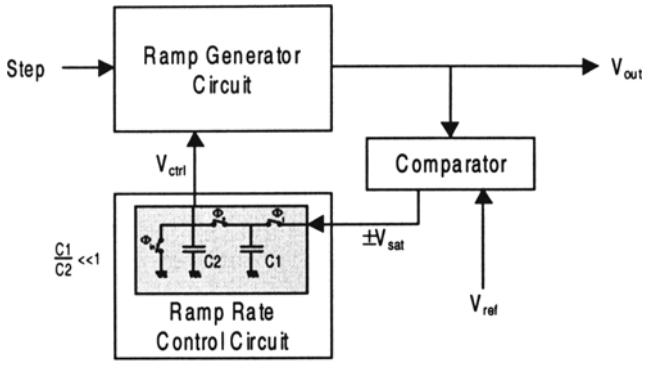


Figure 4. Implementation of the corrective scheme

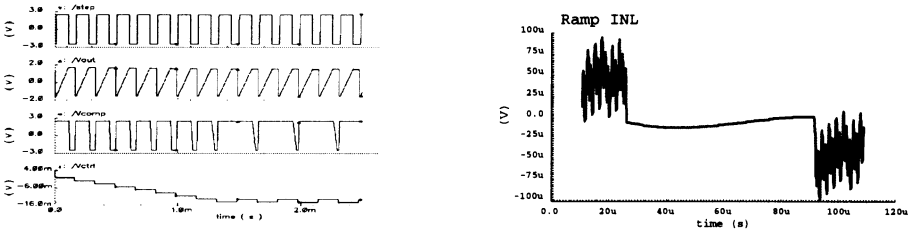
Figure 4 shows the implementation of this adaptive scheme. The feedback circuitry simply consists of a capacitor bridge controlled by the comparator output. At each iteration, we have an adjustment of the control voltage according to the comparison result. This adjustment is actually performed by the capacitor bridge in a two-phase operation, i.e. first pre-charge of capacitor C1 to either the positive or negative saturation voltage according to the comparison result, and then charge distribution between the 2 capacitors. The resulting output voltage is expressed as:

$$V_{ctrl}(i) \cong V_{ctrl}(i-1) \pm \Delta \qquad \left(\text{if } \frac{C1}{C2} << 1 \text{ and } \Delta = \frac{C1}{C2} \cdot V_{sat}\right)$$

As an illustration of the calibration procedure, we consider the case of a reduction of the ramp slope due to process variations. The calibration procedure starts with a number of cycles in which the control voltage is progressively augmented of Δ at each iteration, until the ramp voltage reaches the reference voltage within the given period. Then, the control voltage oscillates around the proper value in the following iterations, indicating that the calibration is completed. Once the system is calibrated, we can then use the generator to deliver a saw-tooth signal by continuously iterating the process of ramping without any intermediate calibration step. In this case, the *Step* signal is maintained at logic 1 and only the *Init* signal is used to initialize ramp generation at each cycle.

The calibrated saw-tooth generator has been implemented in a CMOS 0.6µm technology. In order to achieve high precision on the ramp calibration, we have to implement a very low capacitor ratio. For instance, the adjustment of the control voltage within 1mV requires a capacitor ratio of 4.10^{-4} (assuming a ±2.5V saturation voltage for the comparator). To ensure such a low capacitor ratio while maintaining a low area overhead, we suggest to use only the parasitic capacitors of the transmission gates operating as switches for *C1* and choose 10pF for *C2*.

The complete structure has been simulated to validate the calibration process. We can see on figure 5.a that the ramp voltage calibrates itself to the reference voltage in less than 10 cycles. Then, we have oscillations of the control voltage around -13mV with an amplitude less than 1mV. Measurements of the ramp slope once calibrated reveal an average slope error of 0.4%, which clearly demonstrates the effectiveness of the calibration scheme to correct the sensitivity of the ramp generator to process fluctuations.



a) simulation b) linearity

Figure 5. Simulation and linearity of the calibrated ramp generator

We also verify that the linearity of the ramp generator is not degraded by the additional circuitry. A detailed view of the calibrated ramp along with the corresponding INL is given in figure 5.b. We measure a maximum INL of 91μV, which translates in a linearity of 15 bits for the ramp voltage. This result is comparable to the linearity of the basic ramp generator, demonstrating that we have a very low impact of the additional circuitry on the linearity performance.

5. PERFORMANCES AND DISCUSSION

The previous section has detailed the calibration procedure of the saw-tooth generator. In particular, it has been shown that each single ramp of the saw-tooth generator ramp exhibits good linearity and slope precision once calibrated. In this section, we now use the calibrated saw-tooth generator as test stimulus generator for an ADC and we want to evaluate the quality of this test stimulus in the context linear histogram testing. More precisely, we want to demonstrate that the histogram built up collecting the samples on the ADC output corresponds to the histogram of a perfect converter.

The experimental setup is the following. We consider a perfect converter of 10-bit resolution, 3V full scale range and 50MHz clock rate. We want to perform the histogram test on this converter using 64261 samples collected at-speed.

The first step consists in defining the appropriate input stimulus amplitude and period to test this converter. Ideally, the input stimulus amplitude should corresponds to the full scale range of the converter. However in practice, an input signal slightly larger than full scale is usually applied to the circuit under test. This permits to ensure that all converter codes are fully exercised. In addition, this also permits to limit the effect of unavoidable non-linearity errors at the initialization of each ramp of the saw-tooth signal. So we choose $V_{init} = -1.6V$ and $V_{ref} = +1.6V$ so that the saw-tooth generator delivers a 3.2V amplitude signal once calibrated.

Then, we have to define the period of the input signal. We actually want to collect 64261 with a sampling frequency at 50MHz. In order to minimize test time, the coherent testing approach is usually adopt [16]. Indeed, coherent testing provides a means to gather information using the least number of samples. Basically the idea is that, given a number of samples, these samples can be distributed over a controlled interval in a way that is informationally equivalent to a uniform distribution over one signal period. The fundamental requirement for coherent testing is described by the equation:

$$\frac{F_{in}}{F_s} = \frac{M}{N}$$

with M and N relatively prime, where F_{in} is the input test frequency, F_s the sampling frequency, M the number of input test cycles and N the number of samples.

So according to this equation, we determine that the samples have to be collected on M=13 periods on the input test signal. Indeed, remember that the basic ramp generator is designed to deliver a ramp signal in the 3V amplitude range with a 0.1ms duration under typical mean conditions. The input test frequency consequently lies in the 10kHz range, implying 13 periods of the input signal to collect the 64261 samples. The test frequency is then selected according to the coherent testing requirement as $F_{in} = 10.111kHz$, corresponding to a signal period of 98.9µs. So we define the *Init* signal as a pulse at logic 1 each 98.9µs with a duration of 0.3µs, while the *Step* signal is maintained at logic 1 for the duration of the input test stimulus.

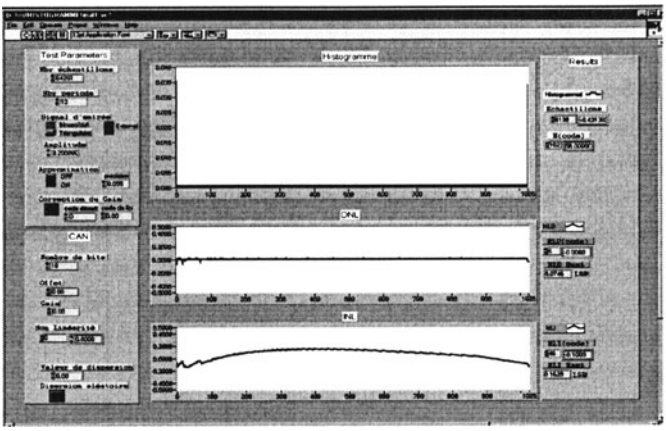


Figure 6. Experimental histogram test results

Finally, we apply 13 periods of the calibrated saw-tooth signal to the converter and we build up the corresponding histogram. From this histogram, we can now evaluate the DNL and INL of the converter. Experimental results are given in figure 6. The first graph corresponds to the measured histogram on the ADC output. As expected, this histogram appears perfectly flat with an equal code count for all codes (excepted the extreme ones because of the overloaded input signal). The second graph plots the DNL of the converter. The maximum measured DNL value is equal to 0.07 LSB. Such a low value is in agreement with the assumption of an ideal converter, taking into account that the finite number of samples used to built up the histogram introduces an inaccuracy in the parameter measurement. Finally, the last graph shows the INL of the converter. The maximum measured INL value is 0.16 LSB. At first glance, this value seems to be less performing than the DNL one. Nevertheless, it remains close to that obtained from an ideal converter. In any case, it remains under that usually derived from real converters.

Concerning the critical criterion of extra area the solution we propose is found to be highly performing. Indeed, the area of our generator is less than 0.05 mm. Which corresponds to an area overhead of 2 % when compared to a classical flash 6-bit ADC.

6. CONCLUSIONS

In the context of BIST for analog and mixed signal circuits, this paper presents an on-chip generator dedicated to the test of A-to-D Converters using a linear histogram approach. In order to fulfill reliable characterization of ADCs a very original adaptive scheme is proposed that ensures both high

linearity of the ramp and precise amplitude control while maintaining low silicon overhead. The basic principle of the generator consists in comparing the generated ramp voltage to a predetermined reference voltage and feeding back an adjustment signal so that the ramp voltage converges with the reference one. The effectiveness of the calibration is clearly demonstrated on an example where the ramp voltage calibrates itself to the reference voltage in less than 10 cycles with an average slope error of 0.4 %. We measured a maximum INL of 91 μV which translates in a linearity of 15 bits for the ramp signal. In addition, the implementation of the circuit requiring only about ten transistors, two capacitors and one comparator, exhibits an extremely small area.

7. REFERENCES

[1] M.J. Ohletz, "Hybrid Built-In Self-Test (HBIST) for Mixed Analogue/Digital Integrated Circuits", *Proc. European Test Conference*, pp. 307-316, 1991.

[2] N. Nagi, A. Chatterjee, J. Abraham, "A Signature Analyzer for Analog and Mixed-Signal Circuits", *Proc. ICCD*, pp.284-87, 1994.

[3] K. Damm, W. Anheier, "HBIST Of Nonlinear Analog Building Blocks In Mixed-Signal Circuits", *International Mixed Signal Testing Workshop*, pp.257-62, June 1995.

[4] E. Teraoca, T. Kengaku, I. Yasui, K. Ishikawa, T. Matsuo, "A Built–In Self–Test for ADC and DAC in a Single–Chip Speech CODEC", Proc. International Test Conference, pp. 791–796, 1993.

[5] M.F. Toner and G.W. Roberts, "A BIST Scheme for a SNR, Gain Tracking and Frequency Response Test of a Sigma–Delta ADC", *IEEE Trans. Circuits & Systems II*, Vol. 42, pp. 1–15, 1995.

[6] S Sunter, N. Nagi, "A Simplified Polynomial–Fitting Algorithm for DAC and ADC BIST", *Proc. International Test Conference*, pp. 389–395, 1997.

[7] K. Arabi, B. Kaminska, "Efficient and Accurate Testing of Analog–to–Digital Converters Using Oscillation–Test Method", *Proc. European Design & Test Conference*, pp. 348–352, 1997.

[8] R. de Vries, T. Zwemstra, E. Bruls, P. Regtien, "Built-In Self–Test Methodology for A/D Converters", *Proc. European Design & Test Conference* , pp. 353-358, 1997.

[9] M. Renovell, F. Azaïs. S. Bernard, Y. Bertrand, "Hardware Resource Minimization for a Histogram-based ADC BIST", *Proc. VLSI Test Symposium*, pp. 247-252, 2000.

[10] F. Azaïs, S. Bernard, Y. Bertrand, M. Renovell, "Towards an ADC BIST Scheme using the Histogram Test Technique", *Proc. European Test Workshop*, pp. 53-58, 2000.

[11] X. Haurie, G.W. Roberts, "Arbitrary-Precision Signal Generation for Bandlimited Mixed-Signal Testing", *Proc. International Test Conference*, pp.78-86, 1995.

[12] A.K. Lu, G.W. Roberts, "An Analog Multi-Tone Signal Generator for Built-In Self-Test Applications", *Proc. International Test Conference*, pp. 650-659, 1994.

[13] G.W. Roberts, A.K. Lu, "Analog Signal Generation for Built-In Self-Test of Mixed-Signal Integrated Circuits", *Kluwer Academic Publishers*, ISBN 0-7923-9564-6, 1995.

[14] B. Provost, E. Sanchez-Sinencio, "Auto-Calibrating Analog Timer for On-Chip Testing", *Proc. International Test Conference*, 1999.

[15] F. Azaïs, S. Bernard, Y. Bertrand, X. Michel, M. Renovell "A Low-Cost Adaptive Ramp Generator for Analog BIST Applications", *Proc. VLSI Test Symposium*, 2001.

[16] M. Mahoney, "DSP–based Testing of Analog and Mixed–Signal Integrated Circuits", *IEEE Computer Society Press*, ISBN 0-8186-0785-8, 1987.