Interconnect Capacitance Modelling in a VDSM CMOS Technology

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Abstract: This paper introduces a set of analytical formulations for 3D modelling of inter- and intra-layer capacitance. Based on real silicon data, we have developed and validated efficient and accurate analytical models that are an helpful alternative to lookup tables or numerical simulations.

Key words: interconnects, capacitance, layout extraction, closed-form models.

1. INTRODUCTION

It is now well established that interconnects drastically affect performances of VLSI circuits [1-3]. Even if resistance must be taken into account, capacitance remain the most limiting factor. On the one hand, they affect the total load that must be driven by logical gates. Power consumption is then directly dependent to this capacitive load while propagation delays can only be deduced from the study of distributed RC networks. On the other hand, cross-talk evaluation requires the knowledge of node to node capacitive coupling. Finally, capacitance extraction from a layout must be investigated at different levels:

- at node level, only the total node capacitance is required to evaluate power consumption and delay for short nets,
- at node-to-node level, the mutual capacitance is required to compute cross-talk noise and elementary capacitance of RC networks.

It is then necessary and sufficient to extract node to node mutual capacitance. Even if CAD vendors are proposing several alternatives, this

[1] currently with Atmel, Rousset, France.

The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: 10.1007/978-0-387-35597-9_40

problem is traditionally solved using an open tool (e.g. dracula, diva, ...) together with public domain models (like in [4]). The limitations of those models on realistic test patterns, i.e. patterns with dimensions in the range of the minimum feature size, has been pointed out by the authors in 1995 [5]. In this paper, we are proposing a new set of formulas that have been validated in a 0.25 µm CMOS technology.

In the first section of the paper we discuss previously published models and we select the most complete ones for the purpose of accuracy comparison. After a brief description of the used methodology, the model is extensively presented and discussed in terms of accuracy and efficiency.

2. STATE OF THE ART

Numerous analytical models have been published since interconnect capacitance are extracted from a layout. Some of them have been validated in rather old technologies with minimum feature dimensions largely over one micrometer: they only address the capacitance of a metal wire with respect to a plane. Only models proposed during the last fifteen years are mentioned in this study. They are generally based on formulations validated against numerical simulations or large silicon test patterns. They often exhibit a lack in accuracy owing to several assumptions on process such as the shape of conductors or planarity. Moreover, these formulations often require a reference plane to compute capacitance with a good accuracy. In the following, we have studied and evaluated models found in the literature according to three different configurations: i) inter-layer coupling with overlap, ii) inter-layer coupling without overlap and iii) intra-layer coupling.

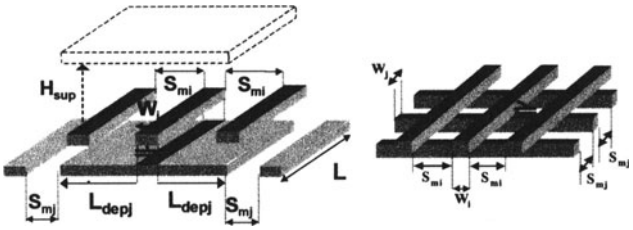


Figure 1. Reference test patterns for inter-layer capacitance with overlap.

Previously proposed models for inter-layer capacitance [6-9] have been evaluated for both 2D and 3D effects according to reference test patterns (Fig. 1). Left-side pattern exhibits only easy-to-model bi-dimensional effects. Chern's model [7] is the only one that takes into account 3D effects (e.g. right side pattern). As accuracy is comparable with other models for 2D

effects we select this model as a reference to evaluate our formulas together with the standard model (deduced from [4]).

Capacitance between two non-overlapping conductors at different interconnect layers has been neglected for years. Arora recently address this phenomenon [8].

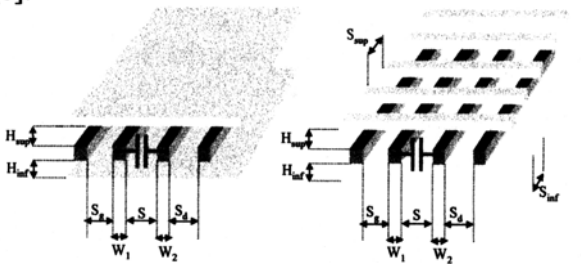


Figure 2. Reference test patterns for intra-layer capacitance.

Concerning Intra-layer couplings, published models [6-10] have been evaluated against test patterns (Fig. 2). Extraction tools generally compute the capacitance using a 1/S model. A $1/S^2$ behaviour is also mentioned in [10]. Models presented by Chern [7] and Delorme [9] are the most complete and we will evaluate our model against them.

3. METHODOLOGY

The process of calibrating a capacitance extraction tool for a given technology is not currently standardised. Each EDA tool vendor is proposing his own methodology that can then be adapted with silicon foundries to their technology. However, several steps are common to most of the proposed methodologies:

- the use of a library of test patterns to identify the behaviour of capacitive couplings with respect to design parameters,
- a 3D finite element simulation engine to calculate accurately each of the reference test pattern,
- the use of analytical or numerical models to speed up the extraction process at the full-chip level.

Our methodology includes the use of on-chip capacitance measurement to obtain numerous silicon data on small silicon test patterns at a reduced silicon cost [11]. It is worth noting that due to their small dimensions, these test patterns allow the identification of small dimension effects. Using these data jointly with technology dependent information, it is then possible to calibrate a numerical simulator. In our case, we have used a 2D finite element simulator that matches silicon data within 5% with a standard deviation of about 2%. A nearly infinite number of test patterns can then be

deduced to study the behaviour of the capacitance with respect to design parameters. To validate our models, we have defined two estimators corresponding respectively to the standard deviation (overall accuracy) and to the maximum deviation (robustness) between data and modelled values.

Our approach consists in the physical decomposition of the total capacitance between two conductors: like in the so-called standard model the mutual coupling is split into physically based elementary effects. Such a decomposition has already demonstrated its efficiency for a 0.8 µm CMOS technology [12].

4. INTER-LAYER CAPACITANCE MODELLING

In this section, we are presenting our model for inter-layer capacitance. The case of two isolated lines is first addressed. We then discuss the impact of lateral environment on the side-wall contribution. Vertical screening and 3D effects are also dealt with. Finally, we describe a practical implementation for layout extraction.

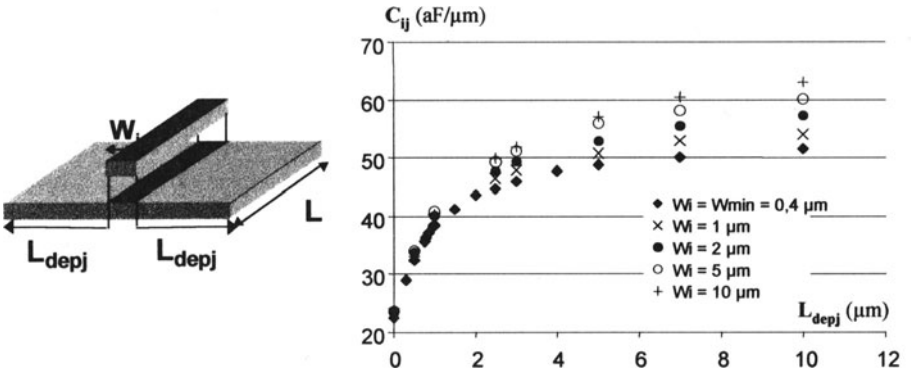


Figure 3. Left side: test pattern for characterisation of $C_{ij}(L_{depj})$.
Rigth side: side-wall capacitance versus W_i and L_{depj}.

4.1 Two isolated lines

Concerning the simple case of two isolated lines, the first test pattern that can be identified concern two conductors that are geometrically identical and perfectly stacked. Capacitance per area unit (C_s) and side-wall capacitance per perimeter unit (C_{sw}) are then constant parameters already defined in the standard model. In the general case, where both conductors are not perfectly stacked it is necessary to relate the side-wall capacitance with the distance in which a conductor projects beyond the other (Fig. 3). More than fifty

different patterns have been defined respectively to both design parameters W_i (from 0.4 up to 10 µm) and L_{depj} (from 0 up to 10 µm).

On the one hand we have identified the dependence of the side-wall capacitance with both design parameters (Fig. 3). This effect is particularly important for the higher value of L_{depj}.

	W_i=0.4 µm						
	Data	LIRMM		Standard		Chern	
L_{depj} (µm)	C_{total} aF/µm	C_{total} aF/µm	Error	C_{total} aF/µm	Error	C_{total} aF/µm	Error
0.5	85.2	85.8	0.7%		44.4%		55.7%
1	97.0	96.4	0.6%		26.8%		36.7%
2.5	109.3	110	0.6%		12.5%		21.3%
3	111.9	112.3	0.4%	123	10.0%	132.6	18.5%
5	117.6	117.5	0.1%		4.6%		12.7%
7	120.4	120.1	0.3%		2.2%		10.1%
10	123.0	122.2	0.7%		0.0%		7.8%
	W_i=10 µm						
	Data	LIRMM		Standard		Chern	
L_{depj} (µm)	C_{total} aF/µm	C_{total} aF/µm	Error	C_{total} aF/µm	Error	C_{total} aF/µm	Error
0.5	571.3	570.5	0.1%		6.4%		5.0%
1	585.6	581.1	0.8%		3.8%		2.4%
2.5	604.5	594.7	1.6%		0.5%		0.8%
3	608.7	597.0	2.8%	607.7	0.2%	599.6	1.5%
5	618.9	602.2	2.7%		1.8%		3.1%
7	625.8	604.8	3.4%		2.9%		4.2%
10	630.9	606.9	3.8%		3.7%		5.0%

Table 1. Accuracy comparison for modelling two isolated lines.

On the other hand, it is also obvious that when the width of the narrower line increases, the surface capacitance increases much more quickly than the side-wall capacitance. As a consequence the effect of neglecting the dependence of the side-wall capacitance with the conductor width should not impact significantly the total mutual capacitance. The proposed model for the side-wall capacitance is then a simple function of L_{depj} that writes:

$$C_{ij}(L_{depj}) = C_0 + \left(C_{ijmax} - C_0\right) \cdot e^{\left(\frac{-A_{ij}}{A_{ij}+L_{depj}}\right)} \quad (1)$$

where C_{ijmax} and A_{ij} are a pair of parameters with a physical meaning and not only fitting parameters. C_{ijmax} is an asymptotic value representing the maximum side-wall capacitance when L_{depj} increases up to an infinite value. A_{ij} represents a distance that traduces the "speed" of variation between the minimum value of the side-wall capacitance (C_{SW} defined with two stacked conductors) and C_{ijmax}. This parameter is calculated to optimise the average error on a few number of test patterns. Finally, C_0 is calculated as $C_0=(C_{sw}-C_{ijmax}.e^{-1})/(1-e^{-1})$. It is worth noting that the physical origin of all parameters makes $C_{ij}(L_{depj})$ robust and reliable: whatever the value of L_{depj} is, the boundaries of $C_{ij}(L_{depj})$ are guaranteed.

Partial results are given in Table 1 for several version of the test pattern illustrated at Figure 3. It is clearly demonstrated that both standard and Chern's model that are not taking into account L_{depj} are very inaccurate especially when the conductor width is small, *i.e.* when the side-wall capacitance represents up to 80 % of the total capacitance. The same model has been also validated for the symmetrical test pattern where the upper layer projects beyond the lower level. Finally, on a set of seventy test patterns covering all significant dimensions that can be encountered in a layout, errors have been computed for each selected model (table 2).

Error	LIRMM	Standard	Chern
Average	2.2 %	10 %	18 %
Maximal	5.7 %	57 %	72 %

Table 2. Accuracy comparison for inter-layer capacitance between two isolated conductors.

4.2 Influence of lateral screening

We have first studied the impact of the presence of conductors in the neighbourhood of two stacked conductors. The total mutual capacitance is defined between the two stacked conductors while lateral lines are grounded and separated from the middle conductor by S_{mi} (Fig. 4). In a 0.25 µm CMOS technology, this distance may range down to 0.6 µm. There is no maximal value, in this case we obtain the behaviour of two isolated conductors. The side-wall capacitance of two stacked conductors can then be defined as a function of the spacing S_{mi} between the lateral shields and the middle conductor (Fig. 4). Similar behaviour has been obtained for lateral screens placed at the bottom layer. It clearly appears that lateral screens are introducing an attenuation coefficient that should be multiplied to the value of the side-wall capacitance obtained for two isolated stacked lines. However, in the realistic case, screens are present at both top and bottom levels, the total attenuation will be too important if both coefficient are simply multiplied.

This discussion leads to add an amplification coefficient that will be used to amplify the side-wall capacitance in the presence of double lateral screens. Finally, it comes:

$$C_{sw}(s_{mi}, s_{mj}) = C_{sw} \cdot e^{-\left(\frac{s_{ij}}{s_{mi}}\right)} \cdot e^{-\left(\frac{s_{ji}}{s_{mj}}\right)} \cdot e^{\left(\frac{k}{s_{mi}+s_{mj}}\right)} \qquad (2)$$

where S_{ij}, S_{ji} and k are fitting parameters with a physical meaning that traduces the sensitivity (previously called "speed") of the side-wall capacitance to screen proximity. S_{ij} is first extracted to optimise the error on a set of stacked conductors with lateral screens at the top level. Then S_{ji} is

calculated for the best fit on test patterns with lateral screens at the bottom level only. Finally, k is determined when screens are present at both top and bottom levels. It is worth noting that the proposed model can be applied to calculate the side-wall capacitance of two stacked conductors whatever the screening conditions are. Obtained accuracy is reported in table 3.

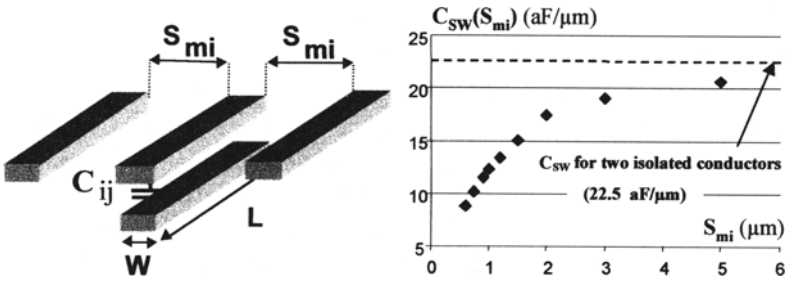


Figure 4. Left side: test pattern for lateral screening evidence. Right side: impact of screening lateral lines on the side-wall capacitance of two stacked conductors.

Error	LIRMM	Standard	Chern
Average	2.1 %	50 %	42 %
Maximal	5.6 %	120 %	71 %

Table 3. Accuracy of studied models on 36 patterns of stacked conductors with lateral screens.

We then extend the previous model to the case of a conductor that projects beyond the other. The same principle has been applied to reach a general formulation for the previously proposed C_{ij} and C_{ji}:

$$C_{ij}(L_{depj}, s_{mi}, s_{mj}) = C_{ij}(L_{depj}) \cdot e^{\left(\frac{-s_{ij}}{s_{mi}}\right)} \cdot e^{\left(\frac{-s_{ji}}{L_{depj}+s_{mj}}\right)} \cdot e^{\left(\frac{k}{s_{mi}+L_{depj}+s_{mj}}\right)}$$

$$C_{ji}(L_{depi}, s_{mi}, s_{mj}) = C_{ji}(L_{depi}) \cdot e^{\left(\frac{-s_{ij}}{L_{depi}+s_{mi}}\right)} \cdot e^{\left(\frac{-s_{ji}}{s_{mj}}\right)} \cdot e^{\left(\frac{k}{L_{depi}+s_{mi}+s_{mj}}\right)} \quad (3)$$

These equations have been validated on more than 300 test patterns with a correct accuracy (Table 4). From previously presented tables, our model always exhibits a better accuracy than the two reference models selected for comparison.

Error	LIRMM	Standard	Chern
Average	6.4 %	63 %	16 %
Maximal	13.6 %	205 %	92 %

Table 4. Accuracy of the studied models for inter-layer capacitance with lateral screens.

4.3 Management of vertical profiles

Results presented until now concern the coupling between two conductors from met3 and met4 layers. As no other layers have been used, bottom plane corresponds to substrate and there is no top plane. In the addressed technology, twelve different vertical environments can be defined for the pair met3 and met4. This corresponds to all possible combination of 4 different bottom planes (substrate, polysilicon, metl or met2) with three different top planes (met5, met6 and none). To represent the impact of the vertical profile, we choose a look-up table approach: in high density layouts, a lot of "possible" vertical profiles are not realistic. As a consequence analytical modelling of vertical profile impact is not required. For each vertical profile that must be covered, a complete set of coefficients must be calculated. We then verify that the proposed model applies whatever the vertical profile is.

Top plane	none	Met5
Bottom plane	substrate	Met2
C_s (aF/µm²)	50.49	49.8
C_{sw} (aF/µm)	22.5	14.33
C_{ijmax} (aF/µm)	53.8	33.36
C_{jimax} (aF/µm)	43.72	32.55
A_{ij} (µm)	0.616	0.304
A_{ji} (µm)	0.326	0.293
s_{ij} (µm)	0.574	0.453
s_{ji} (µm)	0.542	0.442
k (µm)	0.46	0.764
Average error	5 %	7.4 %
Maximal error	13.6 %	14.8 %

Table 5. Accuracy of the proposed model for inter-layer capacitance for two vertical profiles (2D effects).

Table 5 illustrates two "extreme" cases: i.e. the low density one and the higher density one where each met3-met4 pattern is delimited by two metal planes in met2 and met5. More than five hundred test patterns have been characterised and modelled for each vertical profiles and a similar accuracy has been obtained for all of them.

4.4 Modelling of 3D effects

3D effects have been pointed out by the authors in the middle of the 90th [5]. A typical test pattern to address 3D effects is illustrated on the right-hand side of Figure 1. Assuming that most of the 2D effects are still present we only added a new term to the 2D model that represents the contribution

of all non overlapping regions of the two central lines. We called this effect the corner effect and the component C_c, which depends on the vicinity of neighbouring lines, is expressed as follows:

$$C_c(s_{mi}, s_{mj}) = C_{cmin} + (C_{cmax} - C_{cmin}) \cdot \exp^{-\left(\frac{c_{ij}}{s_{mi}} + \frac{c_{ji}}{s_{mj}}\right)} \quad (4)$$

where C_{cmax} and C_{cmin} represent respectively the maximum (no neighbours) and minimum (closest neighbours) values of the offset due to one elementary corner. c_{ij} and c_{ji} are then determined to fit the variation of the corner effect for various separation between central lines and lateral lines. Validated against nine silicon test patterns, the proposed model leads to a maximal error of 9 % and an average error of 6 %.

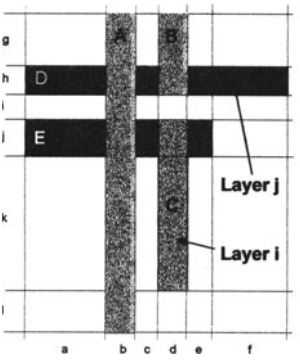


Figure 5. Practical implementation of the proposed model for layout extraction.

4.5 Extraction procedure

This sub-section summarises a practical implementation of the proposed model. The layout represented at Figure 5 is composed of three metal conductors in the vertical routing direction (labelled A, B and C) and two metal conductors in the horizontal routing direction (labelled D and E). The calculated capacitance is the total capacitance between conductor E and conductor C that can be split in 7 independent terms: i) the surface capacitance, ii) four side-wall terms differing in lateral screen configuration and with different projection distance, iii) two corner effects. Finally, the total capacitance writes:

$$C_{EC} = C_s \cdot (d \cdot j) + C_{sw}(s_{mi} = i, s_{mj} = i) \cdot d + C_{ij}(L_{depj} = e, s_{mi} = \infty, s_{mj} = \infty) \cdot j$$
$$+ C_{ij}(L_{depj} = (a+b+c), s_{mi} = c, s_{mj} = \infty) \cdot j + C_{ji}(L_{depi} = k, s_{mi} = \infty, s_{mj} = \infty) \cdot d$$
$$+ C_c(s_{mi} = \infty, s_{mj} = \infty) + C_c(s_{mi} = c, s_{mj} = \infty)$$

5. INTRA-LAYER CAPACITANCE MODELLING

We first address the capacitance between two isolated conductors at the same level. To identify each phenomenon independently, we initially used a calibrated 2D numerical simulator to obtain data without any vertical grounded plane (even the substrate was omitted). Two design parameters can then be identified, the conductor width and the spacing between them.

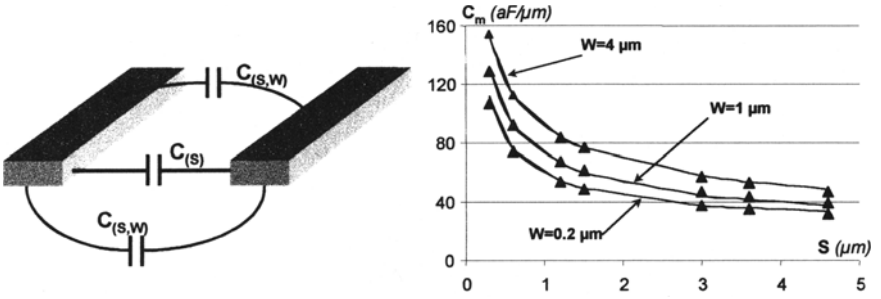


Figure 6. Left side: elementary test pattern for intra-layer capacitance. Right side: characterised *vs* modelled data for intra-layer capacitance in a 0.12 µm technology.

We have then identified two elementary contributions. One owing to the faced-sides relates to the spacing between conductors. The second owing to both top and bottom sides of the conductors is also a function of conductor width. Finally, the mutual capacitance between two isolated conductors has been validated as $C_m(S,W) = 2 \cdot C(S,W) + C(S)$ with:

$$C(S,W) = C_0 \cdot \ln\left(\frac{S+2W}{S}\right) \text{ and } C(S) = \frac{C_1}{\ln\left(\frac{S+k_0}{k_0}\right)} \quad (5)$$

where C_0, C_1 and k_0 are three constant parameters for a given technology and a given metal layer. C_1 and k_0 are both strongly dependent to the thickness of the conductors. The proposed model has been validated against numerical simulations for technologies down to 0.12 µm (Fig. 6). Discrepancies between simulated and modelled data are always below 5%. It is worth noting that our model can be used for different dielectric constants of insulating materials by changing the coefficients. In order to introduce the effect of vertical environment, we first modelled the case of two isolated conductors in presence of a substrate. From both silicon and simulation data, it appears that previously determined terms are still present but attenuated by a grounded plane. Finally, the following generalised model comes:

$$C_m(S,W) = C(S) \cdot e^{-k_S \cdot S} + 2 \cdot C(S,W) \cdot e^{-k_{SW} \cdot S} \quad (6)$$

where k_S and k_{SW} are constant parameters that depend on the vertical profile. C(S) and C(S,W) correspond to previously defined equations where C_0 and

C_1 depend on the vertical profile. Finally, only k_0 appears to be constant for a given interconnect thickness. The proposed model has been validated for all possible vertical profiles. Table 6 reports obtained accuracy for two conductors over a substrate. 76 test patterns have been defined for different line width (0.4µm up to 6 µm) and different spacing (0.6 µm up to 6 µm).

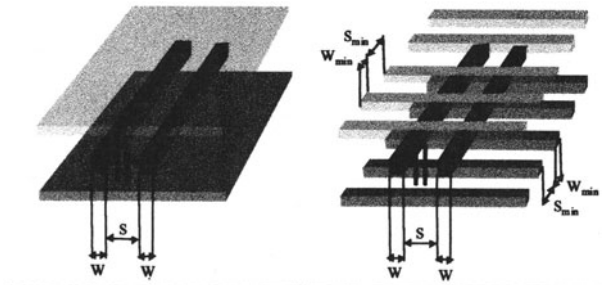
Error	LIRMM	Standard	Delorme	Chern
Average	1.5 %	28 %	8.3 %	5.7 %
Maximal	7.5 %	61 %	17.6 %	15.3 %

Table 6. Accuracy of the studied models for intra-layer capacitance of two met3 conductors over a subtrate.

We have then defined a set of 24 test patterns with two met3 conductors surrounded by two planes in met2 and met4 layers. As capacitance are very low, relative errors can be very important. For this reason, we are only reporting, for each evaluated model, the number of patterns that permits an error lower than the maximal error encountered with our model (Table 7).

Error	LIRMM	Standard	Delorme	Chern
Average	8.3 %	0 / 24	1 / 24	8 / 24
Maximal	13.2 %			

Table 7. Accuracy of the studied models for intra-layer capacitance in high density designs.



0,4	0,6	3,53	0,4	0,6	3,71
1	1,5	0,99	1	1,5	1,11
2	3	0,13	2	3	0,15

Figure 7. Screening effect of a plane versus a minimum pitch network of conductors.

The complete model [13] also includes the effect of non-symmetrical patterns and the effect of lateral screens through an attenuation factor. Finally, we addressed 3D effects. These effects are present when studying vertical screens. We have identified that a network of conductors routed at the minimum pitch are inducing nearly the same attenuation than a plane (Fig. 7).

6. CONCLUSIONS

In this paper we have introduced a set of analytical models for interconnect capacitance extraction in VLSI circuits. These models have been validated in a 0.25 µm CMOS technology. Accuracy has been demonstrated to be within about 10 % of real silicon or 3D numerical simulation. Robustness of these models is guaranteed owing to the self-bounded behaviour of each term. These models are also efficient and it is rather trivial to tune them on a given technology using a minimum set of reference data (real silicon or 3D numerical simulations). The proposed models [13] are also complete as all phenomenon have been covered even if not presented in this paper (i.e. vertical screen due to arbitrarily routed networks on the intra-layer capacitance or modelling of the inter-layer capacitance of non-overlapping conductors).

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