# Integration of Robustness in the Design of a Cell

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## Abstract

*When exposed to an harsh environment in space, high atmosphere or even on earth, Integrated Circuits undergo soft errors. Among these events the most worrying is an electrical upset, so called Single Event Upset (SEU) evidenced in latches. We present here the circuit architecture of a new SEU hardened latch. The hardening is based on an integrated redundancy of the information and a high impedance state switching. The design prevents perturbation to propagate inside the latch and saves an uncorrupted information source for recovery mechanisms. Post layout circuit simulations are used to verify the hardness assurance of this design; we also compare it to usual techniques and report significant improvements for its use in SoC.*

## 1. Introduction

Integrated Circuits ( ICs ) are adversely affected by environment [1]. Two main kinds of effects occur : the Total Ionizing Dose effects ( TID ) due to charge trapping in oxides which can cause threshold voltage shift and current leakage and the Single Event Effects ( SEE ) induced by a single ionized particle hitting on a sensitive area. Among these effects, the Single Event Latch-Up ( SEL ) and the Single Event Upset ( SEU ) are the most significant. The SEL is a destructive effect through the activation of a parasitic thyristor while the SEU results in a flipping of the information bits stored by latches. The SEL problem has now its solutions. We will here address on SEU effects. SEU originates many soft errors in ICs operating in space or high atmosphere as previously reported in [2-4], but also at ground level in terrestrial computer electronics as evidenced by IBM [1] or Normand [5]. The consequences of this effect are enhanced by scaling and the emergence of blocks embedded in System-on-Chip (SoC), difficult to test. As a consequence the robustness of functional blocks is becoming a prior concern in integrated architectures, making of circuit hardening to the environmental constraints a new challenge.

Our approach puts aside special technological solutions. It consists in the implementation of rad-hard designs at the circuit level using available commercial technology. The process is unvaried but the design solutions are easily transferable.

In the following, we shall first examine the phenomenon originating the upset and its consequence on the data latch. Then the new tolerant structure is presented with the principles involved in hardening and its efficiency is evidenced. We conclude by a comparison using an equivalent redundant structure to analyze the performances as far as speed and area are concerned.

## 2. SEU effects on data latches

### 2.1. Upset phenomenon at transistor level

We will first briefly describe the Single Event Upset mechanisms and present the way to simulate its effects on CMOS. More details will be found in [6-8].

Three basic concepts explain SEU : energy loss, charge collection and transient upset. When an energetic ion passes through any material it loses energy through interaction with the semiconductor bound electrons. It creates a dense track of hole-electron pairs, which may recombine with no effect. But in the presence of electric fields, typically in reverse biased P-N junction, electrons and holes are drifted in opposite directions and collected at device junctions. The main consequence is a transient current pulse. Such an upset drives the drain voltage of PMOS or NMOS respectively to the high or low level. Thus, ICs performed with CMOS technology, have several sensitive areas localized under contact diffusions. It is necessary to check off all the SEU sensitive areas to predict SEU effects. Moreover the electric field dependence implies a variation of their location according to the logic state of the node. Summarizing, a voltage difference on a junction induces an electric field and so a sensitive area. In case of a hit on this area, contact voltage is driven to the corresponding substrate voltage ( high voltage for PMOS or low voltage for NMOS).

The physical evolution of this phenomenon is relatively complex, yet electrical simulations of the upset can be done in a simple way with a pulse current source located at the sensitive node giving a good representation of the SEU effects observed on ICs [7]. The current pulse is fixed at a 10 mA amplitude, 50 ps rise and fall

times and a programmable duration to represent worst case conditions. Usually designers consider an upset duration between two or three hundred picoseconds.

Fortunately one another point is the random of the phenomenon joined to a low occurrence of the hits. So, we shall assume that just one upset (a single event upset) can happen at the time on the same sensitive area, excluding the case of multiple upsets.

These rules are used to identify and simulate the SEU sensitivity of a data latch in the next section.

### 2.2. Data latches and SEU

SEU effects on latches is a classical issue. The concern is the sensitivity of a standard data latch circuit to identify its level of vulnerability. This level is high.

If we consider a standard latch in static mode ( H=0, Hb=1 ), the Fig. 1 evidences the cell sensitive areas, state 1 corresponding to Q=G=1 and Qb=0 and state 0 to Q=G=0 and Qb=1. The sensitivity of the latch is characterized by logic state dependence.

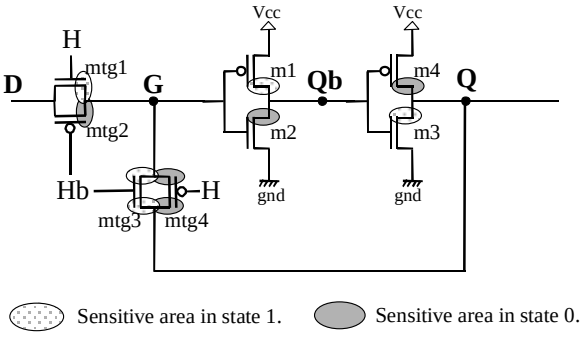



**Figure 1. Latch design and its SEU sensitive areas**

Simulations show, as expected, this high level of SEU sensitivity for the nodes Q, Qb and G. Figure 2 illustrates the results on node Qb with a 0.25 µm CMOS process and a post layout description, including parasitic capacitance extraction. The SEU simulations are achieved with a 50 ps current upset on node Qb and a latch in the logic state 1.

The current upset drives node Qb voltage to high level, turning the second inverter output Q and as a consequence G to low level. Thus, Qb is forced to high level through the first inverter, even after the current pulse has ceased. Feedback dynamics of data latches provoke a permanent bit flip in case of a transient upset.

Regarding the huge amount of data cells of the majority of ICs, designers in charge of radiation hardness have to cope with the SEU issue. We propose in the next section a way to improve the tolerance to the upset by revising the cell design.

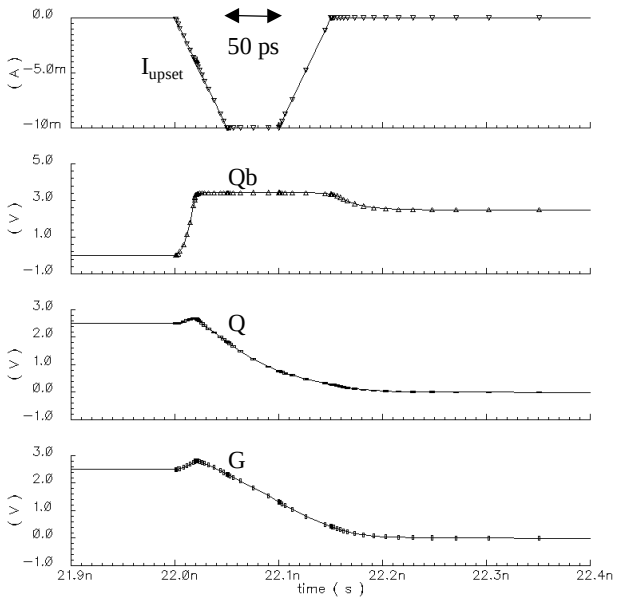



**Figure 2. Upset on node Qb**

## 3. The SEU hardened HZlatch

A few harden CMOS inverters and cells have been presented in the past few years [9-14]. Some are limited by their lack of robustness to the longest upsets, others present prohibitive areas. Our approach consists on providing SEU immunity by restructuring the data latch at the gate level.

### 3.1. The HZ inverter design

To attain SEU hardening assurance, we conceive a new inverter that we use to complete latches. This inverter is itself hardened against SEU through the use of two techniques: an information redundancy and a tristate double-output ( high impedance state gives the inverter name : HZ inverter ). Figure 3 details its design and Table 1 its truth table.

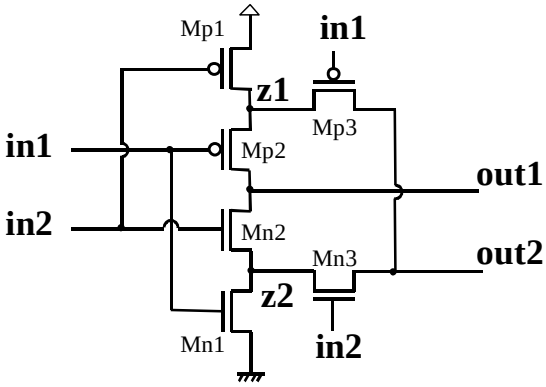



**Figure 3. HZ inverter design**

| In 1 | In 2 | Out 1 | Out 2 |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | HZ | HZ |
| 1 | 0 | HZ | HZ |
| 1 | 1 | 0 | 0 |

**Table 1. HZ inverter truth table**

When the two inputs ( In1 and In2 ) are settled in the same logic state the circuit works like an inverter, with outputs at the same logical level ( Out1=Out2 ) a complementary one of the inputs, as the truth table shows. Now, if an error occurs above in the IC and inverts the logic state of one of the inputs, the outputs are tristating ; thus their logic states remain uncorrupted and the error propagation is stopped.

We take advantage of these properties in the new proposed SEU hardened HZlatch.

### 3.2. The HZlatch design

The way we design the HZlatch is similar to any basic data latch design comprising two cross-coupled inverters. Figure 4 shows how to put together the basic cells. Two HZ inverters are used in conjunction with pass gates to avoid feedback during write operation.

Redundancy and high impedance state provide both static and dynamic SEU hardening by cutting error propagation due to the feedback. A SEU is said to be static when it arises during hold state and dynamic during write operation.

Considering that the hardened latch of figure 4 is in hold state ( H=1 and Hb=0 ) and stores data so that nodes Q1 and Q2 exhibit a low state. As a consequence data nodes Q3 and Q4 are established in a high state, and data nodes Q11 and Q22 are low. For example if a hit occurs at one of node Q1 sensitive area, Q1 momentarily goes high. Then the outputs of the first HZ inverter, Q3 and Q4, are tristated. Thus a source of uncorrupted data remains because Q3 and Q4 are still high. These nodes drive the second HZ inverter, which assigns low state to its outputs Q11 and Q22. A recovery mechanism of node Q1 through the cell feedback is provided, thereby hardening the latch against single particle induced upsets. Similar dynamics are at work to harden the latch when an opposite data state is initially stored and when upset occurs at any of its sensitive nodes.

Dynamic hardening mechanism is similar. After the latch stored the right data, the design prevents any false information to be rewritten. For example any error on D1 has the same effect than any upset on Q1 ( respectively on D2 and Q2). The sole limitation is appearing at high clock frequencies. In this case an upset could last long enough to prevent a new state to be written, by tristating the first HZ inverter outputs during the whole write cycle.

Next section reports SPICE simulations for the purpose to confirm this approach.

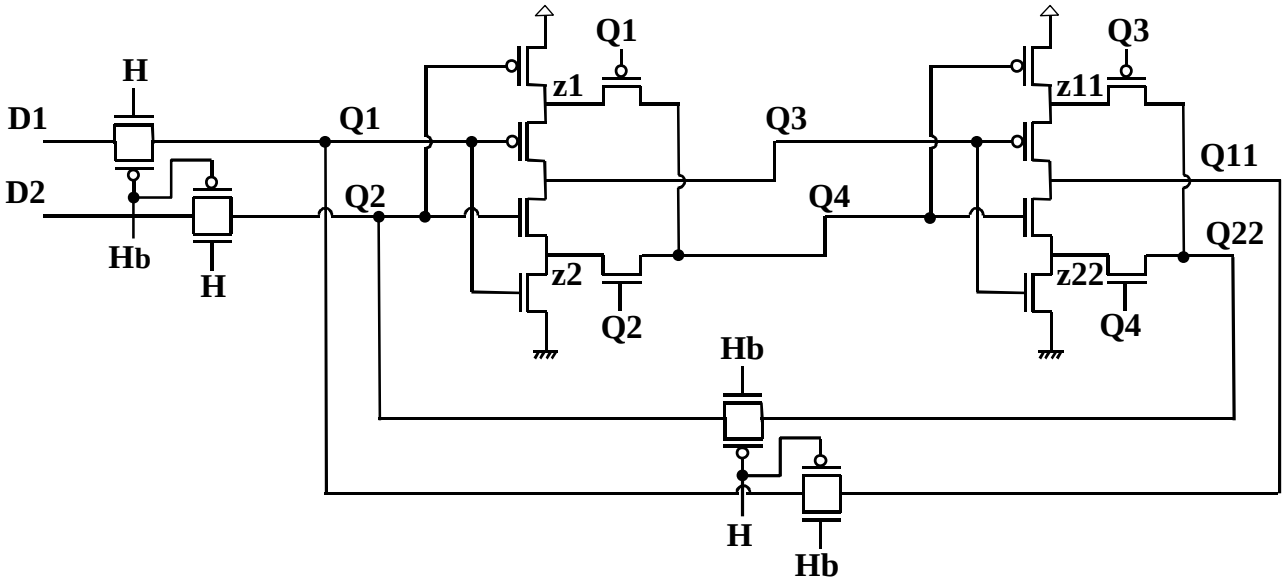



**Figure 4. HZlatch design**

### 3.3. HZlatch simulations

A layout of the HZlatch was completed using 0,25µm CMOS process ( see Fig. 5 ) and SPICE simulations were conducted after parasitic capacitance extraction.

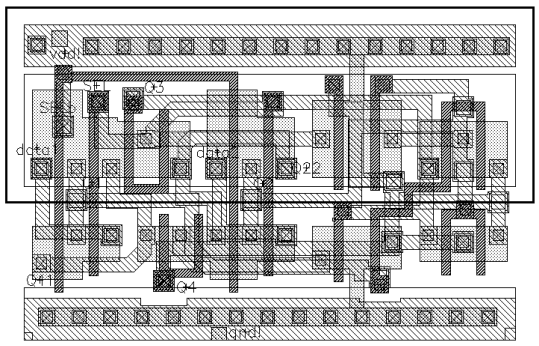



**Figure 5. HZlatch layout**

We report here response curves during upset on node Q1. The results are similar for the other nodes.

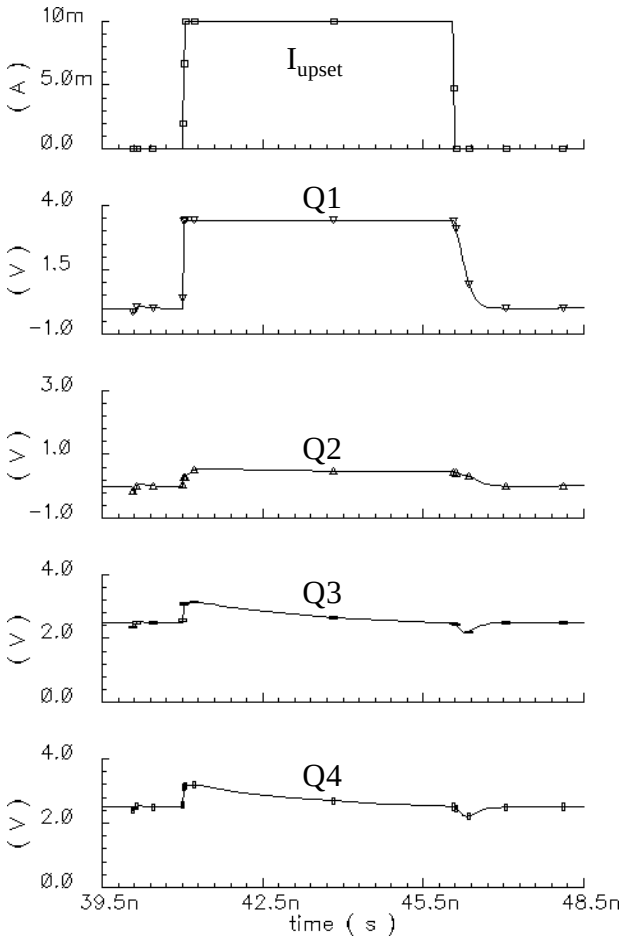



**Figure 6. Upset ( 10 mA, 5000 ps ) on node Q1**

The upset is simulated on node Q1, using a current pulse of 10 mA amplitude with a duration up to 5000 ps. the purpose is to force its voltage to high level. The extreme case is illustrated in Figure 6 and confirms the intervention of hardness mechanisms (part 3.2.)

Indeed node Q2 state is unchanged and due to high impedance effect nodes Q3 and Q4 hold on the high level; thus we verify that the low level of Q1 is restored as the upset current ceases, owing to recovery mechanism.

A simulation of the complementary upset on the same node Q1 ( see Fig. 7 ) confirms the hardness assurance.

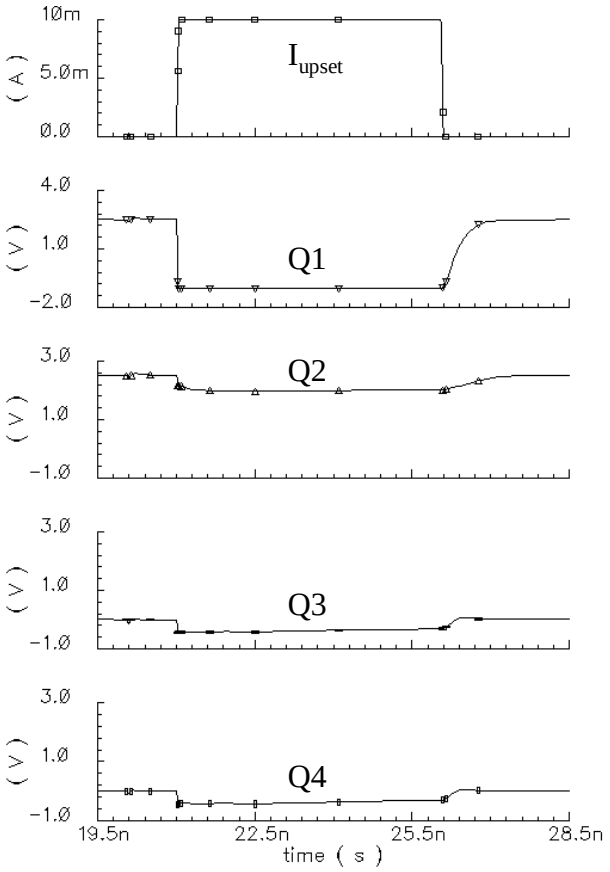



**Figure 7. Upset ( 10 mA, 5000 ps ) on node Q1**

Exhaustive simulations were run on all the HZlatch nodes for a 10 mA amplitude and 5000 ps duration current; in all cases the cell was not flipped. These upsets are longer than upset durations generally reported in scientific literature ( 1000 ps for the longest ) showing that HZ latch is safe even in utmost conditions.

## 4. Comparison with usual designs

In order to evaluate the performances in terms of area and speed, the HZlatch must now be compared with an equivalent tolerant architecture based on a standard latch circuit. A general method to achieve an hardness efficiency of systems is the use of a Triple Modular Redundancy ( TMR ). Figure 8 presents the structure used : three standard latches are connected in parallel to the clock and data inputs while their outputs feed a voting gate.

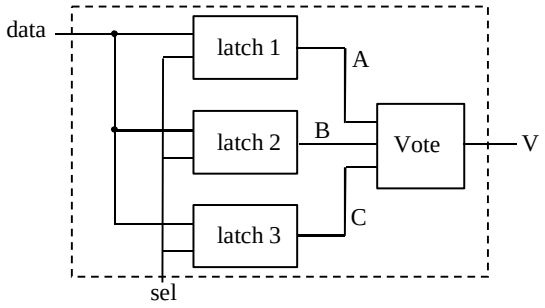
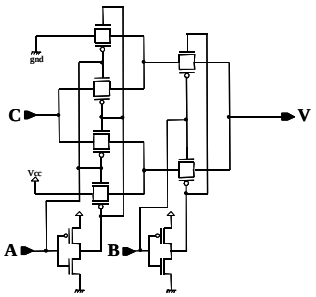



**Figure 8. Tripple Modular Redundancy Structure**

Any SEU arising in the latches will be corrected by the majority voting logic, implemented with a MUX structure as shown in Fig. 9.




| A | B | C | V |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**Figure 9. Majority vote module**

Such a design is not totally SEU proof. Indeed an upset at the voter level is always possible, even if it will be corrected rapidly when the upset ceases. Another problem may appear if the latches are not continuously clocked; in that case errors can "accumulate" in the TMR triplet ruining its functionality. This eventuality is not coming in sight with the HZ latch which is continuously correcting any upset.

Now we evaluate the worst delays to invert the data stored by the standard latch, the redundant circuit with propagation time through the voter and the HZ latch. These delays are estimated from mid-point of the inputs change to mid-point of the outputs voltage swing. The whole SPICE simulations are run with post layout extracted view of a 0.25 µm CMOS process. The simulation results are listed in Table 2 with the respective cell areas.

| | Delay ( ps ) | Area ( $\mu m^2$ ) |
|---|---|---|
| Std latch | 184 | 58.5 |
| Vote module | 238 | 110 |
| **Redundant circuit** | **500** | **285** |
| **HZlatch** | **455** | **126** |

**Table 2. Delay and area comparisons**

This comparison shows that to achieve a similar SEU hardness, the HZ latch presents a delay improvement of 10% and an area reduced by more than half compared to an equivalent TMR design. Besides the HZ latch has an improved reliability.

## 5. Conclusion

We have proposed a new data latch circuit ( the HZlatch ) devoted to work in an harsh environment by restructuring the design at the transistor level. The hardening method stops error propagation inside the cell by using high impedance state and provides an "integrated redundancy" in the shape of a recovery mechanism. The HZlatch can be advantageously compared to the full traditional TMR structure; this make the HZlatch a good candidate for its use in embedded systems like SoC with specific reliability constraints.

## 6. References

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