# Very Low Power High Temperature Stability Bandgap Reference Voltage

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## Abstract

*Due to the expansion of the portable applications and the battery operated products, great interest is given for design methodology for low consumption. When designing a process sensitive devices such as bandgap reference circuits (BGR), a perfect match between the simulation and the measurement on silicon have to be ensured. We present in this paper a very low current high temperature stability BiCMOS BGR design. A low current dedicated process characterization procedure is explained. The micro-power BGR design methodology is presented.*

## 1. Introduction

The design of process sensitive devices such as bandgap reference voltage circuits requires not only a perfect match between the simulation and the measurement but also an accurate modeling of the integration process. Thus the designer has to verify, in the process characterization step, the validity of the related model parameters. As the resolution of the data converter systems increases, the requirements for high accuracy, high temperature stability of BGR's have also increased. Designing a high stability circuit such as the bandgap reference imposes to obtain a very good correlation between the physical parameters and the model specification used in the electrical simulator. Characterizing these parameters for low voltage and current operating points over a wide range of temperature is out of the current foundry measurement protocols. At low operating bias conditions parasitic effects are exhausted, this greatly modifies the stability conditions at high temperature of critical designs such as that of bandgap reference. The temperature variation measured on samples of real bandgap reference voltage is given in Fig. 1 together with the simulation. It is obvious that the performance improvement of this circuit with such a simulation drift is an impossible task.

This paper demonstrates the feasibility of a very high temperature stability micro-power bandgap reference voltage. To reach this result we combine the design methodology resource together with process characterization, using a dedicated test structure organized around that of the final bandgap circuit. In the second section, the architecture of the bandgap circuit is presented. The temperature drift of the process is discussed in section 3. The new characterization procedure is developed in section 4. Section 5 is devoted to the micro-power bandgap design and the experimental validation.

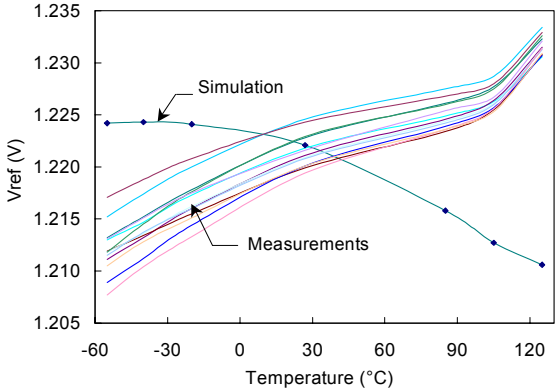



Figure 1. Comparison of the simulated and measured on Silicon Vref(T) characteristic.

## 2. Topology of the bandgap reference circuit test cell

Since introduced by Wildar [1], [2] the BGR has been used extensively to implement on-chip voltage references in A/D and D/A converters, voltage regulators and measurement systems. Several architectures have been proposed in the literature, but the most frequently used configuration is based on the Brokaw cell [3], illustrated in Fig. 2. In this schematic the bandgap reference $V_{REF}$ is obtained by combining the base emitter voltage of the transistor $Q_{IN}$ to the positive temperature coefficient voltage (PTAT), induced in the resistors $R_B$-$R_{B3}$ by the $\Delta V_{BE}$ of $Q_A$ and $Q_B$ and designed with a constant emitter area ratio *r*. The correction voltage $V_{PTAT}$ is obtained by amplifying the difference of the base-emitter voltages of $Q_A$ and $Q_B$ to compensate for at least the first order temperature dependence of $V_{BE}(T)$, noted $V_{CTAT}$(Complementary To Absolute Temperature Voltage). This can be written

$$\Delta V_{BEQA,QB} = \frac{kT}{q} \ln r \qquad (1)$$

where q is the electron charge, k the Boltzmann constant and T the absolute temperature. The resulting output voltage $V_{REF}(T)$ is obtained from

$$V_{ref}(T) = V_{CTAT}(T) + V_{PTAT} = V_{BE}(T) + A\Delta V_{BE}(T) \qquad (2)$$

in which $A$ is an amplification factor chosen to cancel the temperature coefficient of $V_{REF}$ at room temperature.

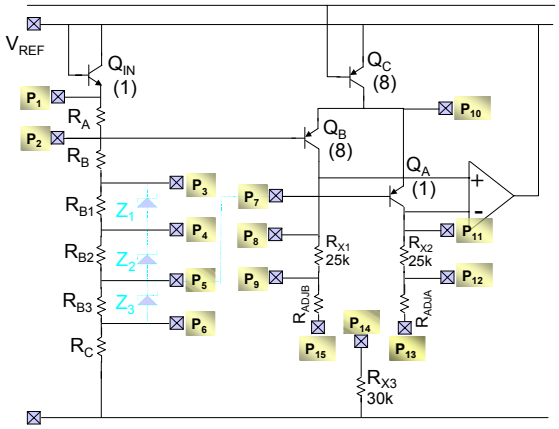



Figure 2. Brokaw cell based bandgap reference circuit

The main characteristic of this test cell is to allow the implementation of the internal access points P1 to P15. This will offer facilities on-chip characterization and modification of the structure configuration. This test cell is then used as a prototype in order to check the optimal operating point of the circuit that gives the best temperature coefficient. Zener diode based trimming devices are provided for the final device in order to cancel the process spread and the expected after packaging offset. The circuit has been implemented with 0.7µm BiCMOS process and 2.2µm×2.2µm emitter area, using P-implanted type resistors. It has been designed to fit the following specifications: ICC=40µA to 10mA with a Vref=1.225V at 27°C, 1% accuracy. The photomicrograph of the circuit is illustrated Fig. 3.

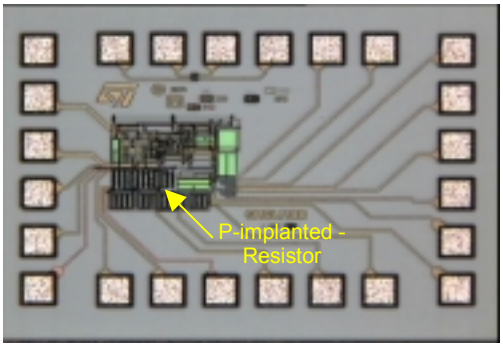
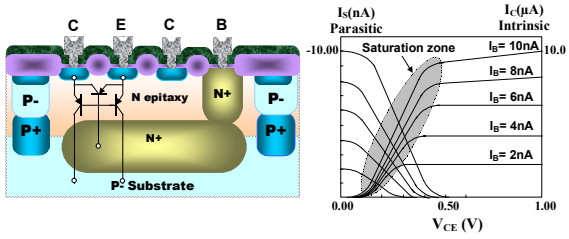



Figure 3. Photomicrograph of the configurable bandgap reference test cell with the R P-implanted

## 3. Temperature drift

Due to economical constraints, the considered process uses a p+ isolation strategy as illustrated in Fig. 4a. Despite the arrival of new isolation techniques, like oxyde isolation or trench isolation, the junction isolation is still currently used, due to its process simplicity and its very good manufacturing yield. The disadvantage of this solution is the presence of associated parasitic BJTs, that conduct a leakage substrate current when the intrinsic BJT works at the saturation region (Fig. 4b). In order to increase the battery efficiency and longevity in mobile applications, low voltage and low quiescent current are required. The low voltage operation is also a consequence of process. This is because the isolation barrier decreases as the component density per unit area increases, resulting in lower breakdown voltages [4-5].

Unfortunately, low reference voltage implies low $V_{CE}$ operating conditions. To generate the PTAT voltage, $Q_A$ and $Q_B$ have to be biased at the same collector current while their emitter area must be different. Therefore, they don't operate at the same saturation level. The corresponding substrate leakage current is then different and induces a second order component on the PTAT voltage. The non-ideality effects are amplified by the resistor ratio that is typically $A=10$, emphasized by the amplifier offset. This results in a dramatic rise in the $V_{ref}(T)$ value. These effects are not considered in the simulations based on the standard model card, which currently characterized between 1mA-10mA.




*(a)* *(b)*

Figure 4. Section view of BJTs implemented with a BiCMOS process

## 4. New characterization procedure

In the industrial context, the same model card is used to simulate several types of circuits that not necessarily operate at the same bias level. Typically, the standard model card is characterized at 1mA-10mA. However, the bandgap circuits operate at 1µA per branch under 1.225V. At this bias level, most of the BJTs work in the saturation domain, the parasitic effects are no more negligible and have to be considered. The corresponding parameters have then to be extracted with a specific strategy, at the circuit working conditions, using the test cell shown in Fig. 2. The structure of this test cell must permit the extraction of the parameters at the actual circuit operating conditions. In this way, the extracted

parameters are obtained under the real operating conditions in terms of bias, temperature, but also packaging induced mechanical stress. Firstly, the standard characterization at the nominal current is considered. The parameter determination consists in a "global fit" on the measured characteristic sets using the SILVACO's UTMOST tool [6]. Secondly, a low current characterization is performed using, as initial value, the set of previous parameters. The parameter extraction at low $V_{CE}$ is realized in order to obtain the best accuracy in the saturation mode. Finally, using the bandgap test cell, biased at 50µA, the more sensitive parameters such as the saturation current $I_S$, the current gain $\beta_F$ of the intrinsic and the parasitic BJTs, and the temperature related parameters $I_C(V_{BE})$ relationship, such as $E_G$ and $X_{TI}$, can be calibrated. These last parameters are of special importance for the bandgap reference voltage and vary dramatically with the $V_{BE}(T)$ slope. Thus, their determination needs a particular strategy that takes into consideration the real operating conditions of the components on the chip. The Meijer method, based on an analytical calculation [7] is used to extract correctly these parameters. The flow diagram of the characterization protocol is shown in Fig. 5.

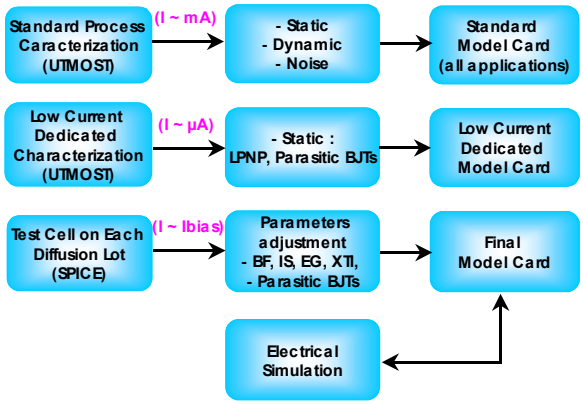



Figure 5. Characterization protocol flow diagram.

The list of the resulting main parameters, determined on the test cell, is given in the Table 1, and compared to the standard list. The resulting model card is more convenient to design very low current operating bandgap reference circuit.

| | Standard Model Card | | | | Proposed Model Card | | | |
|---|---|---|---|---|---|---|---|---|
| | IS | BF | EG | XTI | IS | BF | EG | XTI |
| NPNint | 4.0E-17 | 125.0 | 1.150 | 3.8 | 3.5E-17 | 168.7 | 1.174 | 3.8 |
| PNPpar | 1.0E-16 | 10000.0 | | | 7.3E-17 | 43.3 | 1.165 | 3.0 |
| PNPint | 2.7E-17 | 125.0 | 1.120 | 4.84 | 3.9E-17 | 167.5 | 1.177 | 4.0 |
| PNPparF | 3.0E-19 | 10000.0 | 1.120 | 4.84 | 2.4E-19 | 129.0 | 1.080 | 3.0 |
| PNPparR | 9.8E-17 | 10000.0 | | | 9.8E-17 | 129.2 | 1.184 | 3.0 |

Table 1. List of the main parameters of the standard and the proposed model card

Simulation of the bandgap temperature variation, with the new value of these parameters (in line) together with the measurements performed on silicon (in dots) for different values of the adjustment resistor $R_{ADJA}$ are given in Fig.5. This time we can observe a very good agreement between simulations and measures on Silicon for a low power bandgap circuit. Only if such a condition is reached, the design of a high accuracy, high temperature stability micro-power BGR is possible.

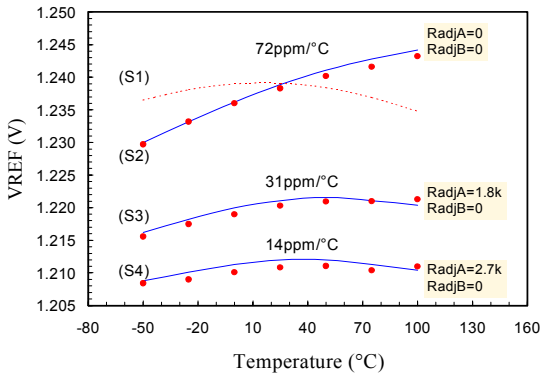



Figure 4. Characterization protocol flow diagram.

## 5. Micro-power bandgap reference design

The expansion of the portable applications has been given a great interest to design methodologies for very low consumption. Until today, the best designed bandgap reference can operate at ICC=40µA with 1µA to 10µA/branch current level (collector current). Our goal is to design a circuit able to operate at ICC=1µA with 10nA to 100nA/branch and a temperature coefficient as low as 10ppm/°C under the automotive temperature range [-50°C to 125°C]. The considered circuit has the same structure than that given in Fig. 2. Only the values of the resistors have been modified in order to allow a few micro-amps operating current. We used the temperature characteristics observed on the standard bandgap reference test cell to improve the micro-Vref design. As shown in Fig. 4, the temperature coefficient of Vref depends on the value of Vref($T_0$). To understand this phenomenon, let us write the temperature variation of Vref corresponding to the circuit given in Fig. 2 as

$$V_{ref} = V_{BEQIN}(T) + \frac{\Delta V_{BE}}{R_B(T)}\left(R_A(T) + R_B(T) + R_C(T)\right) \quad (3)$$

As shown the best temperature compensation must include the diode, PTAT and resistor temperature coefficient and will impose a unique value of the reference voltage minimizing the overall temperature sensitivity. Depending on the bias level, the process doping profile and the type of resistors, this value must be quite different from the standard one (1.225V). The temperature coefficient of the final design can be simply written as

$$TC(Vref) = TC_{VBE} - (TC_{PTAT} + TC_{Rdiff}) \quad (4)$$

The temperature coefficient of this bandgap depends on the $V_{BE}$ (the negative temperature coefficient that is bias dependent) and the PTAT (positive TC) temperature coefficients. Moreover, the resistors used in the circuit have a positive temperature coefficient that have to be compensated for. For micro-Vref design, we've decided to implement 30Ω/ poly resistors. Note that this resistor type has a negative temperature coefficient. The photomicrograph of the corresponding design is illustrated in Fig. 5.

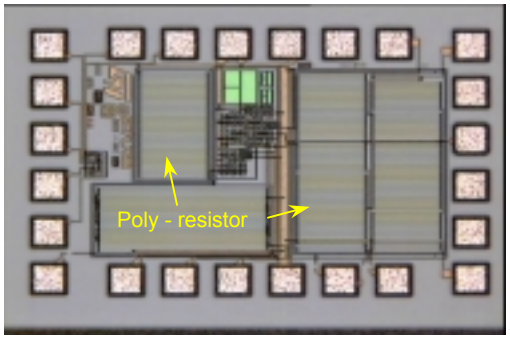



Figure 5. Photomicrograph of the micro-Vref bandgap reference circuit with R-Poly

Although these resistors are area consuming, contrary to the p-implanted resistor type, there is no substrate leakage current with such a resistor insuring a better temperature coefficient control..

## 6. Experimental results

In Fig. 6 and 7 we represent the experimental bias and temperature variation of the micro-power band gap, measured on Silicon. As shown the minimum operating current is as low as 1.4µA and the temperature coefficient range extend from 7 to 10 ppm/°C in the automotive temperature range. This corresponds to a quite good result, that has been allowed thanks to the parameter calibration on the test cell.

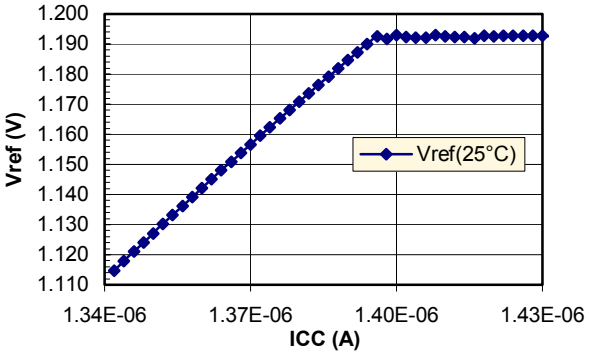



Figure 6. Photomicrograph of the micro-Vref bandgap reference circuit with R-Poly

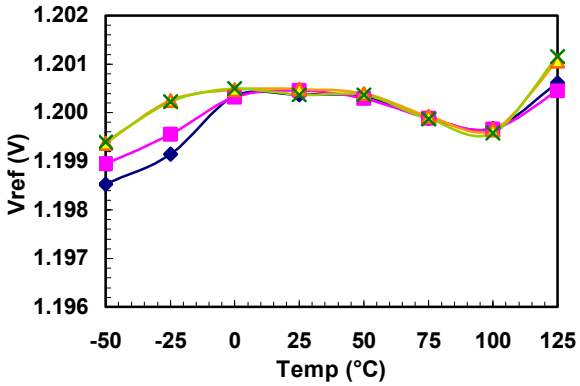



Figure 7. Temperature variation measured on four samples of the micro-Vref bandgap reference.

## 7. Conclusion

A low current dedicated characterization procedure has been presented tested and discussed in the first part of this paper. The method has been implemented in a programmable configuration test cell based on a BGR voltage circuit. The originality of this method remains in the fact that the parameters are characterized directly on the operating circuit at the well circuit bias. It is clearly shown that the parameters extracted from this approach allow a very close matching with the temperature variations observed on a real BGR voltage. A design methodology for a micro-power BGR has been presented in the second part. It has been demonstrated that with a good parameter calibration, a very high performance BGR can be achieved with standard BiCMOS processes.

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