Modeling Gate Oxide Short Defects in CMOS Minimum Transistors

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Abstract

In this paper a new model is proposed for Gate Oxide Short defects based on a non-split MOS transistor. Because the MOS is not split, this model allows to simulate minimum transistors in realistic digital circuits. The construction of the model is presented in details using a comprehensive and didactic approach. It is demonstrated that the electrical behavior of the proposed model matches in a satisfactory way the defective transistor behavior.

1. Introduction

The advent of integrated circuit technology has introduced electronics in many aspect of present-day life. As the use of electronic components increases, the expectation of lower cost, better accuracy, and higher reliability increases. Lower cost and better accuracy is achieved by putting more transistors per unit of silicon, using design automation, increasing device operation speed, and reducing its power consumption. However, these design steps cannot guarantee reliability. In fact, as the circuit density increases, the probability of a manufacturing defect increases. The higher expectation of reliability can only be met by more thorough and comprehensive testing.

Due to the complexity of IC technological process, many physical defects occur during the manufacturing of any system. The typical defects encountered in today technologies and modeled in yield simulators are the so-called spot defects that may cause shorts and/or breaks at one or more of the different conductive levels of the devices. Test generation for any type of defect is obviously not feasible due to the huge amount of CPU time and memory size required. Instead, test generation relies on fault models that are supposed to both represent the defect behavior and allow easy generation of test vectors.

Classical fault models (stuck-at, stuck-open, stuck-on, …) have been proved to be efficient for the analysis of many of these faults. However, it is well-known that these fault models cover only partially the spectrum of real failures in today's integrated circuits. The increasing demand of low ppm defect rates requires the derivation of ever more accurate fault models. In particular, a special attention must be paid to defects that exhibit complex behavior not accurately represented by classical fault models and defects with a high probability of occurrence. Gate Oxide Short (GOS) defects belong to both categories since (i) they change some of the electrical features of the transistor, and (ii) they are predominant defects in today technologies in which devices are scaled down and oxide thickness reduced. A number of research works have been conducted in the past years dealing with the electrical characterization [1-10] and modeling [11-17] of this kind of failure.

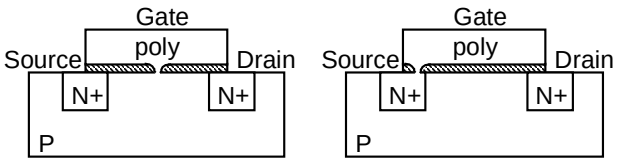
Both for the characterization and modeling process, one should distinguish between two different types of gate oxide short, i.e. GOS connecting directly the gate to the drain or source or GOS connecting the gate to the channel. For the first type of defect, a realistic model based on the addition of a short resistance between the gate the drain (or source) has been proposed in [12]. For the second type of defect, several models have been proposed based on the split of the faulty device in several smaller devices [11-14]. Although these models perfectly match the electrical characteristics of the defect behavior, they suffer from a strong limitation: they cannot be used to study GOS defects in realistic digital CMOS circuits. Indeed, these models are not able to cope with minimum transistors affected by a GOS failure. However, most of the transistors involved in a digital cell library are today designed at minimum-size. It is therefore the objective of this paper to present a new model permitting to handle minimum transistors affected by gate-to-channel shorts.

The paper is organized as follows. GOS failures and their associated behavior are described in section 2. Defect modeling is addressed in section 3 and limitations of the previously proposed models are discussed. In section 4, we introduce the new non-linear non-split model and show how this model permits to accurately represent the defect behavior while preserving the length of the original transistor. Finally, concluding remarks are given in section 5.

2. GOS Failures

2.1. Defect description

A GOS is a transistor defect that cause a relatively low impedance path between the CMOS gate and the underlying silicon. Depending on the defect location, the GOS can be seen as a short circuit between the gate and transistor channel or as a short circuit between the gate and drain or source diffusion zones. Figure 1 illustrates these two types of defect. For both types, an undesired path of current through the oxide of the gate appears thus creating a violation of the gate isolation principle. It is generally admitted that GOS may have different origins such as lithographic defect on mask, field failure due to ESD…



(a) gate-to-channel (b) gate-to-source (drain)

Fig.1: Pinhole in a MOS gate

2.2. Defect behavior

One of the main specificity of a GOS defect is that the pinhole that shorts the gate to one point of the underlying silicon creates a new device in which an important gate current can flow. It is therefore possible to study the IG vs VG characteristics of a defective transistor. As commented by the authors of many previous papers [1-3], two distinct electrical behaviors are observed depending on the defect type. The first type of defects connecting the gate to drain or source diffusion zone is referred as an ohmic defect and exhibits a linear behavior in the IG vs VGS characteristics. In contrast, the second type of defects connecting the gate to transistor channel exhibits a non-linear behavior in the IG vs VGS characteristics. Figure 2 shows typical IG vs VGS characteristics for both the ohmic and non-ohmic types of defects.

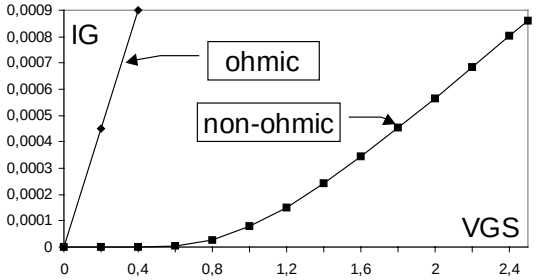
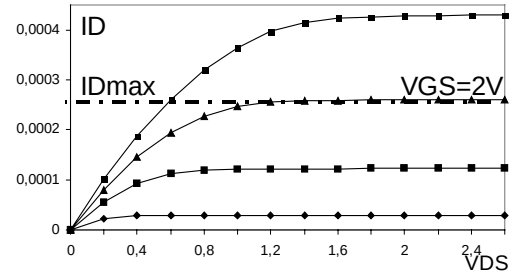


Fig.2: IG vs VGS characteristics of a MOS with a GOS

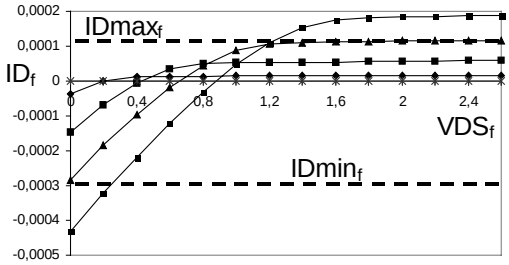
Regarding the ID vs VDS characteristics, all experiments have demonstrated that the drain current of a defective transistor only slightly resemble the typical MOS transistor drain current. Figure 3.a and 3.b show the typical ID vs VDS characteristics of non-defective and defective transistors. Basically, the defect manifests itself through two main phenomena:

- reduction of the maximum drain current at high VDS,
- appearance of a negative drain current when VDS is small in comparison with VGS.

For a given VGS, we will denote IDmax the maximum drain current and IDmin the minimum drain current at VDS=0.



(a) non-defective NMOS



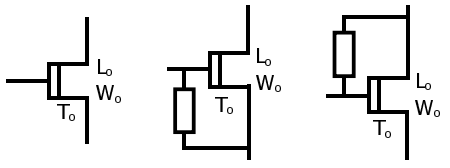
(b) NMOS with a gate-to-channel GOS

Fig.3: ID vs VDS characteristics

3. Electrical MOS models of GOS

3.1. Linear Non-Split MOS Model

A simple linear model has been proposed in [12] based on the addition of a short resistance between the gate and drain or source electrodes as illustrated in figure 4. This model is perfectly adequate to represent GOS defects connecting the gate to drain or source diffusion zone in a n-channel transistor. This model has been extended in [15-17] to cope with both n- and p-channel transistors.



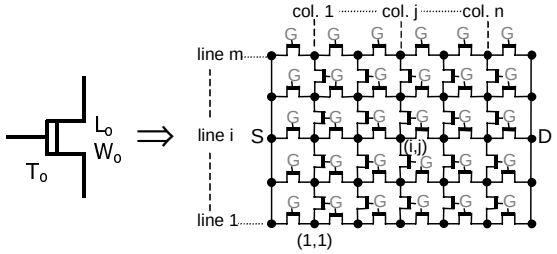
original transistor *gate-to-source short* *gate-to-drain short*

Fig.4: Linear non-split MOS model

One main advantage of these models is that the length of the original transistor T_o is preserved, implying that the model can handle minimum transistors. However, these models cannot apply for gate oxide shorts between the gate and the channel of a transistor as they present a different set of electrical properties. In particular, they are not able to represent the non-linear behavior depicted in the IG vs. VGS characteristics of figure 2.

3.2. Non- Linear Split MOS Model

In order to study GOS defects connecting the gate to the channel, an electrical model of the fault-free transistor based on a lumped-element model has been proposed in [11]. In this model represented in figure 5, the non-defective channel is split and become a two-dimensional array of MOS transistors.



(a) original MOS (b) 5x5 split model

Fig.5: Split model of a non-defective NMOS

As an example, we consider an original transistor T_o with L_o=2.1 µm and W_o=3.5 µm in a 0.25µm technological process. This transistor can be split in a 5x5 network of elementary NMOS transistors designed at minimal length L_i=0.25µm and W_i=0.5µm. As illustrated in figure 6, a good agreement is observed between the simulated ID vs VDS characteristics of the 5x5 network and the original transistor.

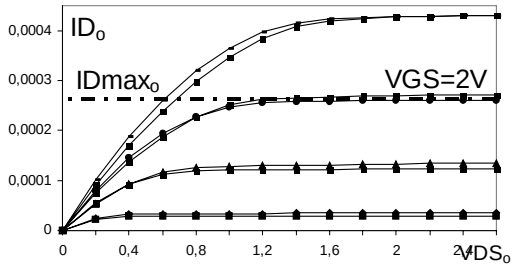


Fig.6: Comparison of the ID vs VDS characteristics of the original transistor and the split MOS model

Based on this lumped-element model, a GOS defect can be introduced in the transistor by connecting a short resistance R_{GOS} between the common gate G and one of the internal nodes of the network, denoted (i_f,j_f). Figure 7 gives an example of a central defect introduced in the transistor. The defect resistance and location can then be varied through the value of R_{GOS} and position (i_f,j_f) in the network.

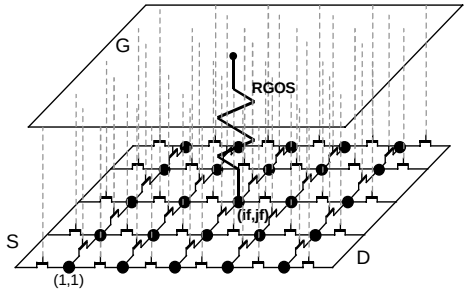
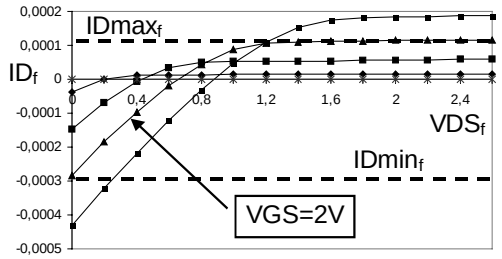
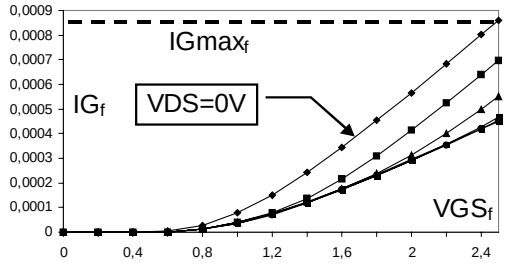


Fig.7: Split model of a NMOS with a GOS

This model has been demonstrated to perfectly describe the electrical behavior of gate-to-channel shorts [8-9]. For illustration, figure 8.a shows the simulated ID vs VDS characteristics of a defective transistor with a 1Ω central defect. For a given VGS, for instance VGS=2V, we observe a reduction of the maximum drain current $IDmax_f$ compared to the non-defective one $IDmax_o$ together with the appearance of a negative drain current for small VDS. This model also permits to simulate the IG vs VGS characteristics, as depicted in figure 8.b. Note that these characteristics are in agreement with the experimental behavior observed for gate-to-channel shorts (see figure 2).



(a) ID vs VDS characteristics



(b) IG vs VGS characteristics

Fig.8: Simulated I-V charateristics of a defective NMOS using the split model

3.3. Limitations

As described in the previous section, the split MOS model for GOS perfectly describes the behavior of gate-to-channel defects and for this reason has been widely studied by different authors [8-14]. However this model suffers from severe limitations as discussed below.

As everybody knows, SPICE simulations are performed using card models describing the transistor parameters in the targeted technological process. Using these card models, transistors of any length can be simulated as far as they are larger than the minimum (L_{min}) allowed by the technological process. Any attempt to simulate transistors smaller than the minimum would make the simulation results (if any) unreliable.

Consequently, when using the split MOS model for simulating GOS defects, the elementary MOS transistor obtained after the splitting of the original transistor cannot have a length smaller than L_{min}. This obviously implies that the original transistor cannot be at minimum length. Even the smallest network composed of two transistors in series as suggested in [13-14] corresponds to an original transistor with length equal or higher that $2L_{min}$. It is therefore impossible to study minimum transistors affected by GOS failures using a split MOS model. This is an extremely strong limitation taking into account that in a classical digital cell library, all transistors are designed at minimum length. In this context, although the split MOS transistor permits to accurately model the defect behavior, it clearly appears inadequate to simulate GOS defects in realistic digital circuits.

4. Non-Linear Non-Split MOS Model

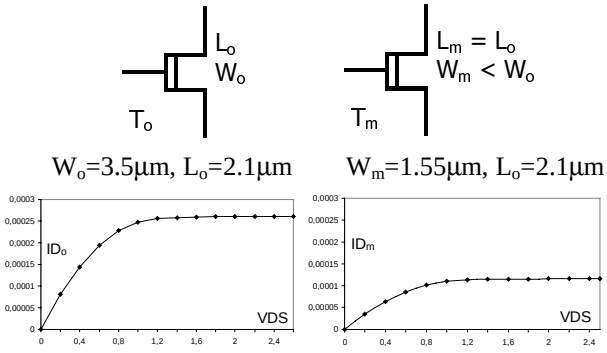
This section describes the new model we developed for GOS defects presenting a non-linear behavior, i.e. gate-to-channel shorts. Our first objective is not to split the original transistor as proposed in [15] for the linear model in order to preserve the length of the original transistor. Our second objective is to introduce non-linearity in the model in order to properly represent the behavior of this type of defect. Consequently, our non-linear model is constructed by adding non-linear components to the original transistor.

For the demonstration, we reuse the original transistor of figure 5 with L_o=2.1µm and W_o=3.5µm in a 0.25µm technology. Because the split model has been proved very accurate [8-9], we consider that the characteristics of the faulty transistors are given by figure 8. Note that these characteristics obtained with the split model are just used here as a reference.

Our non-linear non-split MOS model is now constructed in three steps with the aim to mimic as precisely as possible the characteristics of figure 8.

Step 1

As commented in section 2.2, a first specificity of a transistor affected by a GOS failure resides in the reduction of the drain current. For a given VGS, we observe that the maximum drain current in the defective transistor is smaller than the maximum drain current in the non-defective one: $IDmax_f < IDmax_o$ (see figure 6 and 8). Consequently, we start our model construction with a transistor with the same length L_o than the original transistor but a smaller width W_m (W modified) to reduce the drain current. Note that the length of L_o of the original transistor is preserved as required by our objectives; only the width W_m is modified and calculated to match the faulty current $IDmax_f$. Figure 9 illustrates this first step.



W_o=3.5µm, L_o=2.1µm W_m=1.55µm, L_o=2.1µm

(a) original transistor (b) modified transistor

Fig.9: Non-linear non-split model - Step 1

Step 2

The second specificity of a transistor affected by a GOS failure is the appearance of a negative drain current for low VDS. Consequently, the second step of our model construction consists in connecting an additional component allowing a current to flow from the gate to the drain. This additional component should act only at low VDS but not modify the I-V characteristics at high VDS. We propose to insert an additional transistor T_a connected as illustrated in figure 10.

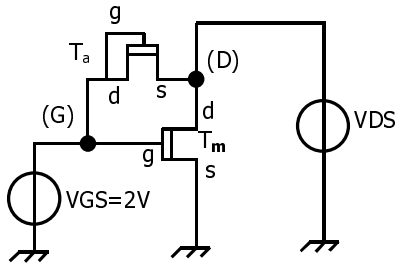
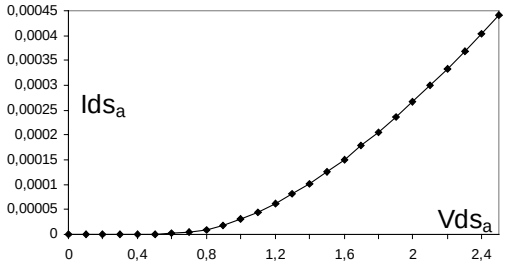


Fig.10: Non-linear non-split model - Step 2

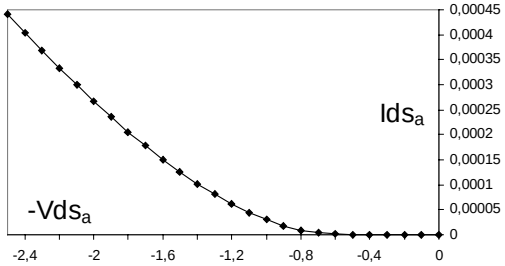
For the sake of clarity, the behavior of the above circuit is analyzed for VGS=2V. The results will be then extended to any VGS.

When VDS is higher than VGS=2V, the additional transistor T_a is OFF and has no influence on the I-V characteristics. When VD is smaller than VGS=2V, the additional transistor T_a has its drain in node G and its source in node D as illustrated in figure 10. Under these conditions, the transistor is ON and operates as a rectifier with Vgd_a=0. The corresponding Ids_a vs Vds_a characteristics are given in figure 11.a. It is to note that $Vds_a = VGS - Vds_m$ so in figure 11.b and 11.c the

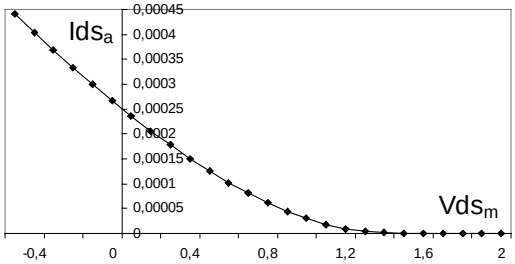
characteristics are flipped and shifted to have compatible x-axis with figure 8.a.



(a) Ids_a vs Vds_a



(b) Ids_a vs $(-Vds_a)$



(c) Ids_a vs $Vds_m=(VGS-Vds_a)$

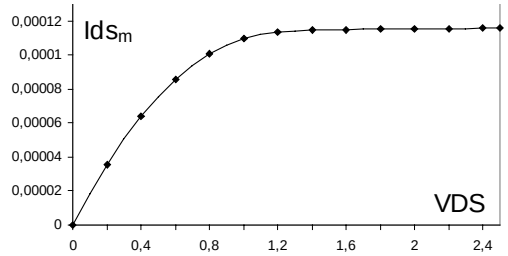
Fig.11: I-V characteristics of the additional transistor T_a

In node D, we can write the current equation as follows:

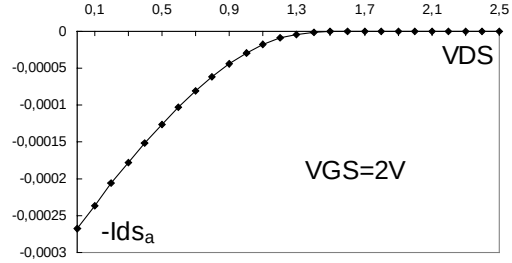
$$ID_f + Ids_a = Ids_m \Rightarrow ID_f = Ids_m + (-Ids_a)$$

That means that the current ID_f flowing in the complete device can be obtained by adding the two characteristics of figure 12.a and 12.b. The resulting ID_f current is represented in figure 12.c.

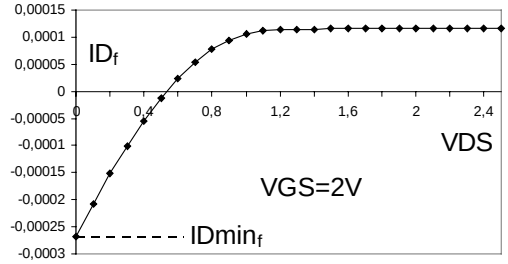
It is now just necessary to adjust the value of the $IDmin_f$ current of figure 12.c to exactly fit the current $IDmin_f$ of figure 8.a. The value of this current actually just depends on the additional transistor size T_a since the current Ids_m is equal to 0 at point VDS=0. Consequently, the current $IDmin_f$ in our model is simply set by tuning the W_a/L_a parameter of the additional transistor T_a. Note that in figure 12.c, the W_a/L_a parameter has been tuned to match the $IDmin_f$ value of figure 8.a with W_a=3.6µm and L_a=2.1µm.



(a) Ids_m vs VDS



(b) $-Ids_a$ vs VDS



(c) ID_f vs VDS

Fig.12: I-V curves in the non-linear non-split model

The same demonstration can be made for any potential VG giving the complete set of ID_f vs VDS characteristics of our non-linear non-split MOS model as presented in figure 13. It clearly appears that this model with its additional transistor correctly mimics the ID-VDS behavior of a gate-to-channel GOS.

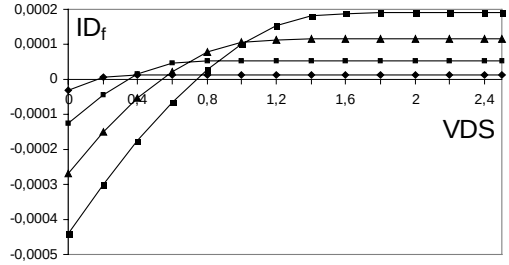


Fig.13: ID_f vs VDS characteristics of the non-linear non-split model

Step 3

Finally, the last specificity of a transistor affected by a gate-to-channel short is the presence of a non-linear gate current. Consequently, the last step in our model construction consists in connecting another additional transistor T_b allowing a current to flow from the gate to the source, as illustrated in figure 14.

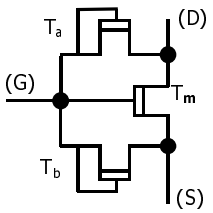


Fig.14: Non-linear non-split model - Step 3

This second additional transistor actually acts symmetrically to the first additional transistor, creating an IG current in the model. As performed in the previous step with the $IDmin_f$ current, we adjust the W_b/L_b conductance of the second additional transistor T_b to mimic the IG_f vs VGS_f characteristics of figure 8.b. For example, when VDS=0, the current IG is maximum and figure 15 gives the equivalent circuit. The current $IGmax_f$ is equal to Ids_a+Ids_b. The current Ids_a has already been fixed and so $IGmax_f$ is adjusted through W_b/L_b. To match the $IGmax_f$ value of figure 8.b, we set the additional transistor T_b to with W_b=3.6µm and L_b=2.1µm.

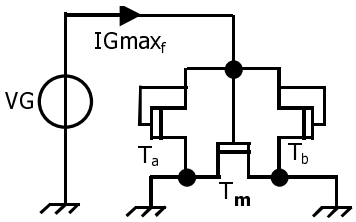


Fig.15: Equivalent circuit for the model at VDS=0

Finally, figure 16 gives the complete set of the IG vs VGS characteristics simulated with our model. These characteristics correctly reproduce the IG-VGS behavior of a gate-to-channel GOS.

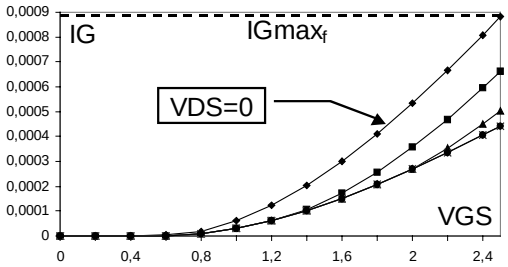


Fig.16: IG_f vs VGS of the non-linear non-split model

5. Conclusions

In this paper, we proposed a new non-linear non-split MOS model for gate-to-channel GOS defects. The fundamental idea is not to split the original transistor in order to handle minimal-length transistors and therefore enable the simulation of GOS defects in realistic digital circuits. Based on the analysis of the electrical defect behavior, we developed a comprehensive method for the construction of the model. The model is constructed by first modifying the width of the original transistor, and then inserting two additional transistors between the gate and drain/source of this transistor:

- the width modification (W_m) of the original transistor allows to adjust the level of the drain current at high VDS ($IDmax_f$),
- the conductance W_a/L_a of the first additional transistor allows to adjust the level of the negative drain current at low VDS ($IDmin_f$),
- the conductance W_b/L_b of the second additional transistor allows to adjust the level of the gate current (IG_f).

It has been shown that the behavior of the proposed model matches in a satisfactory way the behavior of a defective transistor model.

Finally, future work will concentrate on the tuning of the model parameters (W_m, W_a/L_a, W_b/L_b) to reproduce GOS defects of various resistance, location and size.

6. References

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