Inductance Effect in Crosstalk Prediction

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***Abstract*—Rapid progress in integrated circuit technology has led to an increase in switching speeds of digital circuits. This increase is the primary reason why inductance noise causes chips to fail. As a result, there is a growing interest in the inductance associated with on-chip signal lines. In this paper, we present the electromagnetic analysis we have followed in order to determine the accurate values of the R, L, C, G equivalent parameters from which a set of multiple coupled transmission lines could be modeled. We then determine the most critical parameters which make the inductance effect important and we propose a new analytical expression to accurately evaluate the crosstalk voltage.**

***Index Terms*—Crosstalk, electromagnetic analysis, inductance effect, on-chip interconnections, transmission lines.**

I. Introduction

MICROELECTRONICS evolution is characterized by an important rise in integration and circuit speed running. Today the race toward integration is faced with the problem of interconnects which has become one of the blocking points in the improvement of circuit performances. Technological advances in microelectronic fabrication techniques focus on the maximum integration of devices in the same chip. This implies an increase in the role of interconnects in circuit behavior, which necessitates the analysis of interconnects in integrated circuits. Tools employed in order to get interconnect characteristics are of two kinds. The first kind makes use of tables and analytic formulations, derived from the equations of electromagnetism. Here the number of approximations increases considerably with the problem complexity, so that the results could become unreliable even for simple structures. The second type of tool requires numerical simulation help (these utilities are often based on the finite difference time domain or on the finite element method). Here the accuracy of the solutions obtained is better than in the first type. However these tools are mainly geared to simulate propagation phenomena in models which eventually show quite a large diversity of sizes (such as small lines imbedded in a large background), and from which the users may encounter difficulties in meshing the models. Therefore it is desirable to have numerical methods which could give confident modeling of relatively complex structures, and in particular the magnetic coupling between their constituting elements.

In deep submicron technology, the wire thickness is often greater than the wire width, and the spacing between adjacent wires is often smaller than the distance between adjacent metal layers. This makes the coupling capacitance between adjacent wires on the same layer larger than the ground capacitance to adjacent layers. The reduction of distances between wires in deep sub-micron technologies increases the coupling effects and interactions between circuit interconnection lines. Two adjacent wires form a coupling capacitor and a mutual inductor. A voltage or a current change on one wire can thus interfere with the signal on the other wire. This interference noise (crosstalk) consists of the appearance of a glitch in a line (victim line) which is in its steady state (high or low level) when a neighboring line (affecting line) makes a transition (high–low or low–high). Noise profoundly affects the performance of a circuit and is becoming one of the most important areas for concern in the design of deep submicron integrated circuits. This problem is especially serious for designs with higher clock frequencies, lower supply voltages, and the use of dynamic logic since they have a lower noise margin. To ensure that a final layout is noise immune, accurate and efficient noise models are needed to guide interconnect optimization at various stages.

Recently, a number of simple crosstalk noise models were proposed. The effects of the coupling capacitance have been addressed by Shoji [1] using a simple linear RC circuit and by Becer [2] and Vittal [3], using Π and L lumped-circuit models. Recent models such as [4], [5] propose complex models of prediction of crosstalk requiring complex calculations, and, as a result important CPU time. Reference [6] proposes a closed-form peak noise formula by assuming a saturated ramp input for the aggressor net. Most of these models, however, did not consider the distributed nature of RC networks, which is necessary in deep sub-micron designs. Servel [7] proposes an analytical expression of crosstalk voltage for one, two and four adjacent lines, which takes into account interconnect capacitances, line resistance and their distributed nature, driver resistance and variable strengths of the buffers driving coupled lines. None of these works includes the inductive effects on crosstalk evaluation, which is becoming an important consideration regardless of the system frequency. An efficient on-chip interconnect model is critical to interconnect optimization at high-level, logic synthesis and physical design. Closed-form formulas are particularly efficient and effective for these design stages.

In this paper, we highlight the importance of on-chip inductance modeling for crosstalk voltage evaluation, and we show how the most critical parameters make the inductance effect very important in high-performance VLSI circuit design today. We also propose a new analytical expression to accurately evaluate the crosstalk voltage.

This paper is structured as follows: after the introduction, Section II presents the electromagnetic analysis we have followed in order to determine the accurate values of the RLCG

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G. Servel and D. Deschacht are with Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier, Montpellier Cedex 5 34392, France (e-mail: deschacht@lirmm.fr).

F. Saliou, J. L. Mattei, and F. Huret are with Laboratoire d'Electronique et Systèmes de Télécommunications, Université de Bretagne Occidentale, Brest Cedex 29285, France.

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equivalent parameters from which a set of multiple coupled transmission lines could be modeled. In Section III we compare the time domain response of three coupled lines for RC and RLCG models to give the respective variations of the crosstalk amplitude in order to determine the level of modeling which is necessary to represent interconnects. We investigate the most critical parameters which make the inductance effect important. Finally, a corrective term is proposed in Section IV to improve the accuracy of the simple RC model to take into account the inductive effects.

II. Quasi-Static Characterization of Interconnects

For submicron design, where interconnect dramatically affects the performance, the broad-band transmission line behavior of interconnects have to be characterized by rigorous analytical or numerical approaches. Therefore, the simulation of high-speed analog and digital integrated circuits requires the analysis of frequency-dependent transmission lines with nonlinear devices.

The frequency-dependent behaviors of transmission lines such as losses and dispersions are accurately represented in the frequency domain, while the determination of transmission line delays and reflections requires the time-domain simulation of a nonlinear network often used as drivers and terminations. In order to resolve this dilemma, most analysis programs use numerical-transform techniques to alternate between frequency and time-domain.

Interconnect cross-sectional surfaces are inhomogeneous. According to Maxwell's equations, all of the propagating modes within an inhomogeneous structure are hybrid. Usually, to analyze such waveguides, it is necessary to perform a full-wave analysis. In such cases, the Finite Element Method, associated with the Helmholtz equation, is probably the full-wave analysis method that is the most generally applicable and the most versatile [8], [9]. The frequency dependent R, L, C, G per unit length elements can be extracted from the corresponding full-wave results. However, it is advantageous to represent the broad-band interconnect characteristics in terms of equivalent circuits consisting exclusively of ideal lumped elements because, in this case, the approach is compatible with general purpose circuit simulators such as SPICE. In this paper, by considering the standard technological constraints of the 0.25 μm technology, we first demonstrate that the per unit length elements $(R, L, C, \ldots)$ of studied digital circuits on-chip interconnects can be efficiently determined by quasistatic analysis.

Since this analysis is readily extended to the multiconductor case, the discussion is focused here on two coupled lines depicted in Fig. 1.

The calculated self and mutual interconnect line parameters are shown in Figs. 2–4. To demonstrate the accuracy of the quasistatic calculation, these figures also include the corresponding full wave solution [8].

The bandwidth used in determining relevant frequency components of a digital pulse with a transition time tr, is generally accepted as $0.35/tr$. We can also estimate the Useful Frequency Bandwidth from the clock frequency by $10.f$ clock. This leads to 5 GHz for a classical 0.25 μm technology. For frequencies higher than this value, the spectral component amplitudes are very small.

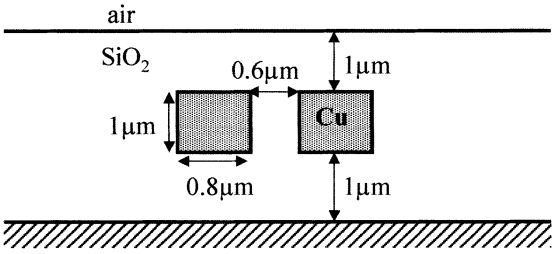


Fig. 1. Two coupled Cu lines.

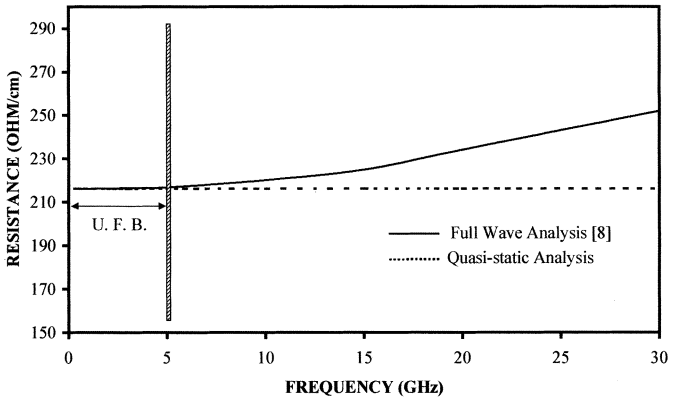


Fig. 2. Behavior of serie resistances of the two coupled lines.

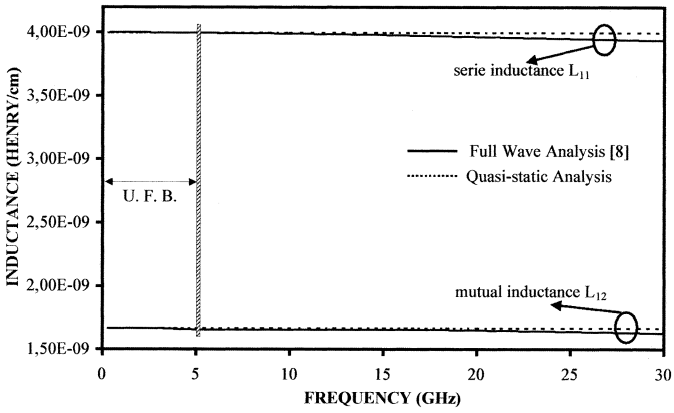


Fig. 3. Mutual and serie inductance of the two coupled lines.

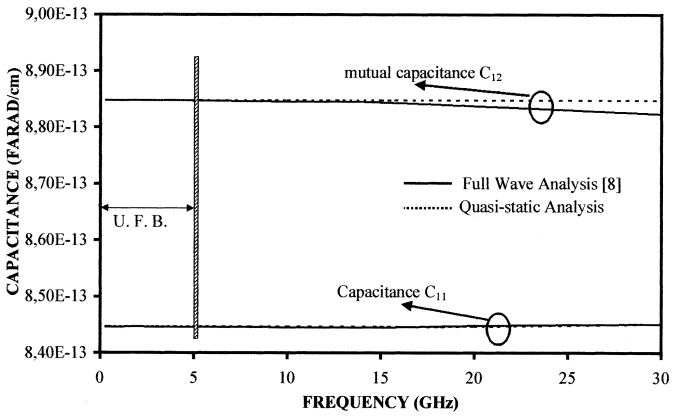


Fig. 4. Capacitances of the two coupled lines.

In addition, the attenuation of these components increases naturally with the frequency. This phenomenon also decreases the influences of the higher frequencies' small components.

In the useful frequency bandwidth (UFB), the comparison shows good agreement between the quasistatic and the full-wave solutions, and allows us to use frequency-independent per unit length elements. We have to note that the quasistatic approximation used in this study, depends only on the frequency (UFB), and not on the wire length. Finally, the accuracy of the quasistatic calculation has been also demonstrated for on-chip interconnects on lossy silicon substrate [10].

Now, this section briefly presents the principles of the analysis we have followed in order to obtain the numerical values of the (R, L, C, G) equivalent parameters from which a set of coupled transmission lines could be modeled. This work has been performed by using commercial FEM packages developed for two dimensional computation of electromagnetic problems [11]. These packages allow us to solve conveniently and independently both magnetic and electric fields, provided that the quasistatic condition is fulfilled. A noteworthy advantage of this static approach lies in the very reduced CPU time taken for each computation (about 4 minutes). The computational model is based on the static Maxwell's equations. This method divides the studied structure into sub-domains. It is then possible, with this tool, to fit any polygonal shape by choosing the element shapes and sizes.

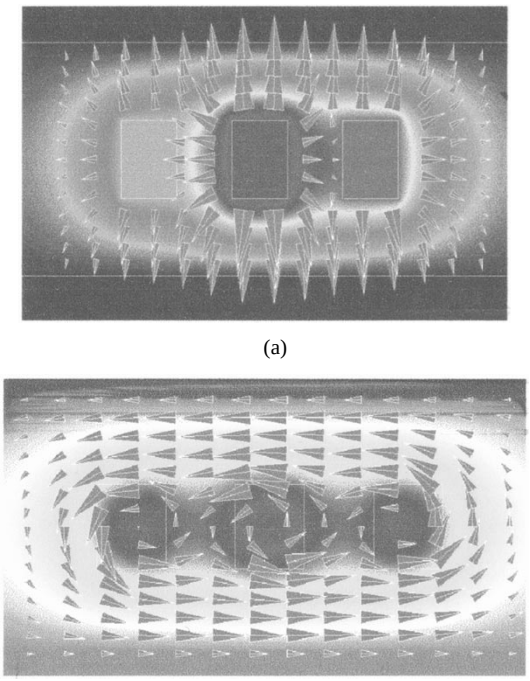
We focus here on the (R, L, C, G) parameters which describe one central and two adjacent parallel transmission lines. The three copper lines are imbedded in a dielectric matrix (permittivity $\varepsilon_r = 3.9$), with lower and upper ground planes, as sketched in Fig. 6. The electric potentials and the currents have been fixed to arbitrary values. In order to modify the coupling between a given line and the two other lines, the spacing between them (denoted S) has been changed in the range 0.6–1 μm. Owing to the determination of appropriate mesh patterns, an accuracy of about 1% on the computed fields has been reached. Typical views of the field distributions are represented on Fig. 1. The arrows are the electric field [Fig. 5(a)] or the magnetic field [Fig. 5(b)]; the colors give the intensity of the electric potential or of the scalar magnetic potential (values increasing from blue to red). They give qualitative indications on the intensity of the coupling strengths.

As an example, the magnetic energy (E_m) and the electric energy (E_e) stored in the structures have been computed. From these the following set of parameters can be calculated: the selfs and the mutual inductances (L_{ii} and L_{ij}, $j \neq i$), the capacities and the influence coefficients (C_{ii} and C_{ij}, $j \neq i$). Their numerical values have been obtained from the following general expressions (1a) and (1b):

$$E_m = \tfrac{1}{2} \sum_{i=1}^{n} L_{ii} I_i^2 + \sum_{i=1,\, i \neq j}^{n} L_{ij} I_i I_j \qquad \text{(1a)}$$

$$E_e = \tfrac{1}{2} \sum_{i=1}^{n} C_{ii} V_i^2 + \sum_{i=1,\, i \neq j}^{n} C_{ij} (V_j - V_i)^2 \qquad \text{(1b)}$$

where the sums are over the n conductors (here we take $n = 3$). I_i denotes the currents flowing through the ith line, which is placed at the potential V_i. Obvious symmetry considerations lead to reduce the twelve unknowns to (L_{11}, L_{22}, L_{12}, L_{13}) in (1a), and to (C_{11}, C_{22}, C_{12}, C_{13}) in (1b). So, in both these cases, and for each value taken by the spacing parameter S, four values of the stored energy have been computed (corresponding to different values of the I_i and of the V_i), and the equations solved.



(a)

(a)

Fig. 5. (a) Electric field and (b) magnetic field.

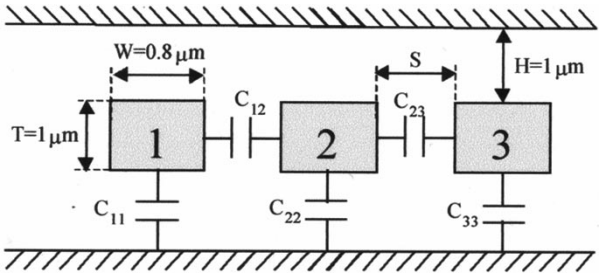


Fig. 6. Interconnection geometry.

Fig. 6 represents the interconnect geometry used to illustrate our study. The lower metal 3 and upper metal 5 layers are considered to be very dense and the perfect metallic walls are taken into account on both sides of the metal 4 layer. In this case, the conductance G is negligible (10^{-6} mS/cm) and must not be incorporated in the model. Corresponding electrical parameters are given in Table I.

III. Comparison Between RC and RLC Models

The first problem is to determine the level of modeling which is necessary to represent deep-submicron interconnects. With this aim, we compare the time domain response for RC and RLC models. The crosstalk amplitude is obtained by HSPICE simulations with a 0.25 μm process, with a level 49 foundry specified card model, the interconnection being modeled by an RC

TABLE I
ELECTRICAL PARAMETERS USED TO MODEL THE INTERCONNECTIONS

	C_{11}=C_{33} fF/cm	C_{22} fF/cm	C_{12}=C23 fF/cm	L_{11}=L_{22}=L_{33} nH/cm	L_{12}=L_{23} nH/cm	R_1=R_2=R_3 Ω/cm
S = 0.6 μm	820	500	880	4	1.66	216
S = 1 μm	865	600	560	4	1.30	216

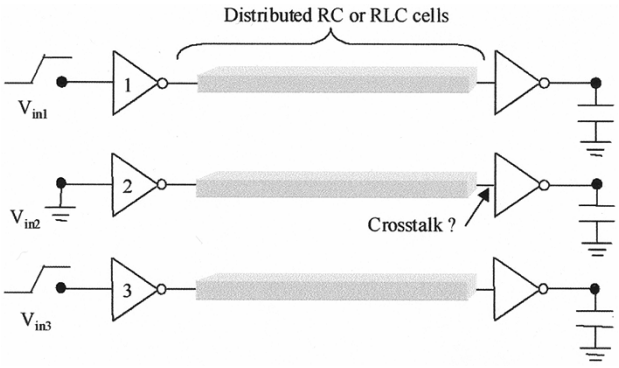


Fig. 7. Worst-case configuration.

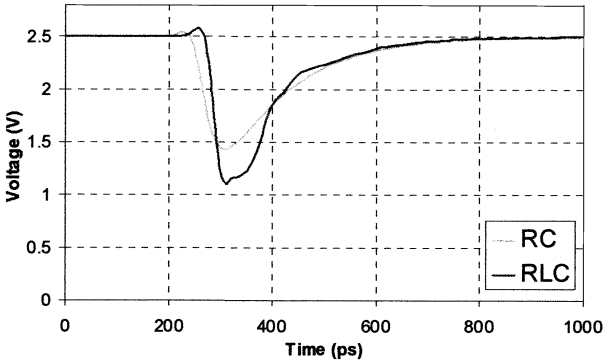


Fig. 8. Signal variation at the output of the victim wire.

or RLC distributed model, whose number of basic cells depend upon the considered length. The crosstalk amplitude increases with the number of adjacent lines. We only consider the case where inaccurate evaluation of the crosstalk amplitude could be at the origin of a malfunction of the circuit, so we directly study the case of the bus structure. We consider three, 6 mm length, adjacent lines in the worst-case configuration, that is to say, when $Vin1$ and $Vin3$ (inputs of the aggressors) change from 0 to Vdd and $Vin2$ (input of the victim line) is at Vdd, we have the most important noise voltage induced on the victim line [7] (Fig. 7). The buffer sizing is calculated to keep a constant loading factor equal to 5, and a 2 μm receiver size is used. Fig. 8 shows the temporal variation of the voltage at the output of the victim interconnection.

This first result shows a discrepancy between the two models, and the need to evaluate in detail the inductive effects. The inductance increases the crosstalk amplitude, and a logic fault can be shielded by using a simple RC model.

Fig. 9 represents the variation of the crosstalk amplitude versus the interconnection length for two different spaces, S, between lines, and the corresponding discrepancy in percentage, Fig. 10, between RLC and RC models. Whatever the space between the lines, the crosstalk amplitude increases

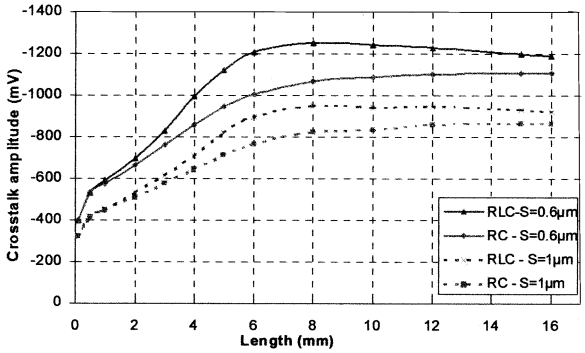


Fig. 9. Crosstalk amplitude variation versus interconnection length.

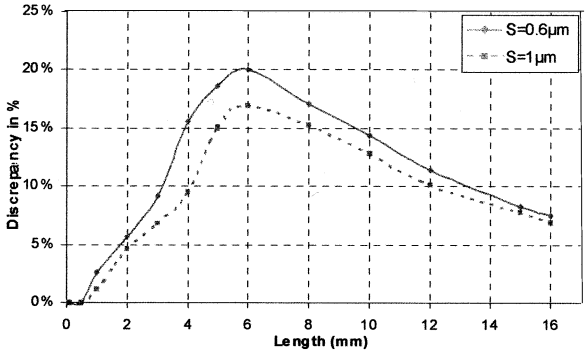


Fig. 10. Discrepancy between RLC and RC model versus interconnection length.

with lengths up to 6 mm with a tendance toward a constant value. Only an analytical expression can rapidly determine this maximum value. In a strategy of buffering, the knowledge of this value is fundamental. When the propagation delay poses no problem, the maximum value of interconnect length on a chip, can for some cases be equal to the half perimeter of the chip. The propagation can then be made with two or three clock cycles. So, even if the maximum number of interconnect in a bus is only a few millimeters, it is important to analyze and to validate the analytical expressions up to this maximum value.

The discrepancy increases with the interconnection length, because when the length of the wire is no longer negligible in comparison with the length of the associated wave, the quasistatic hypothesis. Current and Voltage constant in the propagation direction isn't realized, then inductance modeling becomes necessary. For long lines however, the reflection phenomena are shielded from the attenuation factor, the amplitude of the reflected wave decreases with the increase in length, so that the reflection effect becomes negligible. The inductance modeling is no longer necessary.

We now analyze this discrepancy versus all the parameters, by beginning with the sensitivity study of interconnect process parameters. Various low-k materials have been introduced to reduce not only the intra-metal capacitance in the same plane, but also the inter-metal capacitance between two planes. Fig. 11 shows that we have obtained similar results with different relative permittivity, ε_r, varying between 4 and 2.5, for three coupled lines of 6 mm with three different sizing for the buffer corresponding to different loading factors F. The relative permit-

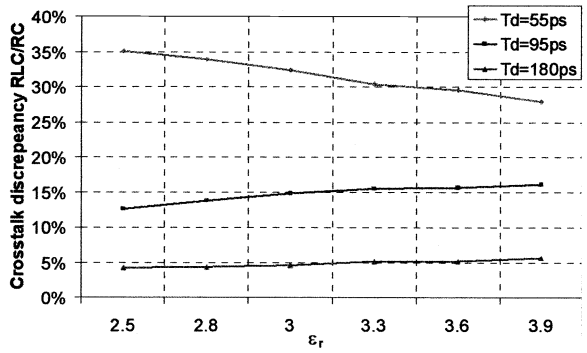


Fig. 11. Discrepancy between RLC and RC model versus permittivity.

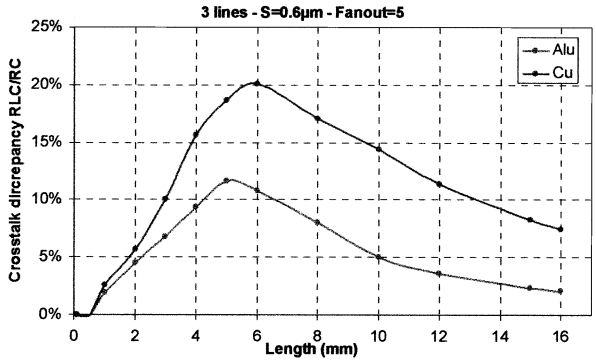


Fig. 12. Discrepancy between RLC and RC model versus interconnection length for Al and Cu wire.

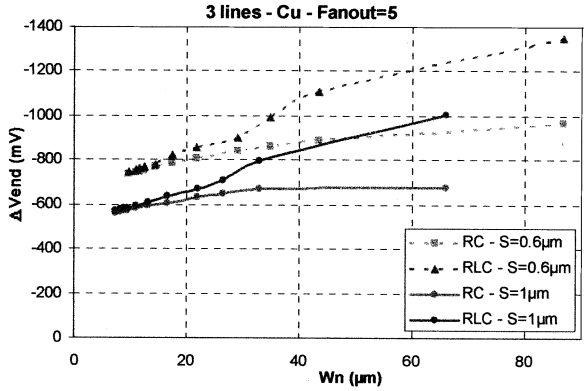


Fig. 13. RLC and RC crosstalk amplitude versus transistor size for two spacing between lines.

tivity doesn't affect significantly the discrepancy between RC and RLC models.

With the aim of higher performance, the use of some low resistivity metals has been studied to replace Al in order to minimize wire RC delays and many designers have demonstrated the success of using copper (Cu) wires. Cu is very attractive due to its low resistivity and excellent electromigration resistance. But the process integration of Cu poses many potential problems one of which is diffusion, and as a result, barrier layers need to be introduced. We compared the behavior between Al and Cu wires in Fig. 12. As was expected, the discrepancy between RLC and RC models increases when the resistivity of the lines decreases.

In Fig. 13 we show the noise amplitude and the corresponding discrepancy versus driver size (W_N) for 4 mm interconnect

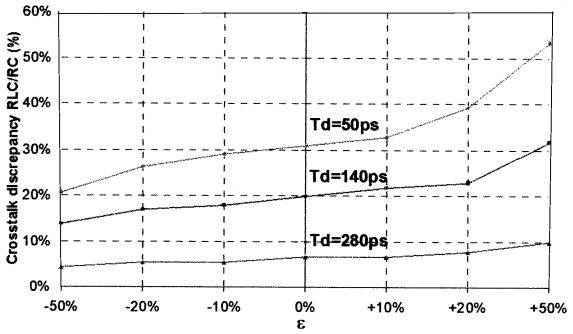


Fig. 14. Discrepancy between RLC and RC model versus a variation of the inductance value.

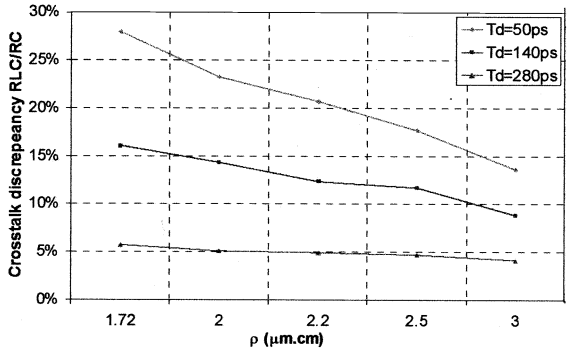


Fig. 15. Discrepancy between RLC and RC model versus the resistivity of the metal layer.

length. Driver size ranges from 7 μm to 85 μm corresponding to a loading factor between 2 and 12, and two different spaces between lines. We find that a stronger driver notably increases the discrepancy. The higher the driver size, the larger the RLC/RC discrepancy. The reason for this is that strong drivers yield faster-ramping waveforms, which give higher $L\omega/R$.

The following figures summarize these variations:

1) versus the variation of the inductance, written as $L = L_0(1+\varepsilon)$, Fig. 14, for three different input transition times; we have verified that the mutual inductance has no significant influence on the crosstalk amplitude;
2) versus the resistivity of the metal used for the interconnection, Fig. 15, for three different input transition times.

IV. Analytical Expression

In [7], the authors have presented a new simple closer form expression to calculate the crosstalk amplitude between two, three and five adjacent lines, using an RC distributed model. To take into account inductive effects, it is possible to add a corrective term to the calculation of this RC model, as

$$\Delta V_{RLC} = \Delta V_{RC} \cdot \left(1 + \alpha \cdot \frac{L_{22} \cdot \omega}{R_{line2}}\right)$$

with

$$\omega = \frac{2 \cdot \pi \cdot 0.35}{T_{com}}$$

and

$$\alpha = \frac{1}{0.35} \cdot \exp\left(-\frac{\left(\frac{R_{inv1}+R_{inv3}}{2}\right) + R_{inv2} + R_{line2}}{95}\right).$$

TABLE II
COMPARISON OF CROSSTALK VALUES FOR $W_{N1} = W_{N3}$

Length (mm)	W_{N1}=W_{N3} (μm)	W_{N2} (μm)	HSPICE ΔV_{RC} (mV)	HSPICE ΔV_{RLC} (mV)	MODEL ΔV_{RLC} (mV)	Error %
0.5	3.3	4.3	–530	–530	–530	0%
1	6.5	8.7	–575	–590	–576	–2.37%
3	19.6	26	–761	–803	–825	2.74%
4	65.6	86.8	–964	–1353	–1377	1.77%
4	26.2	34.7	–860	–994	–971	–2.31%
4	13.1	17.4	–785	–825	–799	–3.15%
6	98.4	130.2	–1068	–1397	–1447	3.58%
6	39.2	52.1	–1006	–1208	–1167	–3.39%
6	19.7	26	–914	–970	–954	–1.65%
10	32.8	43.4	–1062	–1174	–1115	–5%
12	39.4	52.1	–1086	–1185	–1130	–4.64%
16	52.5	69.4	–1104	–1174	–1129	–3.83%

TABLE III
COMPARISON OF CROSSTALK VALUES FOR $W_{N1} \neq W_{N3}$

Length (mm)	W_{N1} (μm)	W_{N2} (μm)	W_{N3} (μm)	HSPICE ΔV_{RC} (mV)	HSPICE ΔV_{RLC}(mV)	MODEL ΔV_{RLC} (mV)	Error %
0.5	16.4	8.7	3.3	-562.3	-567	-562	-0.88%
0.5	6.5	4.3	16.4	-1008	-1013	-1008	-0.49%
2	65.5	34.8	13.1	-663.6	-728	-768	5.64%
2	26.5	17.4	65.5	-1100	-1142	-1250	7.76%
4	131	69.5	26.2	-768	-1061	-1004	-5.37%
4	52.4	34.8	131	-1165	-1445	-1518	5.05%
6	196.5	104.3	39.3	-927	-1129	-1190	5.40%
6	78.6	52.1	196.5	-1205	-1467	-1545	5.32%
10	327.4	173.8	65.5	-1061	-1203	-1225	1.83%
10	131	86.9	327.4	-1182	-1343	-1364	1.56%
15	491	260.7	98.2	-1095	-1183	-1159	-2.03%
15	196.5	130.3	491	-1147	-1241	-1213	-2.26%

L_{22} is the inductance of the line 2, R_{inv1}, R_{inv2} and R_{inv3} are the equivalent resistances of the inverter 1, 2 and 3 respectively, R_{line2} is the resistance of the line 2 and T_{com} the rise time at the input of the inverter 2.

To validate this expression, we have simulated more than a hundred different configurations, with a range of wire length between 0.5 mm to 20 mm. We give here in Tables II and III, some examples of these comparisons between calculated and simulated values of the crosstalk amplitude, for the cases where $S = 0.6$ μm, for different configurations. For all the simulations, we considered the worst-case configuration, with $W_P = 2.W_N$. In Table II we keep the same size for the buffers of the two aggressor's lines, the size of the buffer of the victim line being different, as reported in the table. We give the simulation values of the simple RC distributed model and the values of the RLC model. These values are compared with those calculated by our expression. Finally the discrepancy between calculated and simulated values is given in the last column. We can see the good agreement and the importance of the corrective term.

In Table III, we consider different sizes for the buffers.

For these cases, we can see also a good agreement between simulated and calculated crosstalk values and the necessity of taking into account the inductance effect in a large range of length.

We now consider a new interconnect geometry. The corresponding electrical parameters obtained by electromagnetic simulations are

$$R = 172\,\Omega/\text{cm} \quad C_{11} = C_{33} = 1870\,\text{fF/cm}$$
$$C_{22} = 1600\,\text{fF/cm} \quad C_{12} = C_{23} = 400\,\text{fF/cm}$$
$$L_{11} = L_{22} = L_{33} = 4.9\,\text{nH/cm}$$
$$L_{12} = L_{23} = 0.912\,\text{nH/cm}.$$

For $S = 1$ μm, and the size of the buffers calculated to keep a constant loading factor equal to 5, we have obtained the following results given in Table IV.

For this configuration, largely different from the previous one, the accuracy of our proposed model is also good, and simulations with an RLC model are essential. The inductive effect cannot be neglected.

The coefficient α has been determined for the 0.25 μm technology. For the passage to a new technology, this corrective term has the same form, but it will be necessary to fit the new coefficient. In each case, the error between calculated and simulated values is less than 10%.

V. CONCLUSION

It is important for designers to know if crosstalk problems may arise in their final designs. An analytical expression to calculate the crosstalk would help the circuit designers to locate the

TABLE IV
COMPARISON OF CROSSTALK VALUES FOR A NEW GEOMETRY

Length (mm)	HSPICE ΔV_{RC} (mV)	HSPICE ΔV_{RLC}(mV)	MODEL ΔV_{RLC} (mV)	Error %
0.1	-163.4	-163.4	-163.4	0%
0.5	-202.2	-201.5	-202.2	0.35%
1	-214.4	-221.7	-215.3	-2.9%
2	-242.6	-263.1	-258.9	-1.6%
3	-279.3	-323	-332.9	3%
4	-319.1	-391.7	-412.3	5.3%
5	-351.3	-448.9	-474.2	5.6%
6	-375.4	-487	-512.8	5.3%
8	-397.6	-497.9	-534	7.3%
10	-398.5	-474.5	-513	8.1%
12	-405.1	-456.6	-495.8	8.6%
15	-405.5	-438	-464.7	6%

pair of lines which is most sensitive to crosstalk interference. The accuracy of RC models is no longer sufficient for deep submicron circuits. In this paper, a methodology has been proposed to determine the accurate electrical parameters R, L, C, G. We have shown the influence of inductive effects and proposed a corrective term in order to efficiently deal with them. The accuracy and applicability of a simple closed-form model for calculated crosstalk noise was shown.

REFERENCES

[1] M. Shoji, *Theory of CMOS Digital Circuits and Circuit Failures*. Princeton, NJ: Princeton University Press, 1992.

[2] M. Becer and I. N. Hajj, "An analytical model for delay and crosstalk estimation with application to decoupling," in *Proc. IEEE 1st Int. Symp. Quality Electron. Design*, San Jose, CA, Mar. 20–22, 2000, pp. 51–57.

[3] A. Vittal, L. H. Chen, M. Marek-Sadowska, K. P. Wang, and X. Yang, "Modeling crosstalk in resistive VLSI interconnections," in *Proc. IEEE Int. Conf. VLSI Design*, Jan. 1999, pp. 470–475.

[4] M. Kuhlmann, S. S. Sapatnekar, and K. K. Parhi, "Efficient crosstalk estimation," in *Proc. IEEE Int. Conf. Computer Design: VLSI in Computer Processors*, 1999, pp. 266–272.

[5] A. B. Kahng, S. Muddu, and D. Vidhani, "Noise and delay uncertainty studies for coupled RC interconnects," in *Proc. IEEE Int. ASIC/SOC Conf.*, 1999, pp. 3–8.

[6] J. Cong, D. Z. Pan, and P. V. Srinivas, "Improved crosstalk modeling for noise constrained interconnect optimization," in *Proc. ASP-DAC Conf.*, 2001, pp. 373–378.

[7] G. Servel and D. Deschacht, "On-chip crosstalk evaluation between adjacent interconnections," in *Proc. 7th IEEE Int. Conf. Electron., Circuits Syst.*, Dec. 2000.

[8] J. F. Legier, E. Paleczny, G. Servel, D. Deschacht, F. Huret, and P. Kennis, "Coupled line modelization of lossy adjacent interconnects with a full wave tangential vector finite element method," in *Proc. IEEE Workshop Signal Propagat. Interconnects*, Venice, Italy, May 2001.

[9] F. Huret, D. Deschacht, G. Servel, P. Paleczny, and P. Kennis, "Full wave analysis of conductor and substrate losses in high speed VLSI Interconnects," in *Proc. 30th EuMC Conf.*, Paris, France, Oct. 2000.

[10] J. Zheng, Y.-C. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent-circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 1443–1451, Sept. 2000.

[11] "OPERA2D," Vector Fields, 24 Bankside, Kindlington, Oxford, UK.

Grégory Servel received the Ph.D. degree in electrical and computer engineering from the University of Montpellier, France, in 2001.

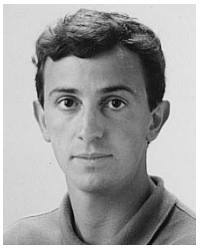
His research activities concerned the parasitic effect due to interconnections. He is currently with Silvaco Research Center, Grenoble, France.

Denis Deschacht received the M.S. and Ph.D. degrees in solid state physics from the University of Montpellier, France, in 1979 and 1984, respectively. His Ph.D. work was on the effect of grain-boundary scattering on electrical properties of thin films.

In 1984, he joined the Laboratory of Automatics and Microelectronics of Montpellier, as a CNRS Researcher. Since 1996, he has been Director of Research and is Program Leader of a French research group on interconnection with the objective to modelize, characterize, and build guidelines for handling propagation and crosstalk effect and all integrity problem.

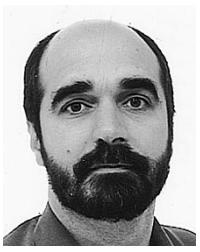
Françoise Saliou was born in Lannion, France, in 1975. She received the M.S. degree in electronics from the University of Brest, France, in 1999, where she is currently pursuing the Ph.D. degree at the Laboratory for Electronics and Communication Systems.

Her current research activities include the superconductor materials processing and its application in microwave circuits. Moreover, the theoretical approach of microwave devices and VLSI circuits, such as designing problems, are under interest.



Jean-Luc Mattei was born in France, in 1961. He received the Ph.D. degree in solid state physics from the University Joseph Fourier, Grenoble, France, in 1990.

He is currently Assistant Professor in the Electronic Department, University of Brest, and a member of the Laboratoire d'Electronique et des Systèmes de Télécommunications (LEST, UMR CNRS 6165). His main research activities deal with the study of granulars materials for applications in the microwave range. He is also interested in the modeling of electromagnetic fields in other structures, such as in digital electronic circuits.



Fabrice Huret received the Ph.D. degree in electronics from the University of Lille, Villeneuve d'Ascq, France, in 1991.

In 1992, he became an Assistant Professor at the Electromagnetic and Circuits Group, Institut d'Electronique et de Microélectronique du Nord (IEMN), University of Lille. In 2000, he joined the University of Bretagne Occidentale as a Professor. He is currently the Group Leader of the Materials Engineering and Microwave Devices Group, Laboratoire d'Electronique et Systèmes de Télécommunications (LEST). He is involved in the modelization of ULSI interconnects, new substrate materials and their effects on microwave circuits, microwave circuits for telecommunication systems.