Experimental test infrastructure supporting IEEE 11494 Standard

Uroš Kač, Franc Novak, Jozef Stefan, Florence Azaïs, Pascal Nouet, Michel Renovell

Experimental test infrastructure supporting IEEE 1149.4 Standard

Uroš Kač, Franc Novak
Jozef Stefan Institute, Ljubljana, Slovenia
Florence Azaïs, Pascal Nouet, Michel Renovell
LIRMM, University of Montpellier, France

1. Introduction

The IEEE 1149.4 standard for a mixed-signal test bus (Dot4) [1], which addresses the application of boundary-scan test techniques in mixed analog / digital circuits, was adopted already in 1999. However, major electronic manufacturers, with few exceptions [2], do not seem very keen to include Dot4 support into their products. It is our belief that wider acceptance of Dot 4 mixed-signal test bus will only come with the demonstration of its benefits in actual designs and the presentation of innovative and efficient applications of the Dot 4 infrastructure [3, 4]. To support development and evaluation of Dot4 based test and measurement procedures we decided to design and implement a series of experimental Dot 4 chips to serve as technology demonstrator vehicles.

2. Dot 4 test chip implementation

The test chip design was approached in two stages. A preliminary chip adherent to IEEE 1149.4 Standard guidelines was first designed, which would allow us to assess the characteristics of implemented mixed-signal cells (Analog Boundary Module - ABM, Test Bus Interface Circuit - TBIC) and identify possible design inefficiencies and necessary modifications.

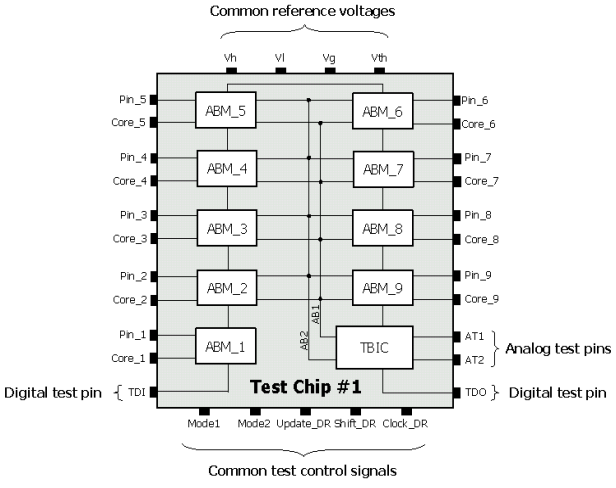

Figure 1: Preliminary test chip block diagram

The design follows schematic representations of the analog boundary scan register modules as proposed by the standard. In order to simplify the design only the TBIC and ABM cells, which represent key architectural features of the Dot4 standard, were implemented on-chip (Figure 1), while digital cells (TAP controller, bypass and instruction registers, decoder) were implemented with programmable logic (FPGA). Although standard cells were available for the choosen 0.8µm AMS CYE technology, realization of analog switches and comparators required particular attention. Since the test chip does not include a functional core, switches were realized as CMOS transmission gates. This provides a more generic ABMs structure applicable both on analog inputs and outputs. As a result, AMS library switch cells were slightly modified in order to reduce switch-ON resistance (Table I).

Cell	Dimensions (µm)	Surface (µm^2)	R_{ON} (Ω) at V_{DD}
TG2B (library)	16.2 x 34.5	559	1620
TG_inv (modified), integrated inverter	26.8 x 39.7	1064	750

Table I: Comparison of area and resistance between library and modified switch cell

Furthermore, standard cell comparators occupied unacceptably large silicon area, therefore a full-custom comparator was designed, which satisfies our requirements both in terms of silicon area and electrical characteristics (Table II).

Cell	Offset (µV)	A_v (dB)	V_{out} min	V_{out} max	V_{th} min	V_{th} max	Size (µm^2)
Comp01B (library)	27	87	3nV	5V	0.1V	4.4V	25000
Comparator (full custom)	92	61	17 mV	5V	0.1V	4.6V	2800

Table II: Comparison between library and full-custom comparator implementation

Digital control logic and register cells synthesis required some optimization in order to accomodate standard library cells (inv, nand2, nor2). The layout of the preliminary Dot 4 test chip featuring nine ABM cells and one TBIC, with an active area of 1980 x 1980 µm^2 and 39 pads is illustrated in Figure 2.

3. Modified Dot4 test chip

The second series of Dot4 test chips will include modifications and minor improvements in ABM cells as well as integrated on-chip digital control logic. The revised ABM design will provide better flexibility for the inclusion of ABMs into experimental Dot4 compatible

analog designs. Furthermore, implementation of additional hardware facilities within ABM cells will allow us to simulate some optional 1149.4 instructions. These will provide the means for the implementation of various alternative test and measurement procedures based on existing Dot 4 infrastructure.

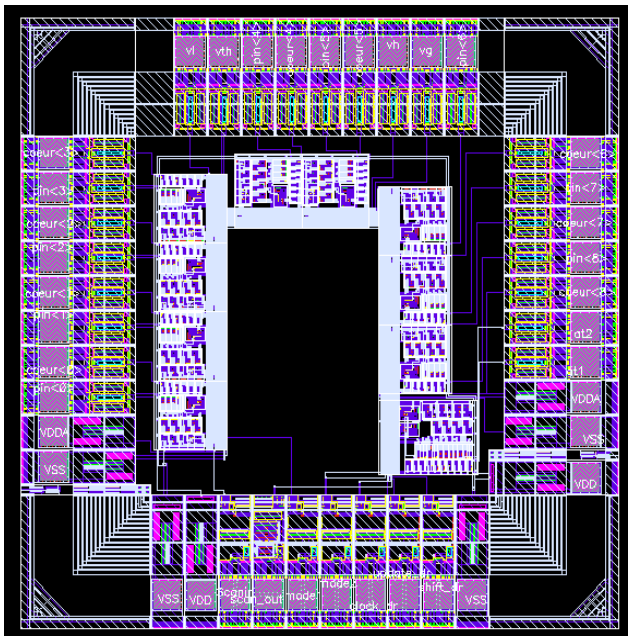

Figure 2: Preliminary test chip layout

Considering both implementation guidelines and measurement methodology proposed by the standard, we decided to apply some modifications to the ABM switching architecture. The core disconnect switch was excluded from the original cell implementation and was implemented as a separate cell consisting of a low resistance (R_{ON} < 50Ω) CMOS transmission gate.

Three modified ABM cells were also designed with additional switching resources, which allow to connect the compare voltage input of the comparator to either V_{th} or one of the V_H, V_L or V_G reference voltages (Figure 3).

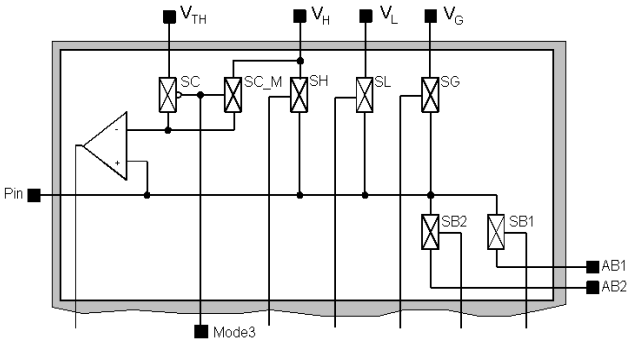

Figure 3: Modified switching architecture in ABM cell

This facility provides augmented diagnostic capabilities as it allows to distinguish between multiple input voltage levels. It could for example prove useful during test operations such as EXTEST.

Finally, the test control circuitry will be implemented on-chip, releasing valuable pad resources required by input/output control signals and simplifying the use of the Dot 4 test chip. A schematic representation of the modified test chip is illustrated in Figure 4.

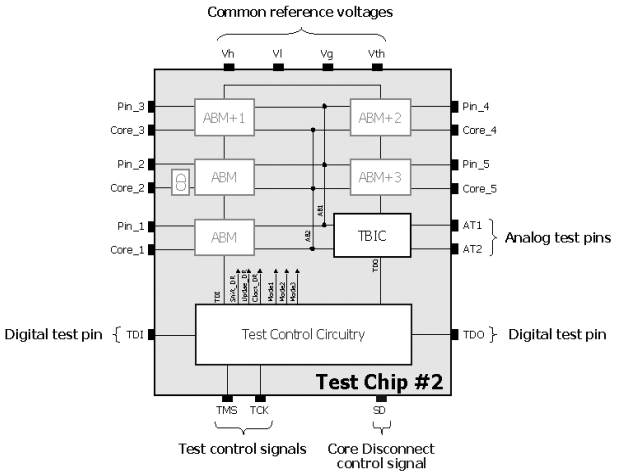

Figure 4: Block diagram of the modified Dot 4 test chip

4. Conclusion

The paper reports current results in the design, implementation and applications of an IEEE 1149.4 test chip with extended ABM functionality. The work is performed by LIRMM and JSI in the frame of the bilateral french-slovenian PROTEUS project. A first lot of the preliminary test chip version has recently become available and will allow us to evaluate the characteristics and functionality of analog and digital parts of the design before integration into the second Dot 4 chip version. Hopefully, a third version featuring a functional analog core will follow soon as the demonstrator of enhanced standard Dot4 measurement procedures as well as some alternative Dot4 based test methods.

References

[1] IEEE Standard for a Mixed-Signal Test Bus, IEEE Standard 1149.4-1999, IEEE, 1999

[2] National Semiconductor, Mixed-Signal Test and the IEEE 1149.4 Standard, http://www.national.com/appinfo/scan/

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[4] U. Kač, F. Novak, S. Maček, M.S. Zarnik, Alternative Test Methods Using IEEE 1149.4, Proc. DATE 2000, pp. 463-467.