



HAL
open science

The First IEEE International Workshop on Electronic Design, Test and Applications (DELTA 2002)

Michel Renovell, Seiji Kajihara, Ibrahim Ai-Bahadly, Serge Demidenko

► **To cite this version:**

Michel Renovell, Seiji Kajihara, Ibrahim Ai-Bahadly, Serge Demidenko (Dir.). The First IEEE International Workshop on Electronic Design, Test and Applications (DELTA 2002): 29-31 January 2002 Christchurch, New Zealand. IEEE Computer Society, 2002, 0-7695-1453-7. lirmm-00268664

HAL Id: lirmm-00268664

<https://hal-lirmm.ccsd.cnrs.fr/lirmm-00268664>

Submitted on 19 Jul 2018

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Proceedings

The First IEEE International Workshop on
Electronic Design, Test and Applications



*Cover art courtesy of Giovanni Moretti, Massey University,
Palmerston North, New Zealand. Reprinted with permission of the artist.*

Proceedings

The First IEEE International Workshop on
Electronic Design, Test and Applications
 **'2002**

29-31 January 2002
Christchurch, New Zealand

Edited by

M. Renovell, S. Kajihara, I. Al-Bahadly and S. Demidenko

Sponsored by

IEEE Computer Society Test Technology Technical Council (TTTC)
Massey University, New Zealand

In cooperation with

MOSIS, University of Southern California
SEMI—Semiconductor Equipment and Materials International
Tanner EDA—A Division of Tanner Research Inc.
University of Canterbury, New Zealand



With assistance from

IEE—Institution on Electrical Engineers
IPENZ—Institute of Professional Engineers of New Zealand



<http://computer.org>

Los Alamitos, California

Washington • Brussels • Tokyo

Copyright © 2002 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries may photocopy beyond the limits of US copyright law, for private use of patrons, those articles in this volume that carry a code at the bottom of the first page, provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

Other copying, reprint, or republication requests should be addressed to: IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 133, Piscataway, NJ 08855-1331.

The papers in this book comprise the proceedings of the meeting mentioned on the cover and title page. They reflect the authors' opinions and, in the interests of timely dissemination, are published as presented and without change. Their inclusion in this publication does not necessarily constitute endorsement by the editors, the IEEE Computer Society, or the Institute of Electrical and Electronics Engineers, Inc.

IEEE Computer Society Order Number PR01453
ISBN 0-7695-1453-7
ISBN 0-7695-1455-3 (microfiche)
Library of Congress Number 2001098179

Additional copies may be ordered from:

IEEE Computer Society
Customer Service Center
10662 Los Vaqueros Circle
P.O. Box 3014
Los Alamitos, CA 90720-1314
Tel: + 1 800 272 6657
Fax: + 1 714 821 4641
[http://computer.org/
csbooks@computer.org](http://computer.org/csbooks@computer.org)

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
Tel: + 1 732 981 0060
Fax: + 1 732 981 9667
[http://shop.ieee.org/store/
customer-service@ieee.org](http://shop.ieee.org/store/customer-service@ieee.org)

IEEE Computer Society
Asia/Pacific Office
Watanabe Bldg., 1-4-2
Minami-Aoyama
Minato-ku, Tokyo 107-0062
JAPAN
Tel: + 81 3 3408 3118
Fax: + 81 3 3408 3553
tokyo.ofc@computer.org

Editorial production by Anne Jacobs

Cover art production by Joe Daigle/Studio Productions

Printed in the United States of America by The Printing House



DELTA 2002

Table of Contents

Committees	xiii
Reviewers	xv
Message from the General Co-Chairs	xvi
Message from the Program Co-Chairs	xvii

Technical Sessions

Analog Test

Analog and Mixed-Signal IP Cores Testing	3
<i>M. W. T. Wong, K.Y. Ko, and Y.S. Lee</i>	
Testable Design and Testing of High-Speed Superconductor Microelectronics	8
<i>H. G. Kerckhoff, A. A. Joseph, and S. Heuvelmans</i>	
Observer-Based Test of Analog Linear Time-Invariant Circuits	13
<i>Z. Guo and J. Savir</i>	
Practical Oscillation-Based Test in Analog Integrated Filters: Experimental Results	18
<i>G. Huertas, D. Vazquez, A. Rueda, and J. L. Huertas</i>	
Constrained Specification-Based Test Stimulus Generation for Analog Circuits Using Nonlinear Performance Prediction Models	25
<i>S. Bhattacharya and A. Chatterjee</i>	

Communications

MIMO Transmit Optimization for Wireless Communication Systems	33
<i>R. Choi and R. Murch</i>	
Adaptive Power Control Design for Microwave Communication System	38
<i>T. A. Rahman and T. C. Leng</i>	
VSIA Interface Cosynthesis	43
<i>S. Ouadjaout, M.-F. Albenge, and D. Houzet</i>	
Bluetooth-Based Wireless Personal Area Network for Multimedia Communication	47
<i>J. Y. Khan, J. Wall, and M. A. Rashid</i>	
Multi-User Detection for CDMA Communications Based on Self Organized Neural Networks Structures	52
<i>F. Carlier, F. Nouvel, and J. Citerne</i>	

Digital Signal Processing and Architectures

An Applications-Based Approach to Measuring DSP Efficiency.....	59
<i>J. G. Chase, C. Pretty, A. Bedarida, and P. Bettler</i>	
Reconfigurable DSP's for Efficient MPEG-4 Video and Audio Decoding.....	63
<i>C. Pretty and J. G. Chase</i>	
Smart Antenna Software Radio Test System	68
<i>P. J. Green and D. P. Taylor</i>	
GALA Approach in Design of Asynchronous Control for Counterflow Pipeline Processor.....	73
<i>V. Varshavsky and V. Marakhovsky</i>	

From Low to High Level Fault Simulation and Diagnosis

Behavioral Fault Simulation: Implementation and Experiments Results	81
<i>D. Federici, P. Bisgambiglia, and J.-F. Santucci</i>	
Multi-Level Fault Simulation of Digital Systems on Decision Diagrams	86
<i>R. Ubar, J. Raik, E. Ivask, and M. Brik</i>	
Fault Simulation Method for Crosstalk Faults in Clock-Delayed Domino CMOS Circuits	92
<i>K. Shimizu, M. Takamura, T. Shirai, N. Itazaki, and K. Kinoshita</i>	

High Level Design

Research on VHDL RTL Synthesis System	99
<i>H. Zhou, Z. Lin, and W. Cao</i>	
An Accurate Coverage Forecasting Model for Behavioral Model Verification	104
<i>A. Hajjar and T. Chen</i>	
A Novel CAM/RAM Based Buffer Manager for Next Generation IP Routers	111
<i>C. Dou, S.-J. Jiang, and K.-C. Leu</i>	
Interconnect IP Node for Future System-on-Chip Designs	116
<i>I. Saastamoinen, D. Sigüenza-Tortosa, and J. Nurmi</i>	

Memory

Signal Margin Analysis for Memory Sense Amplifiers.....	123
<i>J. Vollrath</i>	
Address and Data Scrambling: Causes and Impact on Memory Tests	128
<i>A. J. van de Goor and I. Schanstra</i>	
Flash Memory Built-In Self-Test Using March-Like Algorithms.....	137
<i>J.-C. Yeh, C.-F. Wu, K.-L. Cheng, Y.-F. Chou, C.-T. Huang, and C.-W. Wu</i>	
A Method for Storing Fail Bit Maps in Burn-In Memory Testers.....	142
<i>A. Iseño and Y. Iguchi</i>	

Power Issues in Design and Test

Coup de Fouet Based VRLA Battery Capacity Estimation	149
<i>P. E. Pascoe, H. Sirisena, and A. H. Anbuky</i>	
Power Optimization of Combinational Circuits by Input Transformations	154
<i>C. Gopalakrishnan and S. Katkooi</i>	
Reducing Test Power During Test Using Programmable Scan Chain Disable	159
<i>R. Sankaralingam and N. A. Toubia</i>	

Sensor and Analog Design

Test Socket Chip for Measuring Dark Current in IR FPA	167
<i>M. L. Sheu, T. P. Sun, and F.-W. Jih</i>	
A Low Power High Speed Class-B Buffer Amplifier for Flat Panel Display Application	172
<i>C.-W. Lu and C. L. Lee</i>	
Design of a Low-Voltage Instrumentation Amplifier for Enzyme-Extended-Gate Field Effect Transistor Based Urea Sensor Application	177
<i>W.-Y. Chung, M.-H. Yeh, J.-C. Chen, S.-K. Hsiung, D. G. Pijanowska, W. Torbicz, J.-C. Chou, and T.-P. Sun</i>	
A Silicon Piezoresistive Pressure Sensor	181
<i>R. Singh, L. L. Ngo, H. S. Seng, and F. N. C. Mok</i>	

Special Session on Education

Evolution of the MOSIS VLSI Educational Program	187
<i>C. A. Piña</i>	
The Search for Design in Electrical Engineering Education	192
<i>D. V. Kerns, S. E. Kerns, G. A. Pratt, M. H. Somerville, and J. D. Crisman</i>	
The Development and Transfer of Advanced Technology from Universities to Industry	197
<i>R. M. Hodgson</i>	
Competencies of BSc and MSc Programmes in Electrical Engineering and Student Portfolios	203
<i>T. J. Mouthaan, R.W. Brink, and H. Vos</i>	
Electronics Education: A Systems Based Mechatronic Approach	209
<i>D. A. Carnegie</i>	
Boundary Scan as a Test Solution in Microelectronics Curricula	214
<i>A. Rucinski and B. Dziurla-Rucinska</i>	
Making ATE Accessible for Academic Institutions	219
<i>W. Moorhead and S. Demidenko</i>	
Teaching Integrated Circuit and Semiconductor Device Design in New Zealand: The University of Canterbury Approach	223
<i>R. J. Blaikie, M. M. Alkaisi, S. M. Durbin, and D. R. S. Cumming</i>	

European Network for Test Education.....	230
<i>Y. Bertrand, M.-L. Flottes, F. Azaïs, S. Bernard, L. Latorre, and R. Lorival</i>	
PARTOS-11: An Efficient Real-Time Operating System for Low-Cost Microcontrollers.....	235
<i>Y. Li and P. Wilson</i>	
Design of a Processor to Support the Teaching of Computer Systems	240
<i>M. Pearson, D. Armstrong, and T. McGregor</i>	
Applied Science (Electronics) at the University of Otago	245
<i>J. L. Bähr</i>	
Harnessing Geographically Distributed Cooperation in Microtechnology Course at Massey University	250
<i>R. Browne, S. Demidenko, and R. O'Driscoll</i>	
Special Session on Electromagnetics and Control	
Design of an Auxiliary Power Distribution Network for an Electric Vehicle	257
<i>W. Chen, S. Round, and R. Duke</i>	
Analysis of Position Estimation Method for Switched Reluctance Drives	262
<i>I. H. Al-Bahadly</i>	
Conceptual Design of an All Superconducting Mini Power Plant Model	267
<i>I. Vajda</i>	
Magnetic Hysteresis Modeling of Electronic Components	272
<i>H. Hauser, P. Fulmek, F. Himmelstoss, T. Wolbank, R. Wöhrnschimmel, and P. Wurm</i>	
Computer Based Real-Time Simulator for Renewable Energy Converters	280
<i>D. Parker</i>	
Special Session on FPGA	
On Biologically-Inspired Design of Fault-Tolerant Digital Systems.....	287
<i>P. K. Lala and K. K. Bondali</i>	
On-Line Diagnosis and Reconfiguration of FPGA Systems	291
<i>A. Antola, V. Piuri, and M. Sami</i>	
Testing the Unidimensional Interconnect Architecture of Symmetrical SRAM-Based FPGA.....	297
<i>M. Renovell, P. Faure, P. Prinetto, and Y. Zorian</i>	
A Fault-Tolerant FPGA-Based Multi-Stage Interconnection Network for Space Applications	302
<i>M. Alderighi, F. Casini, S. D'Angelo, D. Salvi, and G. R. Sechi</i>	

Special Session on Image Processing

FPGA-Based Implementation of Variable Sized Structuring Elements for 2D Binary Morphological Operations	309
<i>J. Velten and A. Kummert</i>	
FPGA Implementation of a Neural Network for a Real-Time Hand Tracking System	313
<i>M. Krips, T. Lammert, and A. Kummert</i>	
Neural Networks to Solve the Problems of Control and Identification.....	318
<i>S. Demidenko, R. K. Sadykhov, L. P. Podenok, M. E. Vatkin, and A. N. Klimovich</i>	
On the Initialization and Training Methods for Kohonen Self-Organizing Feature Maps in Color Image Quantization	321
<i>X. Rui, C.-H. Chang, and T. Srikanthan</i>	
An Architecture for High Speed Ultrasound Image Capture and Real-Time 3D Reconstruction	326
<i>S. Sanei and T. K. M. Lee</i>	

Special Session on Robotics

Genetic Algorithm Application to Vibration Control of Tall Flexible Structures	333
<i>S. Kundu, K. Seto, and S. Sugino</i>	
State Transition Based Supervisory Control for a Robot Soccer System	338
<i>G. Sen Gupta, C. H. Messom and H. L. Sng</i>	
A Semi-Generic System for the Control of Autonomous Mobile Mechatrons	343
<i>D. A. Carnegie</i>	
Strategy for Collaboration in Robot Soccer	347
<i>H. L. Sng, G. Sen Gupta, and C. H. Messom</i>	

Special Session on Submicron Technology

A Novel Analytical Model for Evaluation of Substrate Crosstalk in VLSI Circuits	355
<i>N. Masoumi, M. I. Elmasry, S. Safavi-Naeini, and H. Hadi</i>	
A Comprehensive Fault Model for Deep Submicron Digital Circuits	360
<i>J. A. Abraham, A. Krishnamachary, and R. S. Tupuri</i>	
Noise Analysis under Capacitive and Inductive Coupling for High Speed Circuits	365
<i>S. H. Choi and K. Roy</i>	
Noise—Its Sources, and Impact on Design and Test of Mixed Signal Circuits	370
<i>M. d'Abreu</i>	

Test Generation and Compaction

Properties of Output Sequences and Their Use in Guiding Property-Based Test Generation for Synchronous Sequential Circuits	377
<i>I. Pomeranz and S. M. Reddy</i>	
Path-Oriented Test Data Generation of Behavioral VHDL Description	382
<i>C. Paoli, M.-L. Nivet, J.-F. Santucci, and A. Campana</i>	
Random Pattern Testability of the Open Defect Detection Method Using Application of Time-Variable Electric Field	387
<i>H. Yotsuyanagi, M. Hashizume, T. Iwakiri, M. Ichimiya, and T. Tamesada</i>	
A Method of Static Test Compaction Based on Don't Care Identification	392
<i>K. Miyase, S. Kajihara, and S. M. Reddy</i>	
Generating Small Test Sets for Test Compression / Decompression Scheme Using Statistical Coding	396
<i>H. Ichihara and T. Inoue</i>	

Test Techniques and Methodologies

I _{DDT} Test Methodologies for Very Deep Sub-Micron CMOS Circuits	403
<i>A. Chehab, R. Makki, M. Spica, and D. Wu</i>	
A Functional Approach to Test Cascaded BCD Counters	408
<i>G. Peretti, E. Romero, F. Salvático, and C. Marqués</i>	
Test Data Compression Using Don't-Care Identification and Statistical Encoding	413
<i>S. Kajihara, K. Taniguchi, I. Pomeranz, and S. M. Reddy</i>	
On C-Testability of Carry Free Dividers	417
<i>S. M. Aziz and S. J. Carr</i>	

Poster Papers

Modeling of a Repulsive Type Magnetic Bearing for Five Axis Control under Intermittent Operation Including Eddy Current Effect	425
<i>S. C. Mukhopadhyay</i>	
A Novel Compound Type Resonant Rectifier Topology	428
<i>C. Chakraborty and S. C. Mukhopadhyay</i>	
Modifying Test Vectors for Reducing Power Dissipation in CMOS Circuits	431
<i>Y. Higami, S. Kobayashi, and Y. Takamatsu</i>	
Minimization and Partitioning Method Reducing Input Sets	434
<i>J. Hlavicka and P. Fiser</i>	
Stand-Alone Digital Real-Time Image Processing Board Based on an FPGA	437
<i>M. Pieper and A. Kummert</i>	
Transmission of Data/Sketch through Telephone Lines using Gapping Technique via a Low Cost Telewriting Equipment	440
<i>Z. B. K. Mastan, A. Ghazali, and M. M. Idris</i>	

Enhancing the Static D.C. Fault Diagnosis of a Resistance Temperature Detector Sensor Circuit Using Equivalent Fault Analysis	443
<i>M. Worsman, M. W. T. Wong, and Y. S. Lee</i>	
Test Power: A Big Issue in Large SOC Designs	447
<i>Y. Bonhomme, P. Girard, C. Landrault, and S. Pravossoudovitch</i>	
Multi-Carrier CDMA over Copper Lines—Comparison of Performances with the ADSL System	450
<i>S. Mallier, F. Nouvel, J.-Y. Baudais, D. Gardan, and A. Zeddani</i>	
Multivariable Predictive Feedback Control	453
<i>L. L. Giovanini</i>	
Power Supply Circuit for High Speed Operation of Adiabatic Dynamic CMOS Logic Circuits	459
<i>M. Hashizume, M. Sato, H. Yotsuyanagi, and T. Tamesada</i>	
Monitoring Parallel Interfaces in System Environment	462
<i>J. Sosnowski and K. Szafran</i>	
Pipelining Extended Givens Rotation RLS Adaptive Filters	466
<i>S. Tenqchen, J.-H. Chang, W.-S. Feng, and B.-S. Jeng</i>	
A Flexible Embedded SRAM Compiler	474
<i>Y. Liu, Z. Gao, and X. He</i>	
Advanced Instruction Set Architectures for Reducing Program Memory Usage in a DSP Processor	477
<i>P. Simonen, I. Saastamoinen, M. Kuulusa, and J. Nurmi</i>	
Sensorless Speed Control in Induction Motor Drives	480
<i>W. Phipps and I. Al-Bahadly</i>	
A High Voltage Amplifier for Use in Medical Applications of Electroporation	483
<i>P. Gaynor and J. Skipwith</i>	
A Simple Microcontroller Based Digital Lock-In Amplifier for the Detection of Low Level Optical Signals	486
<i>A. A. Dorrington and R. Künnemeyer</i>	
An Intelligent System for Odour Discrimination	489
<i>R. Singh</i>	
Test Chirp Signal Generation Using Spectral Warping	492
<i>W. Allen, D. Bailey, S. Demidenko, and V. Piuri</i>	
A New Transitive Closure Algorithm with Application to Redundancy Identification	496
<i>V. Gaur, V. D. Agrawal, and M. L. Bushnell</i>	
Test Bed for Number Plate Recognition Applications	501
<i>D. G. Bailey, D. Irecki, B. K. Lim, and L. Yang</i>	
A Synthesizable VHDL Model for an Easily Testable Generalised Multiplier	504
<i>S. M. Aziz, C. M. Basheer, and J. Kamruzzaman</i>	

A Comparison of Genetic Programming and Genetic Algorithms for Auto-Tuning Mobile Robot Motion Control	507
<i>M. Walker and C. H. Messom</i>	
Author Index	511
TTTC: Test Technology Technical Council	515