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The Systolic Ring: A Scalable Dynamically Reconfigurable Core for Embedded Systems

Pascal Benoit, Gilles Sassatelli, Michel Robert, Lionel Torres, Gaston Cambon,
Thierry Gil

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Pascal Benoit, Gilles Sassatelli, Michel Robert, Lionel Torres, Gaston Cambon, et al.. The Systolic Ring: A Scalable Dynamically Reconfigurable Core for Embedded Systems. SAME 2002 - Sophia-Antipolis Forum on MicroElectronics, Oct 2002, Sophia-Antipolis, France. pp.85-90, 2002. <lirmm-00269322>

HAL Id: lirmm-00269322

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Submitted on 10 Oct 2023

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HAL Authorization

Application example - DCT 2D 8*8

64*64 image example - Comparisons

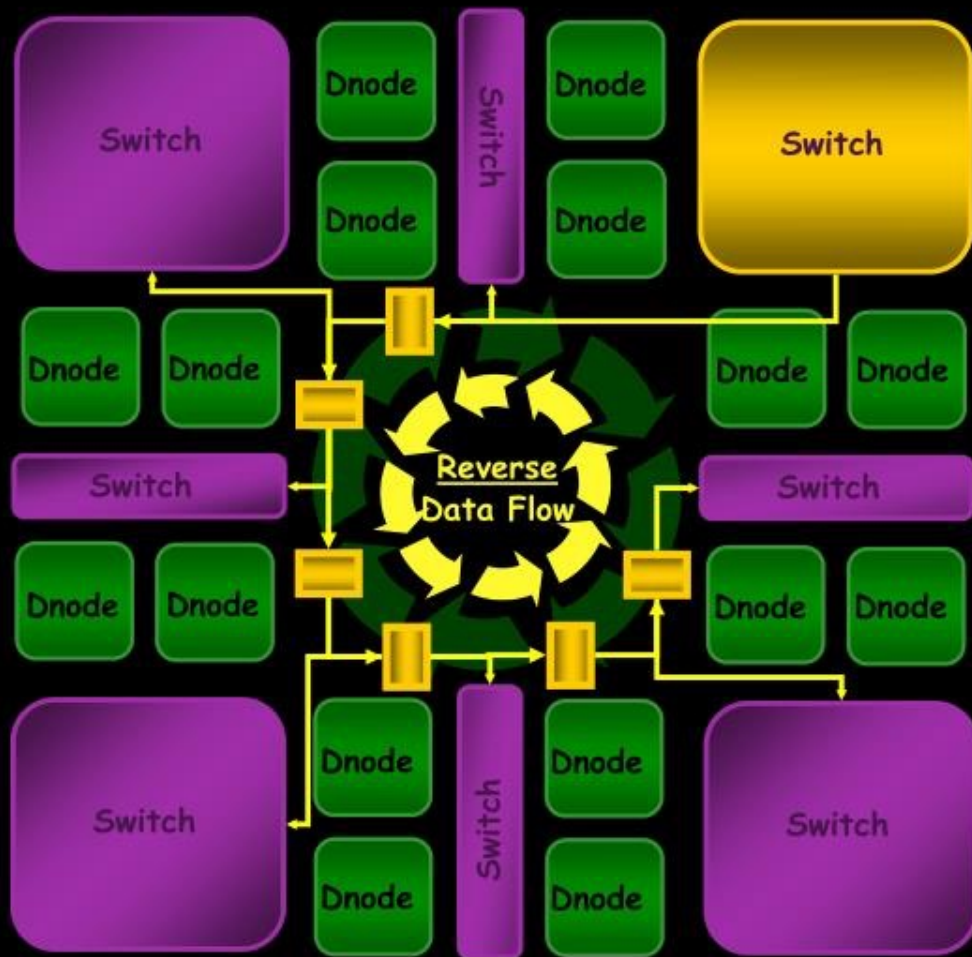
	Pentium IV Intel	DCT Core Xilinx	TMS320C62 TI	RING-16	RING-64
Cycles #	21248	4171	10240	5120	1280
f (MHz)	1200	80*	300	200	200
Proc. Time (μs)	17.7	52.1	34.1	12.8	6.4
Comment	SSE2	*Device dependant	Matrix	Even-Odd decomposition	
Type	Super scalar	Fine Grain Reconfigurable	VLIW	Coarse Grain Reconfigurable	



Only Processing time !!

The Systolic Ring - Operative Layer Topology

Data Flows



Forward Data Flow

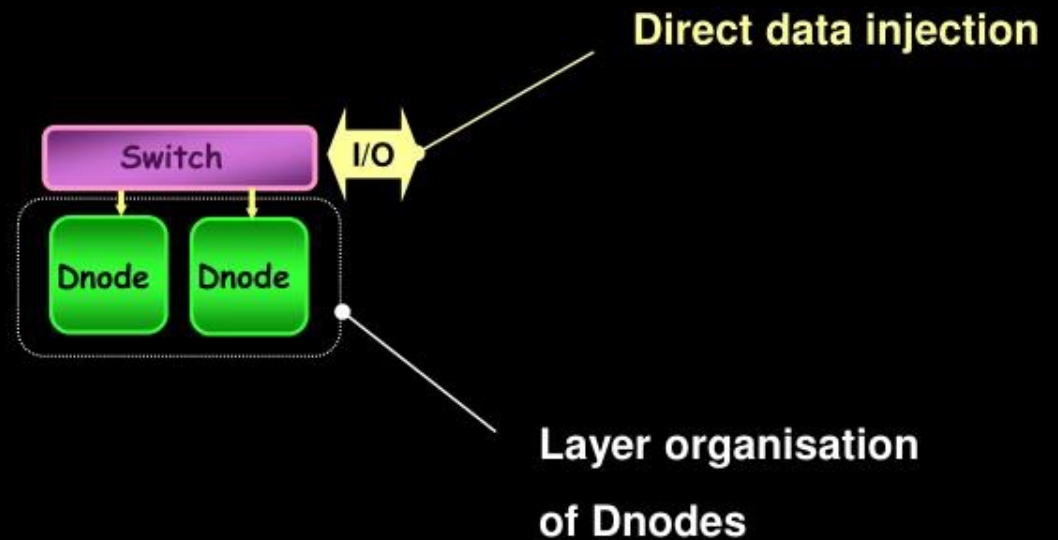
Unidirectional data transit between successive layers (circular pipeline)

Reverse Data Flow

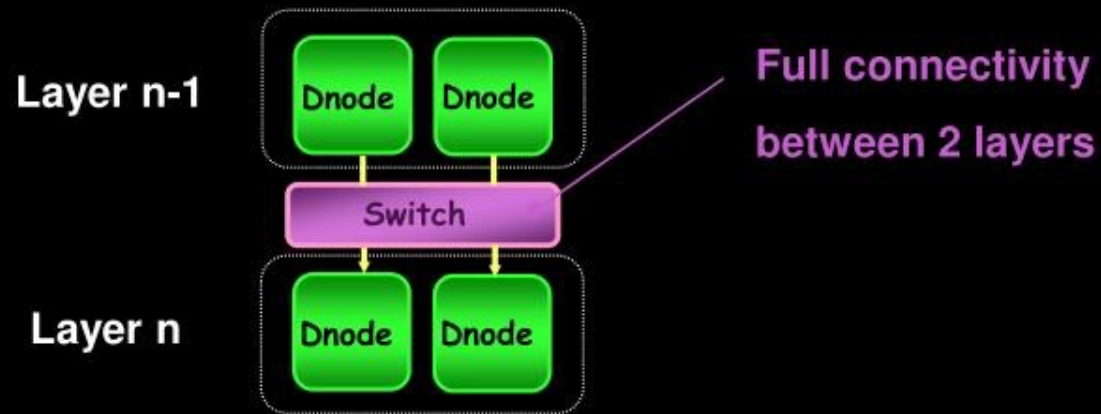
Feedback pipeline network for recursive algorithms

The Systolic Ring - Dnode Clusters

Macro Node



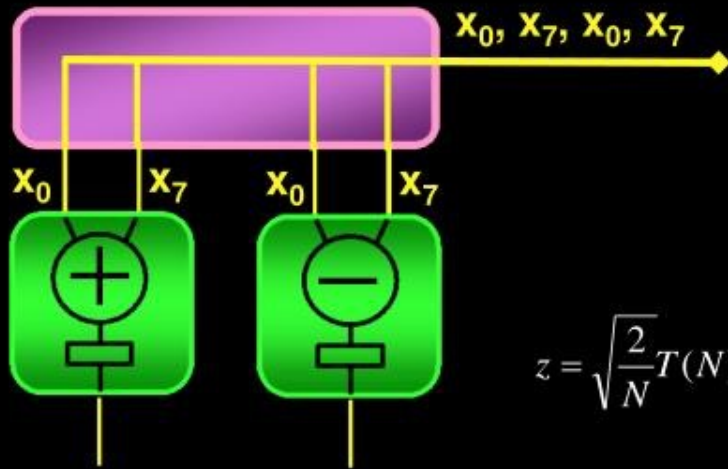
The Systolic Ring - Switch components





Thank You

Application example - 8*8 2D DCT



Cycle 0

$$z = \sqrt{\frac{2}{N}} T(N)x$$

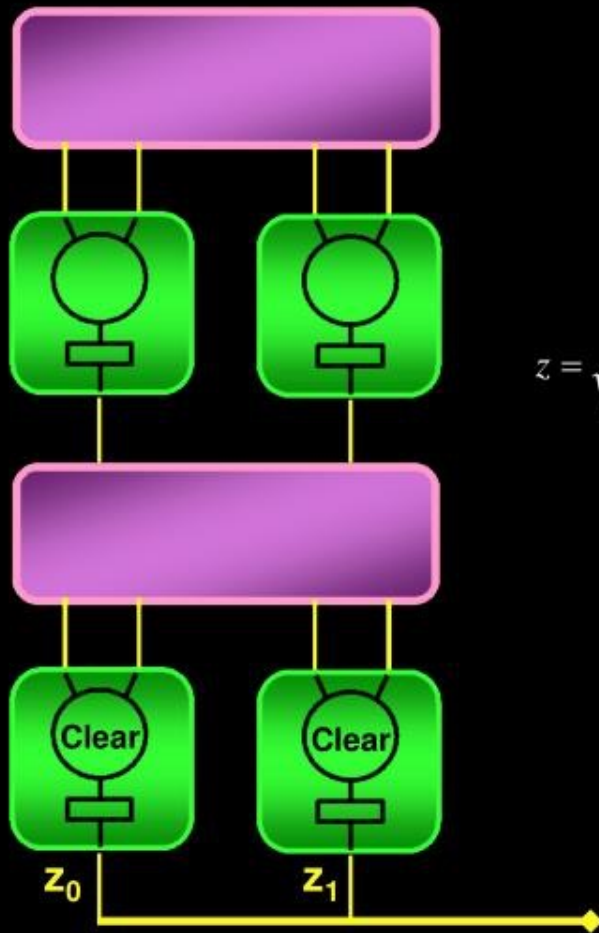
$$\begin{cases} \begin{bmatrix} z_0 \\ z_2 \\ z_4 \\ z_6 \end{bmatrix} = \begin{bmatrix} 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} \\ \beta & \delta & -\delta & -\beta \\ \alpha & -\alpha & -\alpha & \alpha \\ \delta & -\beta & \beta & -\delta \end{bmatrix} \begin{bmatrix} x_0 + x_7 \\ x_1 + x_6 \\ x_2 + x_5 \\ x_3 + x_4 \end{bmatrix} \\ \begin{bmatrix} z_1 \\ z_3 \\ z_5 \\ z_7 \end{bmatrix} = \begin{bmatrix} \lambda & \gamma & \mu & \nu \\ \gamma & -\nu & -\lambda & -\mu \\ \mu & -\lambda & \nu & \gamma \\ \nu & -\mu & \gamma & -\lambda \end{bmatrix} \begin{bmatrix} x_0 - x_7 \\ x_1 - x_6 \\ x_2 - x_5 \\ x_3 - x_4 \end{bmatrix} \end{cases}$$

$$\begin{cases} \alpha = 1/2 \cos(\pi/4) \\ \beta = 1/2 \cos(\pi/8) \\ \delta = 1/2 \sin(\pi/8) \\ \lambda = 1/2 \cos(\pi/16) \\ \gamma = 1/2 \cos(3\pi/16) \\ \mu = 1/2 \sin(3\pi/16) \\ \nu = 1/2 \sin(\pi/16) \end{cases}$$

Application example - 8*8 2D DCT



Cycle 5



$$z = \sqrt{\frac{2}{N}} T(N)x$$

$$\begin{cases} \begin{bmatrix} z_0 \\ z_2 \\ z_4 \\ z_6 \end{bmatrix} = \begin{bmatrix} 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} \\ \beta & \delta & -\delta & -\beta \\ \alpha & -\alpha & -\alpha & \alpha \\ \delta & -\beta & \beta & -\delta \end{bmatrix} \begin{bmatrix} x_0 + x_7 \\ x_1 + x_6 \\ x_2 + x_5 \\ x_3 + x_4 \end{bmatrix} \\ \begin{bmatrix} z_1 \\ z_3 \\ z_5 \\ z_7 \end{bmatrix} = \begin{bmatrix} \lambda & \gamma & \mu & \nu \\ \gamma & -\nu & -\lambda & -\mu \\ \mu & -\lambda & \nu & \gamma \\ \nu & -\mu & \gamma & -\lambda \end{bmatrix} \begin{bmatrix} x_0 - x_7 \\ x_1 - x_6 \\ x_2 - x_5 \\ x_3 - x_4 \end{bmatrix} \end{cases}$$

$$\begin{cases} \alpha = 1/2 \cos(\pi/4) \\ \beta = 1/2 \cos(\pi/8) \\ \delta = 1/2 \sin(\pi/8) \end{cases}$$

$$\begin{cases} \lambda = 1/2 \cos(\pi/16) \\ \gamma = 1/2 \cos(3\pi/16) \\ \mu = 1/2 \sin(3\pi/16) \\ \nu = 1/2 \sin(\pi/16) \end{cases}$$

**2 transformed samples
computed each 5 clock cycles**



8*8 2D transformed samples each 320 clock cycles

Conclusion



■ DESIGN

- Reconfigurable IP Core for SoC
- Assembling Software
- RING-8 prototype

■ FEATURES

- Customisable IP Core
- Good performance / area trade-off : *Ring-8@200MHz (0.18 μ)*

3.3 mm²

1600 MIPS

Results for DCT, Wavelet Transform, Motion Estimation

Application example - 8*8 2D DCT



Even-Odd frequency decomposition

$$z = \sqrt{\frac{2}{N}} T(N) x$$

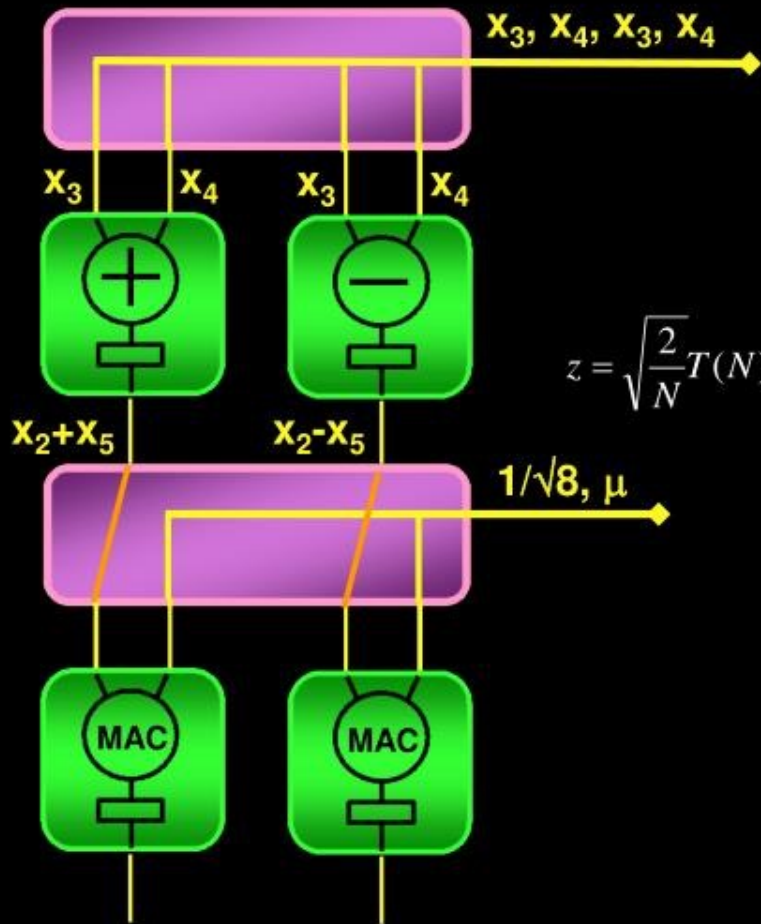
$$\begin{cases} \begin{bmatrix} z_0 \\ z_2 \\ z_4 \\ z_6 \end{bmatrix} = \begin{bmatrix} 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} \\ \beta & \delta & -\delta & -\beta \\ \alpha & -\alpha & -\alpha & \alpha \\ \delta & -\beta & \beta & -\delta \end{bmatrix} \begin{bmatrix} x_0 + x_7 \\ x_1 + x_6 \\ x_2 + x_5 \\ x_3 + x_4 \end{bmatrix} \\ \begin{bmatrix} z_1 \\ z_3 \\ z_5 \\ z_7 \end{bmatrix} = \begin{bmatrix} \lambda & \gamma & \mu & \nu \\ \gamma & -\nu & -\lambda & -\mu \\ \mu & -\lambda & \nu & \gamma \\ \nu & -\mu & \gamma & -\lambda \end{bmatrix} \begin{bmatrix} x_0 - x_7 \\ x_1 - x_6 \\ x_2 - x_5 \\ x_3 - x_4 \end{bmatrix} \end{cases}$$

$$\begin{cases} \alpha = 1/2 \cos(\pi/4) \\ \beta = 1/2 \cos(\pi/8) \\ \delta = 1/2 \sin(\pi/8) \end{cases}$$

$$\begin{cases} \lambda = 1/2 \cos(\pi/16) \\ \gamma = 1/2 \cos(3\pi/16) \\ \mu = 1/2 \sin(3\pi/16) \\ \nu = 1/2 \sin(\pi/16) \end{cases}$$

Independent Matrix Products (//)

Application example - 8*8 2D DCT



Cycle 3

$$z = \sqrt{\frac{2}{N}} T(N)x$$

$$\begin{bmatrix} z_0 \\ z_2 \\ z_4 \\ z_6 \end{bmatrix} = \begin{bmatrix} 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} \\ \beta & \delta & -\delta & -\beta \\ \alpha & -\alpha & -\alpha & \alpha \\ \delta & -\beta & \beta & -\delta \end{bmatrix} \begin{bmatrix} x_0 + x_7 \\ x_1 + x_6 \\ x_2 + x_5 \\ x_3 + x_4 \end{bmatrix}$$

$$\begin{bmatrix} z_1 \\ z_3 \\ z_5 \\ z_7 \end{bmatrix} = \begin{bmatrix} \lambda & \gamma & \mu & \nu \\ \gamma & -\nu & -\lambda & -\mu \\ \mu & -\lambda & \nu & \gamma \\ \nu & -\mu & \gamma & -\lambda \end{bmatrix} \begin{bmatrix} x_0 - x_7 \\ x_1 - x_6 \\ x_2 - x_5 \\ x_3 - x_4 \end{bmatrix}$$

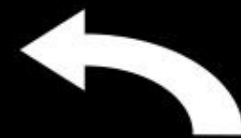
$$\begin{cases} \alpha = 1/2 \cos(\pi/4) \\ \beta = 1/2 \cos(\pi/8) \\ \delta = 1/2 \sin(\pi/8) \end{cases}$$

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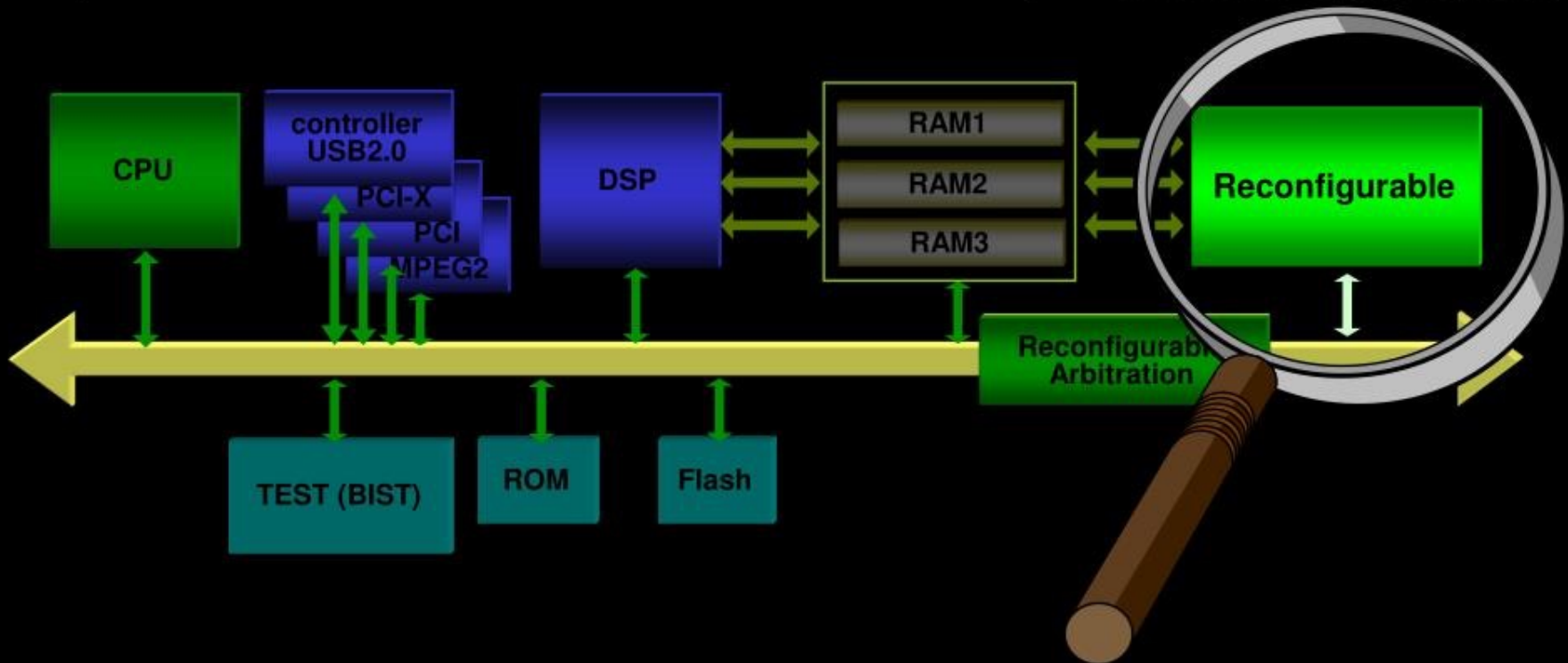
Introduction



Multimedia
Data flow oriented applications



RECONFIGURATION
HARDWARE Static / Dynamic



Introduction

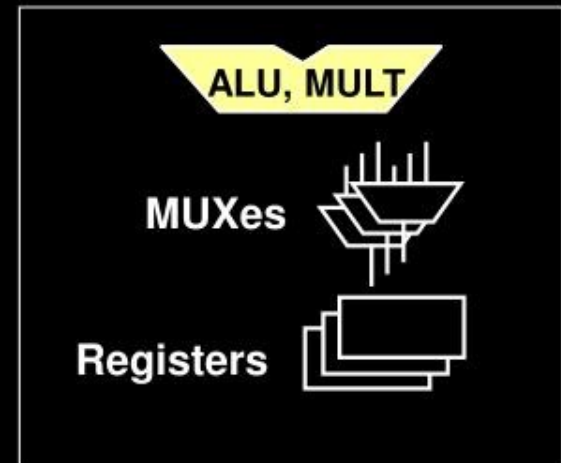
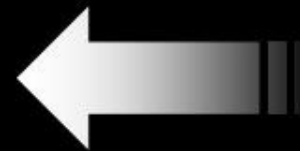
What kind of base block is suitable for Multimedia?

- **Coarse Grain:**

- Granularity: WORD

- adapted to DSP, data flow oriented processing

**SYSTOLIC
RING**



Coarse Grain

Dynamically Reconfigurable
Architecture

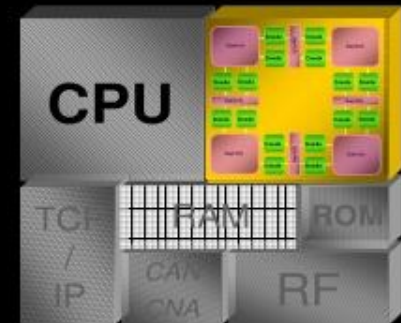
- Low reconfiguration over-cost
- High level of performances

Outline

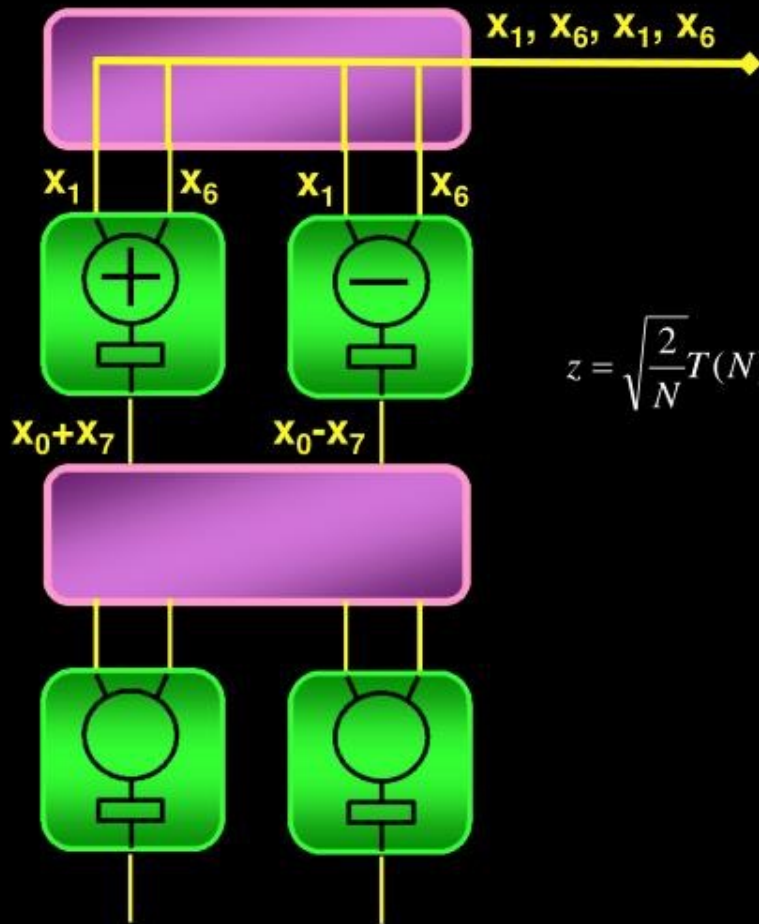


The Systolic Ring : A Scalable Dynamically Reconfigurable Core for Embedded Systems

- **The Systolic Ring**
 - Building Block
 - Operative Layer Topology
 - System Overview
 - Features
- **Application Example**
 - 8*8 2D DCT
 - Structural Mapping
 - Performance Comparisons
- **Conclusion**



Application example - 8*8 2D DCT



$$z = \sqrt{\frac{2}{N}} T(N)x$$

$$\begin{bmatrix} z_0 \\ z_2 \\ z_4 \\ z_6 \end{bmatrix} = \begin{bmatrix} 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} \\ \beta & \delta & -\delta & -\beta \\ \alpha & -\alpha & -\alpha & \alpha \\ \delta & -\beta & \beta & -\delta \end{bmatrix} \begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \end{bmatrix} \begin{matrix} x_7 \\ x_6 \\ x_5 \\ x_4 \end{matrix}$$

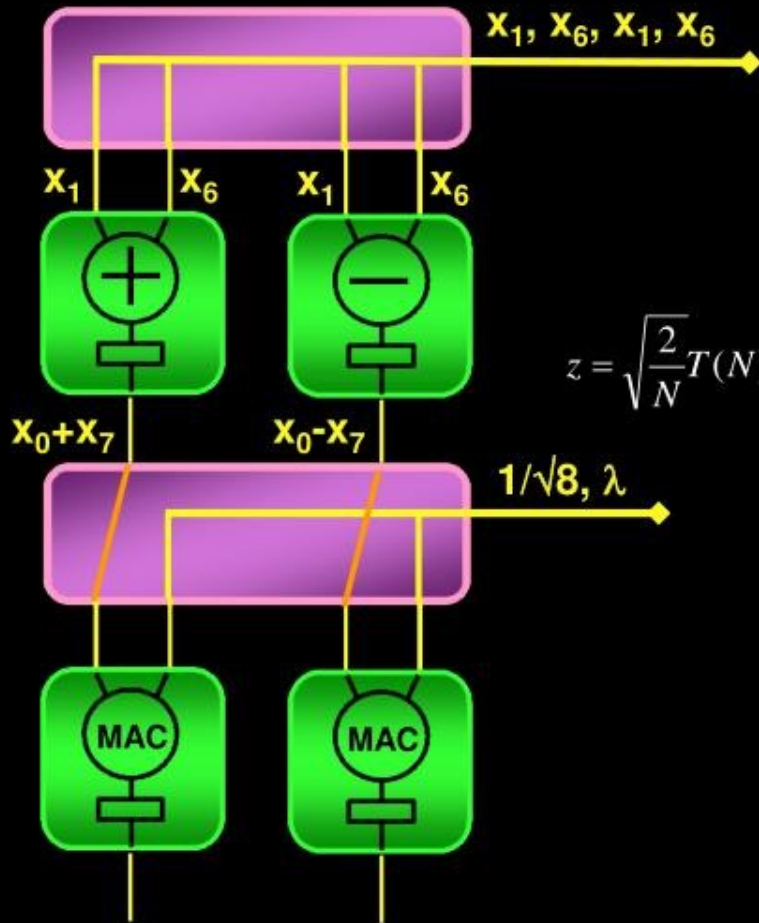
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Row-Column product -> MAC operations

Application example - 8*8 2D DCT



Cycle 1

$$z = \sqrt{\frac{2}{N}} T(N)x$$

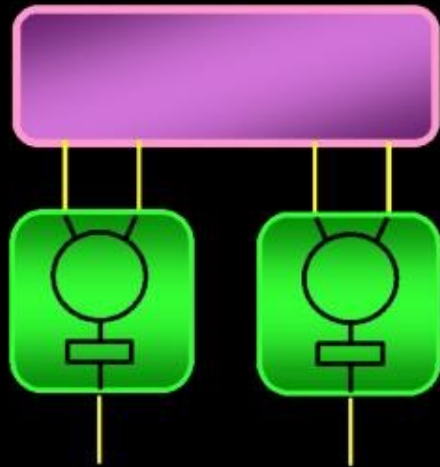
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$$\begin{bmatrix} z_1 \\ z_3 \\ z_5 \\ z_7 \end{bmatrix} = \begin{bmatrix} \lambda & \gamma & \mu & v \\ \gamma & -v & -\lambda & -\mu \\ \mu & -\lambda & v & \gamma \\ v & -\mu & \gamma & -\lambda \end{bmatrix} \begin{bmatrix} x_0 - x_7 \\ x_1 - x_6 \\ x_2 - x_5 \\ x_3 - x_4 \end{bmatrix}$$

$$\begin{cases} \alpha = 1/2 \cos(\pi/4) \\ \beta = 1/2 \cos(\pi/8) \\ \delta = 1/2 \sin(\pi/8) \end{cases}$$

$$\begin{cases} \lambda = 1/2 \cos(\pi/16) \\ \gamma = 1/2 \cos(3\pi/16) \\ \mu = 1/2 \sin(3\pi/16) \\ v = 1/2 \sin(\pi/16) \end{cases}$$

Application example - 8*8 2D DCT



Addition & Subtraction of image samples

$$z = \sqrt{\frac{2}{N}} T(N)x$$

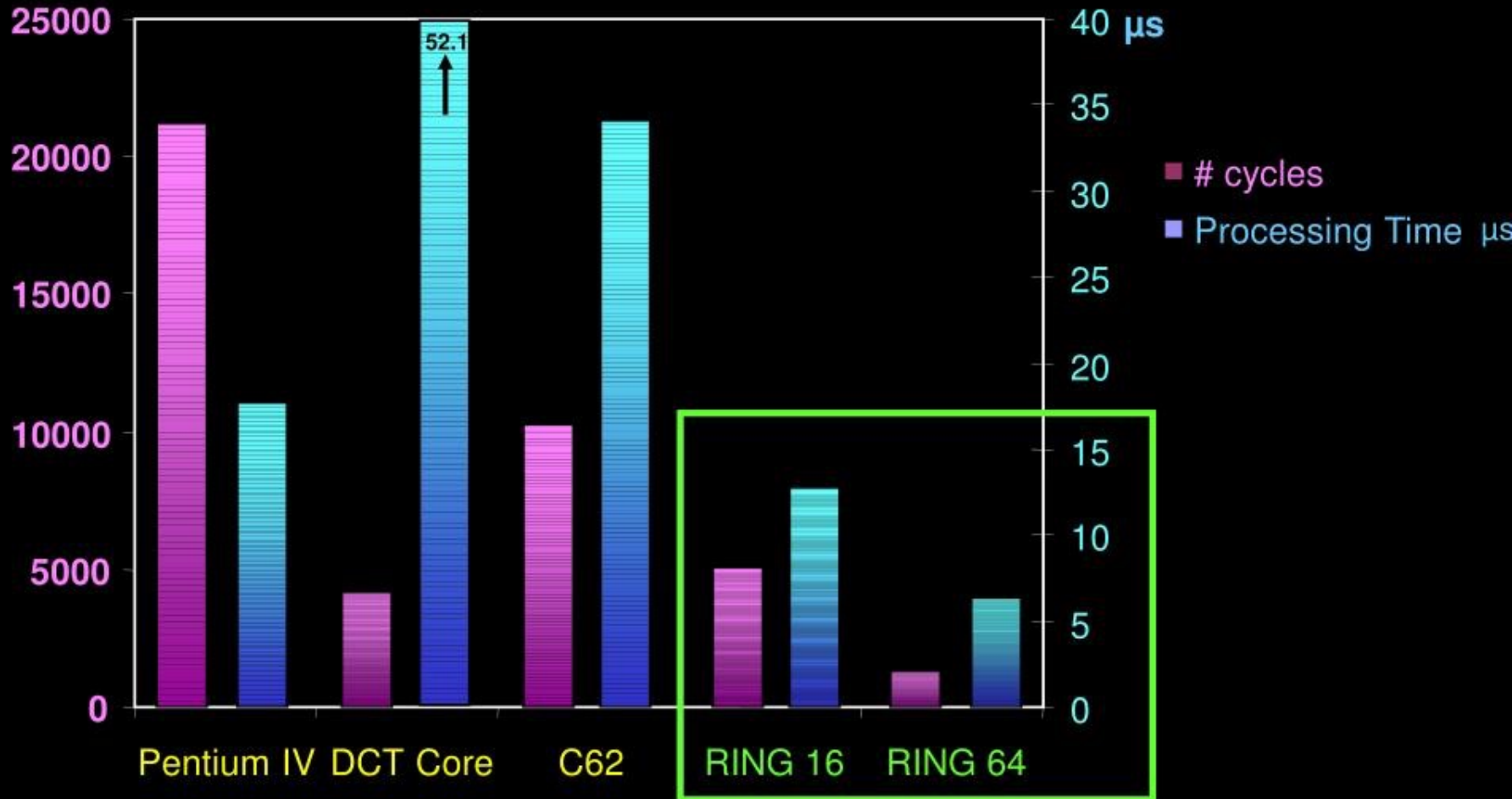
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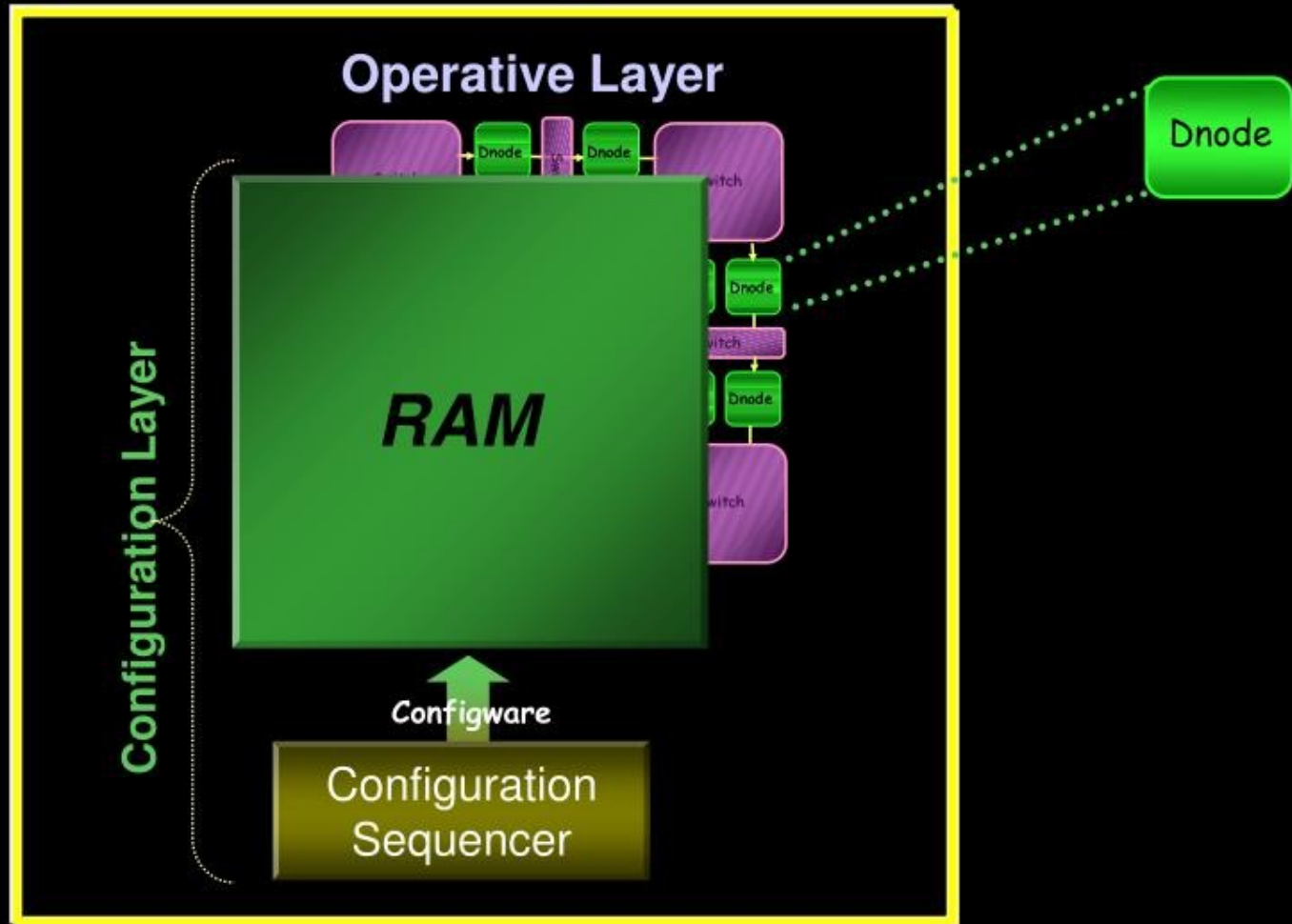
Application example - DCT 2D 8*8

64*64 image example - Comparisons



The Systolic Ring - System Overview

Two-layers based reconfigurable architecture

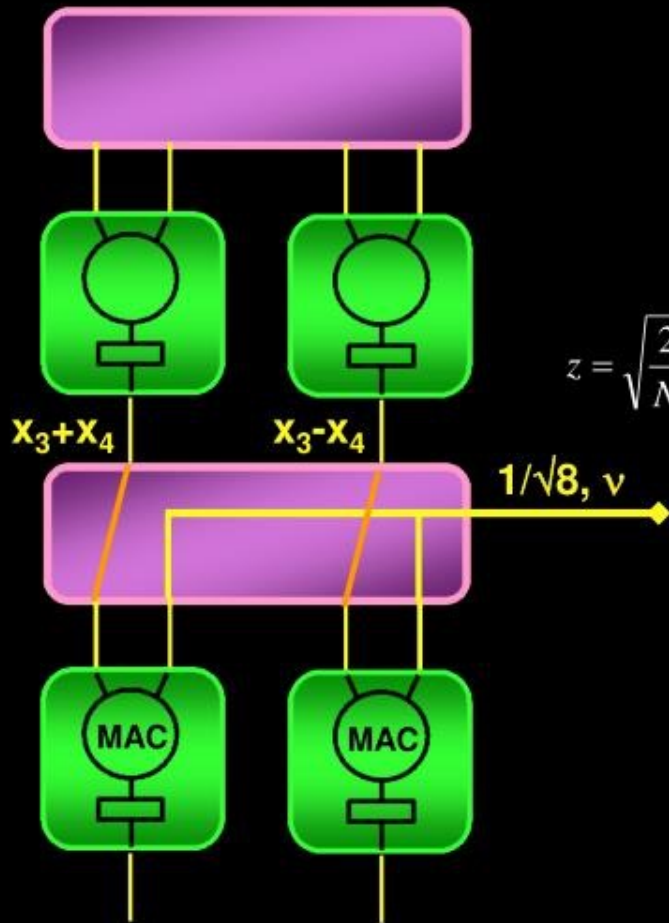


Coarse Grain Dynamically Reconfigurable Architecture

Application example - 8*8 2D DCT



Cycle 4



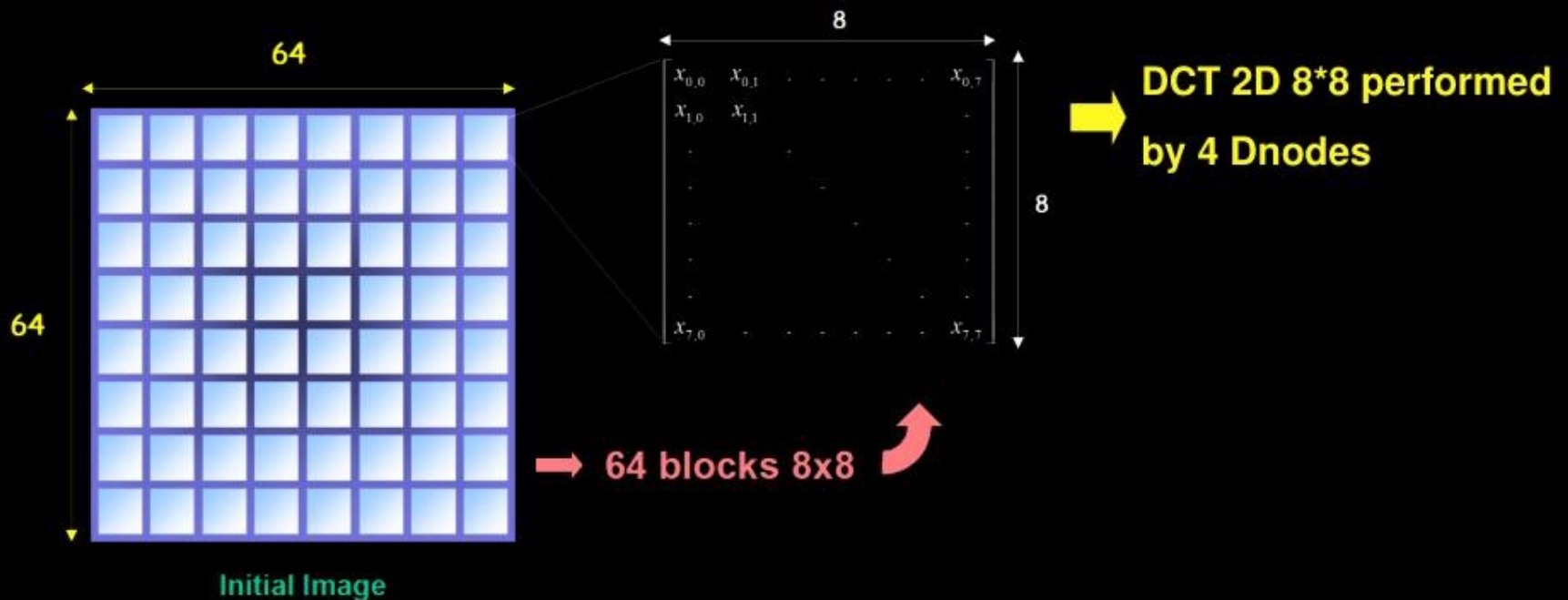
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Application example - DCT 2D 8*8

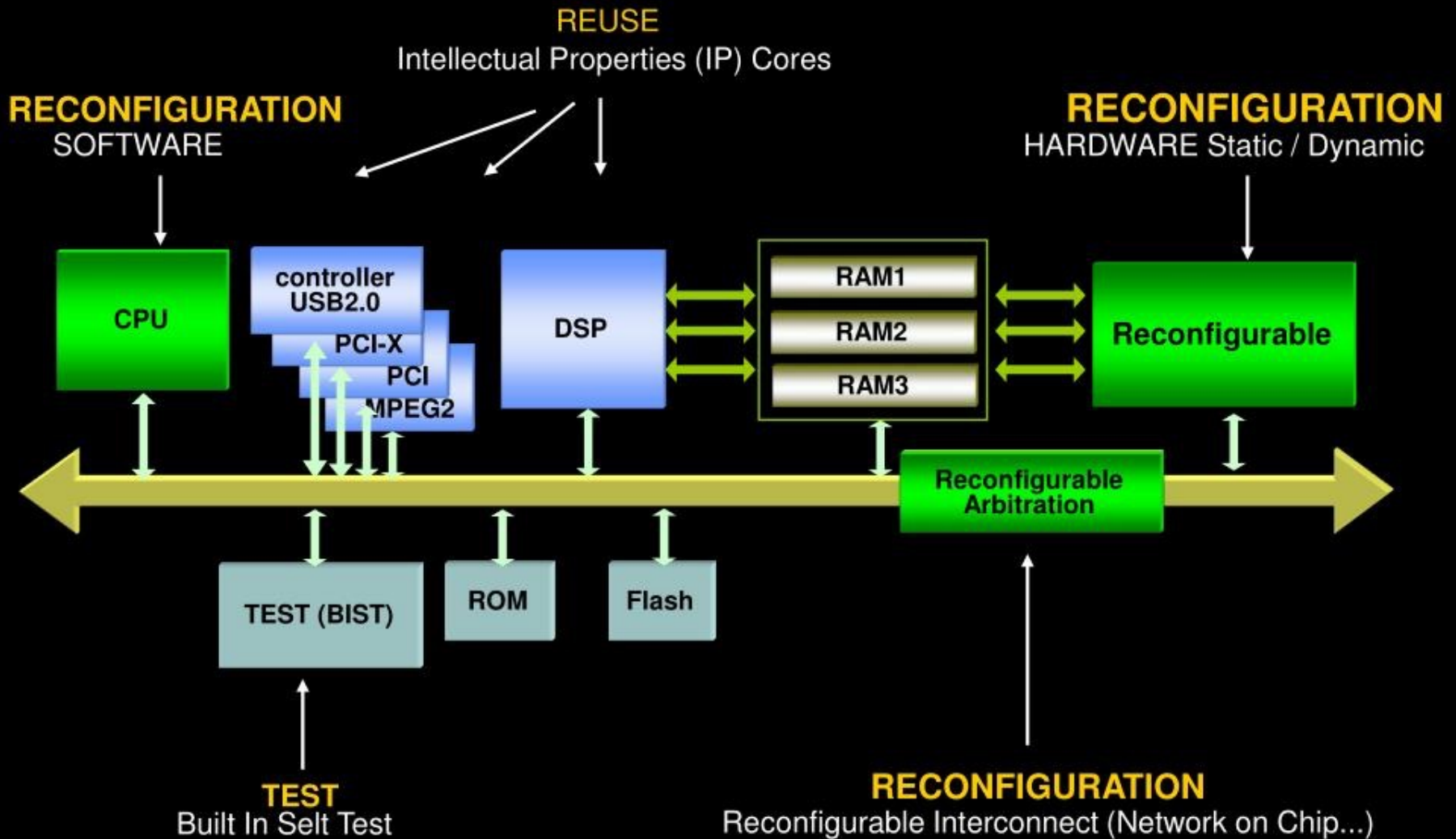
64*64 image example



computation clock cycles = 320 . (# of 8 - points 2D blocks). $\frac{4}{N}$

RING-N implementation (N Dnodes)

Introduction - SoC architectures





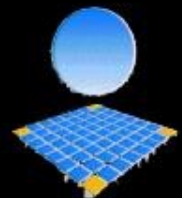
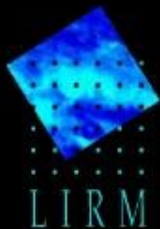
Sophia Antipolis
9-10 Oct 2002

System on a Chip

The Systolic Ring : A Scalable Dynamically Reconfigurable Core for Embedded Systems

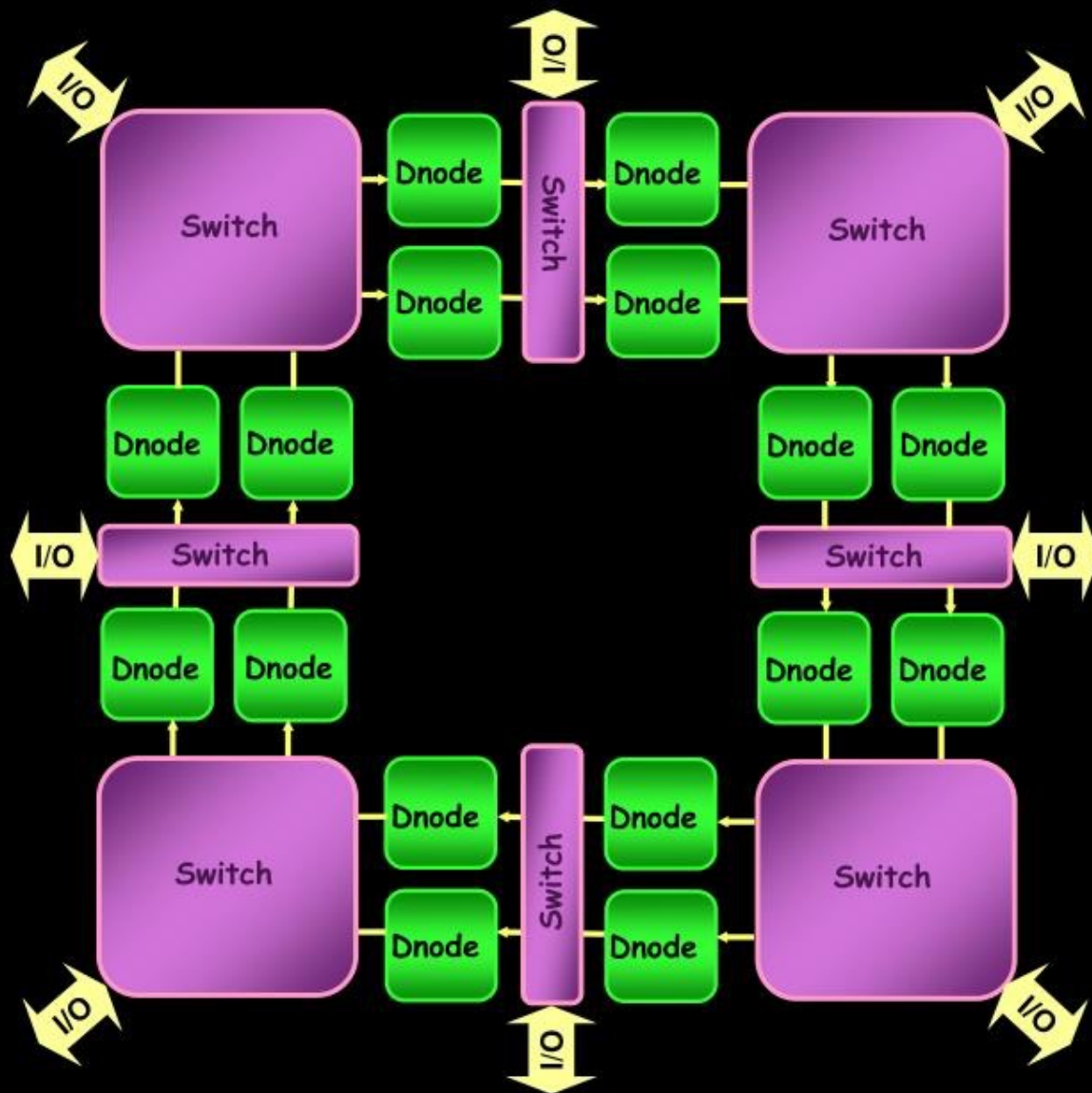
Pascal BENOIT,

G. SASSATELLI, M. ROBERT, L. TORRES, G. CAMBON, T. GIL



UNIVERSITE MONTPELLIER II
SCIENCES ET TECHNIQUES DU LANGUEDOC

The Systolic Ring - Operative Layer Topology



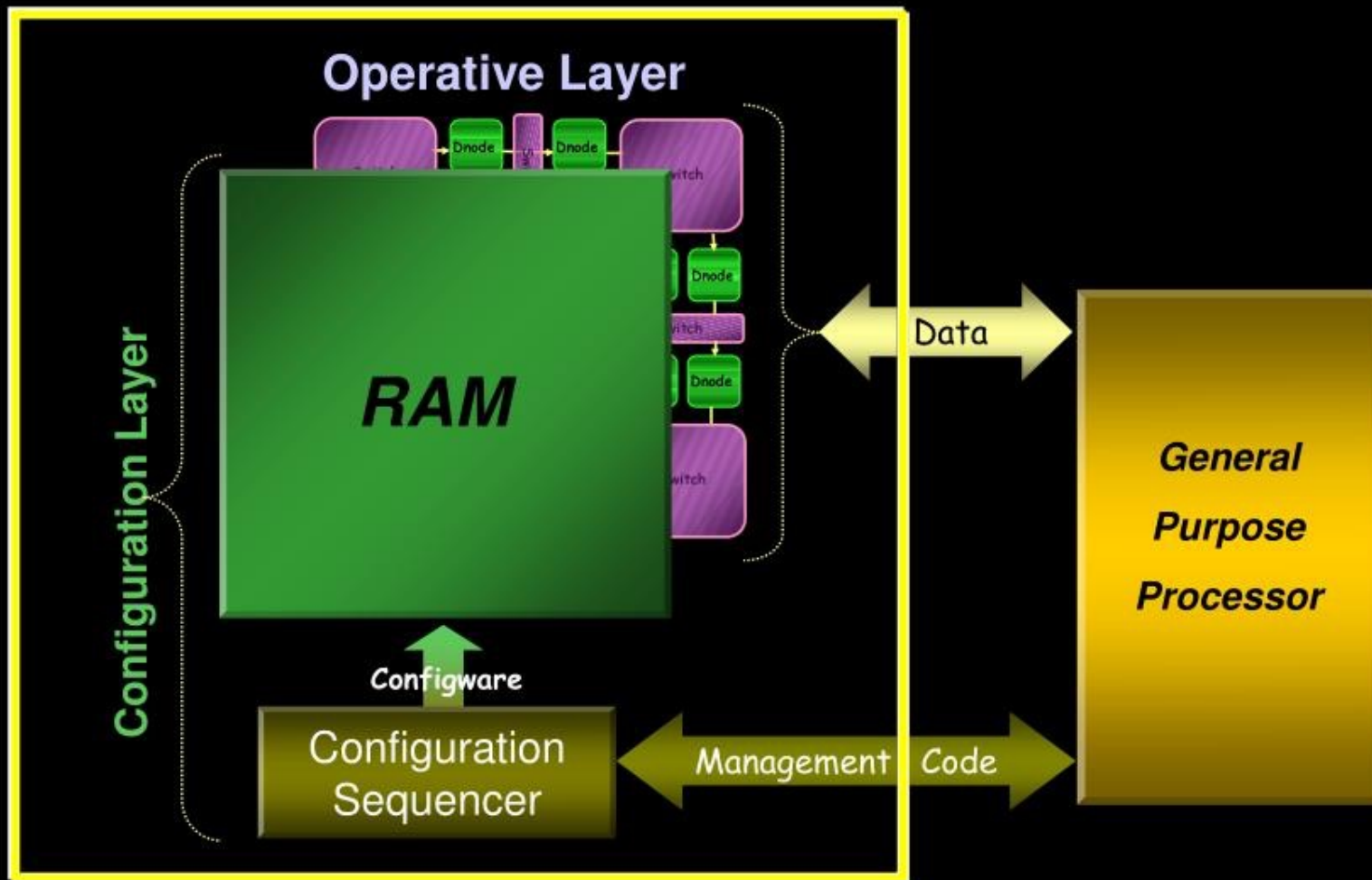
**Ring
Structure**



Customisable...

The Systolic Ring - System Overview

Not a stand-alone solution

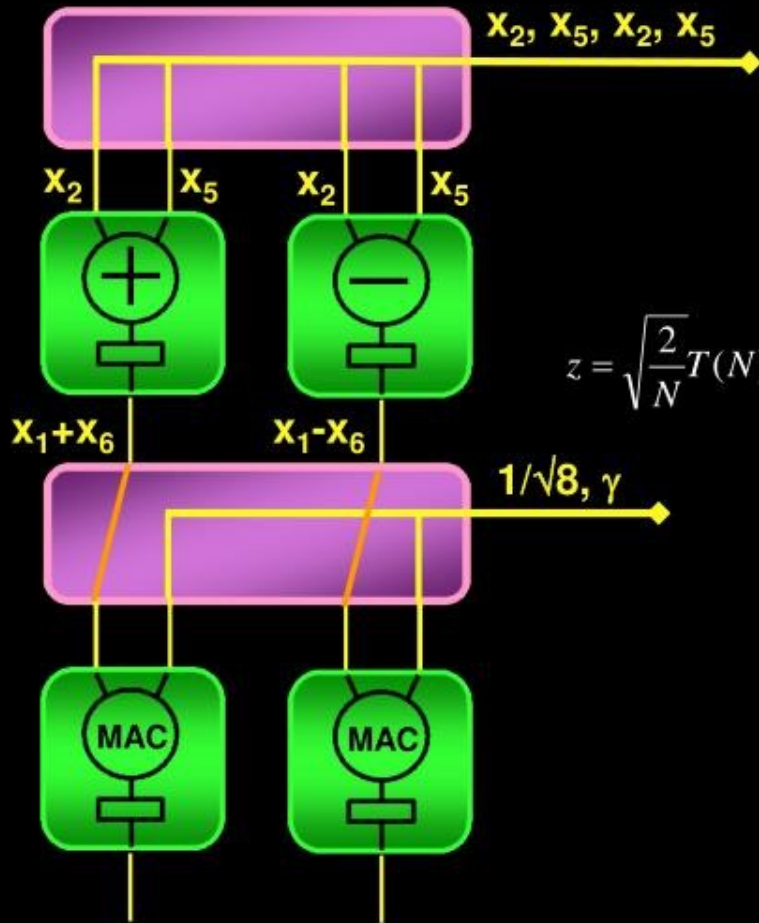


Coprocessor for data flow oriented applications

Application example - 8*8 2D DCT



Cycle 2



$$z = \sqrt{\frac{2}{N}} T(N) x \left\{ \begin{array}{l} \begin{array}{l} \begin{bmatrix} z_0 \\ z_2 \\ z_4 \\ z_6 \end{bmatrix} = \begin{bmatrix} 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} & 1/\sqrt{8} \\ \beta & \delta & -\delta & -\beta \\ \alpha & -\alpha & -\alpha & \alpha \\ \delta & -\beta & \beta & -\delta \end{bmatrix} \begin{bmatrix} x_0 + x_7 \\ x_1 + x_6 \\ x_2 + x_5 \\ x_3 + x_4 \end{bmatrix} \\ \begin{array}{l} \alpha = 1/2 \cos(\pi/4) \\ \beta = 1/2 \cos(\pi/8) \\ \delta = 1/2 \sin(\pi/8) \end{array} \end{array} \\ \begin{array}{l} \begin{bmatrix} z_1 \\ z_3 \\ z_5 \\ z_7 \end{bmatrix} = \begin{bmatrix} \lambda & \gamma & \mu & \nu \\ \gamma & -\nu & -\lambda & -\mu \\ \mu & -\lambda & \nu & \gamma \\ \nu & -\mu & \gamma & -\lambda \end{bmatrix} \begin{bmatrix} x_0 - x_7 \\ x_1 - x_6 \\ x_2 - x_5 \\ x_3 - x_4 \end{bmatrix} \\ \begin{array}{l} \lambda = 1/2 \cos(\pi/16) \\ \gamma = 1/2 \cos(3\pi/16) \\ \mu = 1/2 \sin(3\pi/16) \\ \nu = 1/2 \sin(\pi/16) \end{array} \end{array} \right. \end{array}$$

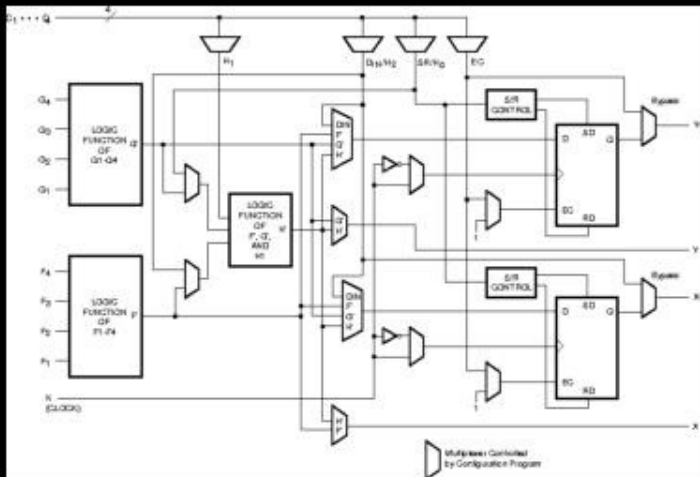
Introduction

What kind of base block is suitable for Multimedia?

■ Fine grain:

→ Granularity: BIT

adapted to Prototyping, Encryption

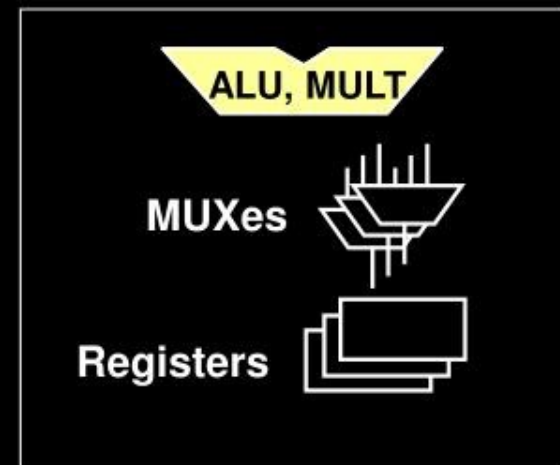
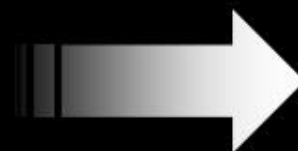


- High reconfiguration over-cost
- Low Functional frequencies

■ Coarse Grain:

→ Granularity: WORD

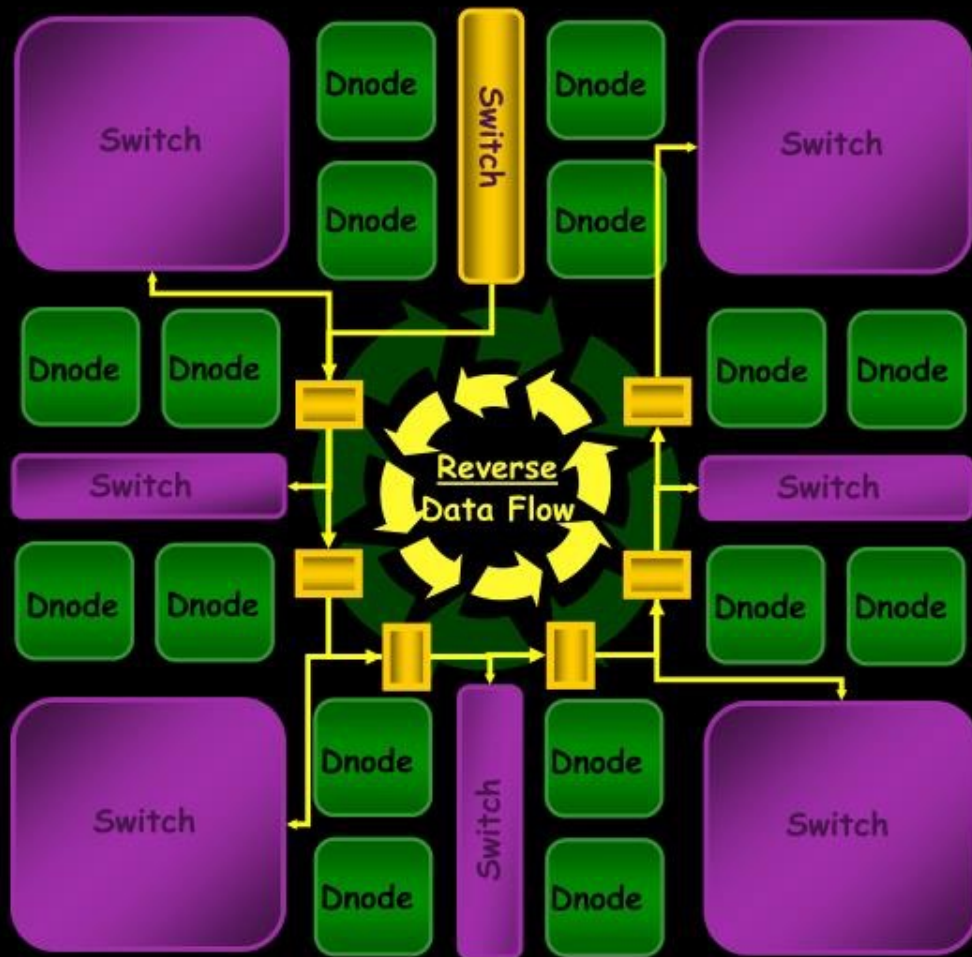
adapted to DSP, data flow oriented processing



- Low reconfiguration over-cost
- High level of performances

The Systolic Ring - Operative Layer Topology

Data Flows



Forward Data Flow

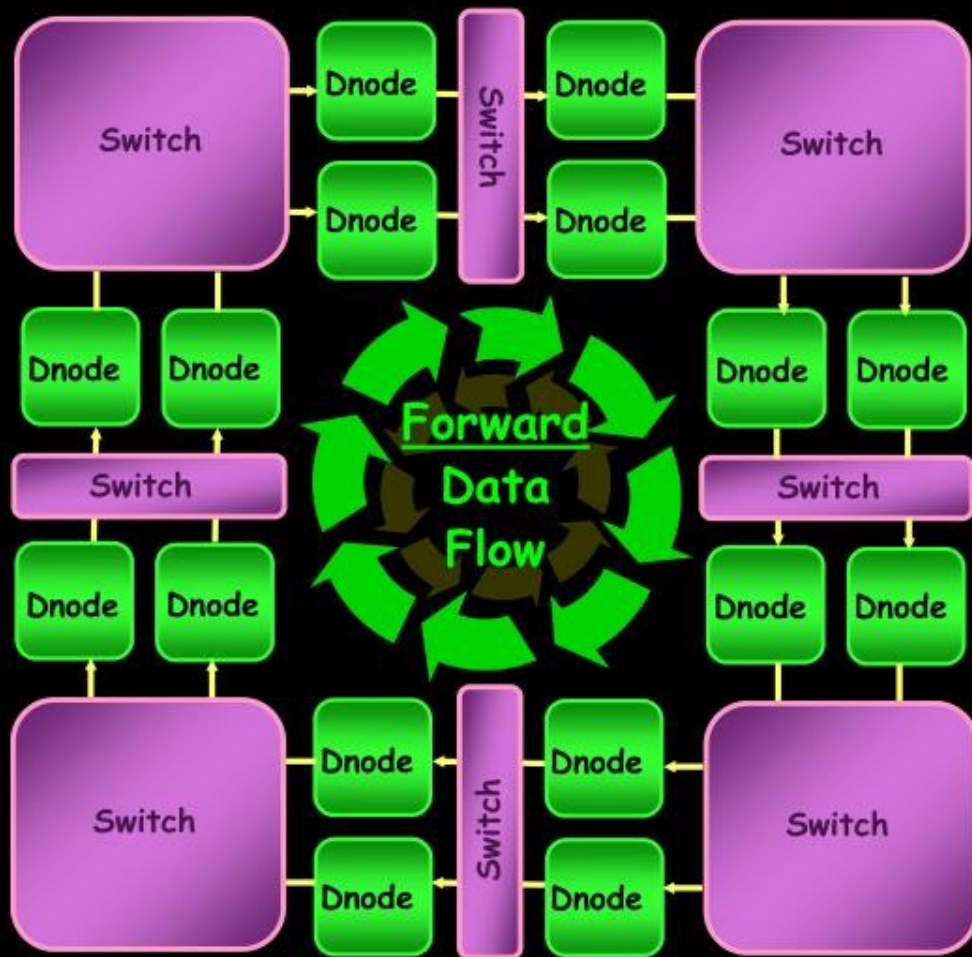
Unidirectional data transit between successive layers (circular pipeline

Reverse Data Flow

Feedback pipeline network for recursive algorithms

The Systolic Ring - Operative Layer Topology

Data Flows



Forward Data Flow

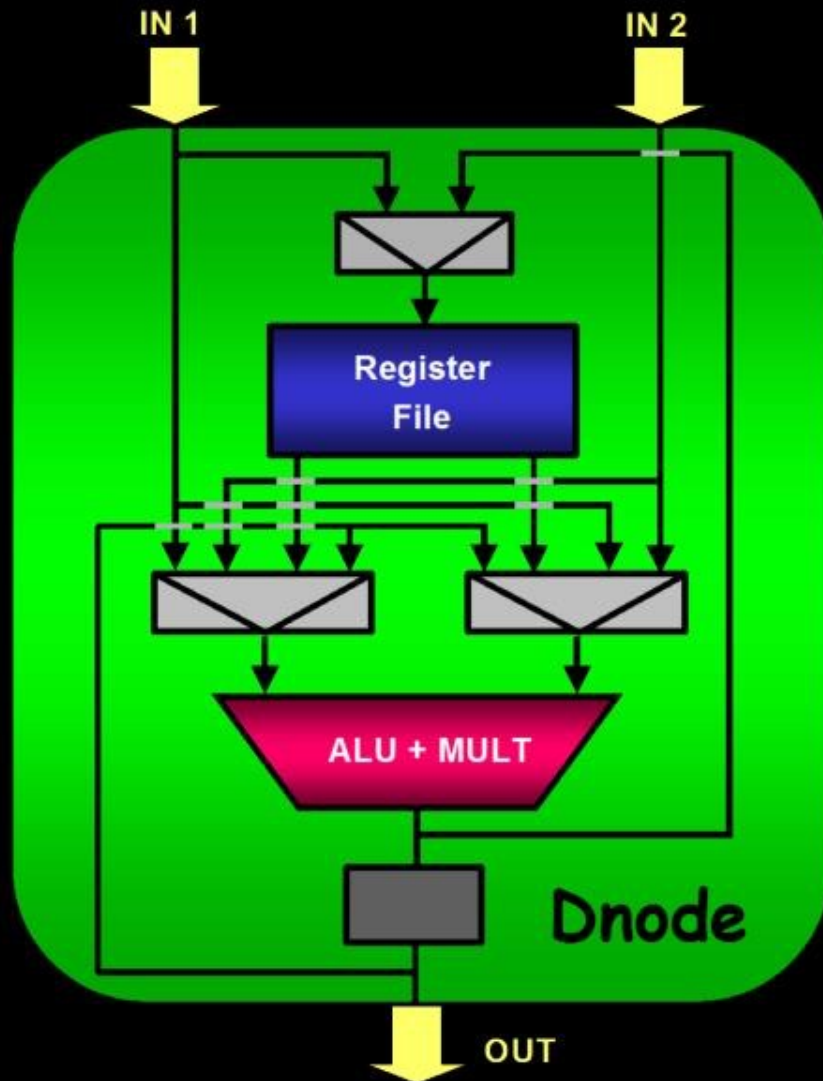
Unidirectional data transit between successive layers (circular pipeline)

Reverse Data Flow

Feedback pipeline network
for recursive algorithms

The Systolic Ring - Building block

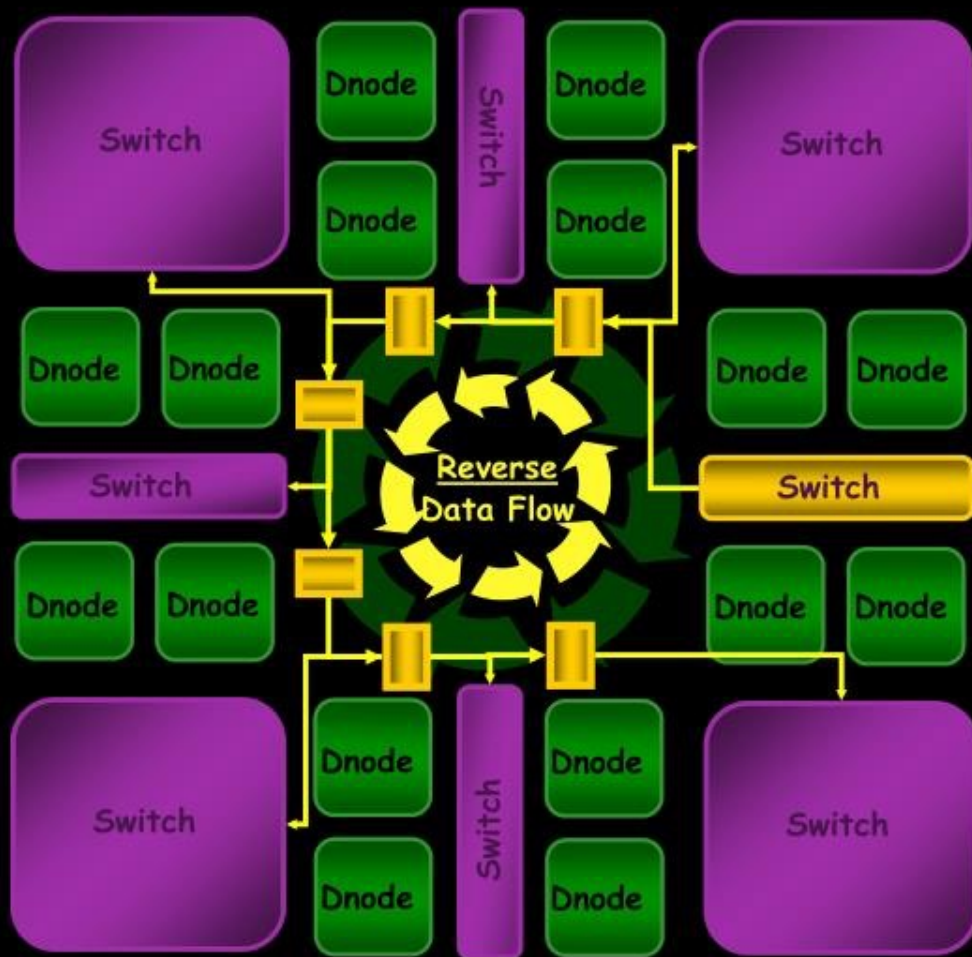
DNODE (Data Node)



- **Data processing oriented block**
 - ALU + Multiplier (MAC)
- **Programmable component**
 - Local Sequencer
 - Dynamic and autonomous configuration management
 - *one instruction per cycle*

The Systolic Ring - Operative Layer Topology

Data Flows



Forward Data Flow

Unidirectional data transit between successive layers (circular pipeline

Reverse Data Flow

Feedback pipeline network for recursive algorithms

The Systolic Ring

Systolic Ring Features

■ RING-8 (8 Dnodes)

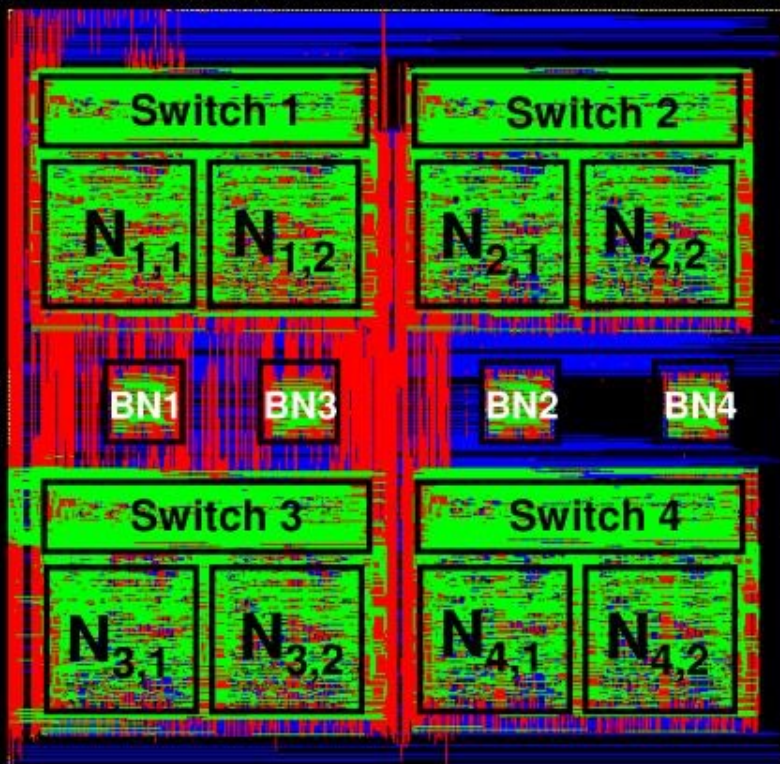
→ 0.18 μ technology

3.3 mm²

200 MHz

1600 MIPS

1600 MMACs / s



Operative Layer Layout

Process geometry dropping \Rightarrow increase Dnode #