# Implementation of an Experimental IEEE 1149.4 Mixed-Signal Test Chip

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Uroš Kač[1], Franc Novak[1], Florence Azaïs[2], Pascal Nouet[2], Michel Renovell[2]

[1]Jozef Stefan Institute, Ljubljana, Slovenia
[2]LIRMM, University of Montpellier, France

**Abstract**

*The paper reports current results in the design, implementation and applications of an IEEE 1149.4 test chip with extended ABM functionality. As no previous experience or information on Dot 4 compatible integrated circuits design was available, the project has been approached in two stages. A simplified preliminary test chip was designed "from scratch" and has recently become available. Debug and evaluation of the preliminary design will provide useful information for the design and implementation of a second test chip version. Besides correcting identified design deficiencies the second version will also include minor ABM modifications which will allow the development of enhanced measurement procedures as described in the paper.*

## 1. Introduction

Since the early 1980s electronics manufacturers have been looking for a solution to the problem of limited access circuit testability. As increasingly dense and complex electronic designs made the established in−circuit test techniques more costly and difficult to implement, the innovative boundary scan method was proposed to improve design controllability and observability. On the initiative of Joint Test Action Group (JTAG) the proposed approach was adopted in 1990 by IEEE as the 1149.1 standard [1]. Since IEEE 1149.1 addressed solely digital circuits, the development of equivalent test structures for incorporation into mixed−signal circuits and corresponding measurement methodologies [2] started soon after. Standardization efforts on a IEEE 1149.1 compatible test bus that would improve mixed−signal design testability at both device and assembly levels finally resulted in the adoption of the IEEE 1149.4 (Dot 4) standard in 1999 [3].

The IEEE 1149.1 boundary scan quickly became a widely accepted design for testability technique in digital circuits, gaining support from component manufacturers as well as EDA tools and test equipment providers. This resulted in extensive use of 1149.1 infrastructure in various designs throughout the past decade. On the other hand, its mixed−signal twin seems to have a much harder time finding the way into real life applications. The apparent lack of interest for 1149.4 from major electronics manufacturers, with few exceptions [4], results in the absence of Dot 4 compatible catalogue devices and consequently the inability of designers to include standardized mixed−signal test infrastructure into their systems.

A probable reason for this situation is the complexity of on−chip Dot 4 infrastructure and the impact it would have on proven analog and mixed−signal designs. The efforts necessary to include overhead logic into the circuit must be justified by the benefits it provides. One can learn from the history of 1149.1 boundary scan technology that its acceptance was greatly helped by applications, which demonstrated its value not only in the design testability domain but also in areas such as design validation and debugging or in−system configuration of programmable devices.

Similarly, we believe that wider popularization of the Dot 4 mixed−signal test bus will only come with the demonstration of its benefits in actual designs and also with the presentation of other interesting applications based on the Dot 4 infrastructure [5]. To facilitate our efforts in developing innovative 1149.4 based test and measurement procedures and in the absence of ready to use solutions we decided to design and implement an experimental Dot 4 chip including certain extended functionality.

## 2. Implementation of the Dot 4 test chip

Since no information on the implementation of on−chip Dot 4 infrastructure other than IEEE 1149.4 standard guidelines was available, we approached the design of the test chip in two stages. First, a preliminary chip adherent to the standard 1149.4 architecture would be implemented, which will allow us to assess actual characteristics of complex mixed−signal cells (Analog Boundary Module / ABM, Test Bus Interface Circuit / TBIC) and identify possible design inefficiencies and necessary modifications. To simplify design debugging, the digital part (Test Access Port / TAP controller, instruction and bypass registers and decoder) is implemented off−chip using a programmable logic device.

In next stage the final version of the Dot 4 test chip will be implemented, which will add the digital control circuitry logic to the design and provide some extended ABM functionality with respect to the standard architecture.

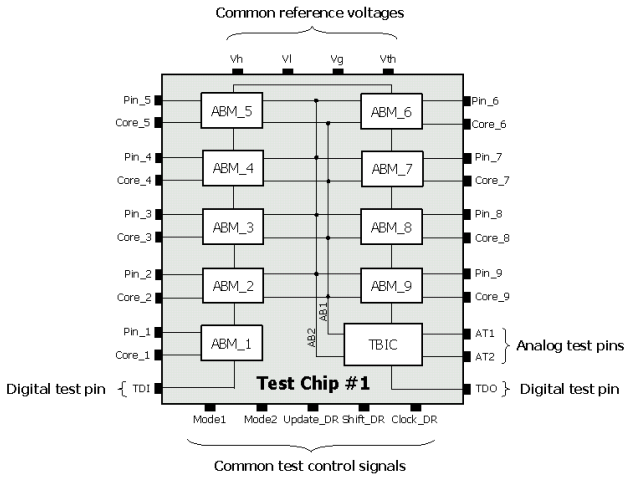


Figure 1: Preliminary test chip block diagram

### 2.1 Preliminary chip version

The design of the preliminary Dot 4 test chip version followed schematic representations of the boundary scan register modules as proposed by the IEEE 1149.4 standard. It required the implementation of three main cells: the ABM cell, the TBIC cell and the test control circuitry, each consisting of a number of sub−modules. As mentioned above, only ABM and TBIC cells, which represent the key architectural features of 1149.4 standard, were implemented on−chip (Figure 1). The 0.8µm AMS CYE technology was chosen for the implementation of the test chip.

The realization of conceptual analog switches and comparators in both ABM and TBIC cells requires particular attention. While the standard allows conceptual switches to be realized in different ways, we have chosen to use exclusively transmission gates since the chip is implemented in CMOS technology and does not include a functional analog core. This would also produce a more generic ABMs structure usable both as an input or output module in experimental designs. The analog switching architecture of an ABM cell is illustrated in Figure 2.

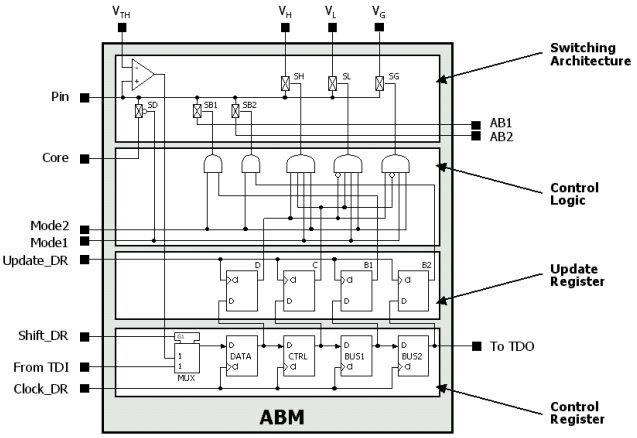


Figure 2: Schematic representation of the ABM

The relatively high internal resistance exhibited by standard AMS library switch cells required design modifications (Table 1) in order to obtain transmission gates suitable for inclusion into the ABM/TBIC analog switching structure. Similarly, available standard cell comparators occupied an unacceptably large silicon area, therefore a full−custom comparator was designed, which satisfies our requirements both in terms of silicon area and electrical characteristics (Table 2).

| Cell | Dimensions (µm) | Surface ($\mu m^2$) | $R_{ON}$ (Ω) at $V_{DD}$ |
|---|---|---|---|
| TG2B (library) | 16.2 x 34.5 | 559 | 1620 |
| TG_inv (modified, integrated inverter) | 26.8 x 39.7 | 1064 | 750 |

Table 1: Comparison of area and resistance between library and modified switch cell

| Cell | Offset (µV) | $A_v$ (dB) | $V_{out}$ min | $V_{out}$ max | $V_{th}$ min | $V_{th}$ max | Size ($\mu m^2$) |
|---|---|---|---|---|---|---|---|
| Comp01 B (library) | 27 | 87 | 3 nV | 5V | 0.1V | 4.4V | 25000 |
| Compa-rator (full custom) | 92 | 61 | 17 mV | 5V | 0.1V | 4.6V | 2800 |

Table 2: Comparison between library and full−custom comparator implementation

Synthesis of the control logic and registers was relatively straight forward, requiring only logic equations optimization in order to allow the use of standard library cells (inv, nand2, nor2). The final implementation of the preliminary Dot 4 test chip is illustrated in Figure 3. Altogether nine ABM cells and one TBIC were laid on an active area of 1980 x 1980 $\mu m^2$, featuring 39 pads connected to 5 control signals (mode1, mode2, update_DR, shift_DR and clock_DR), 2 digital test signals (TDI and TDO), 2 digital power supply lines (VDD and GND), 2 analog power supply lines (VDDA and GNDA), 2 analog test signals (AT1 and AT2) and 18 pairs (pin and core) of ABM functional signals.

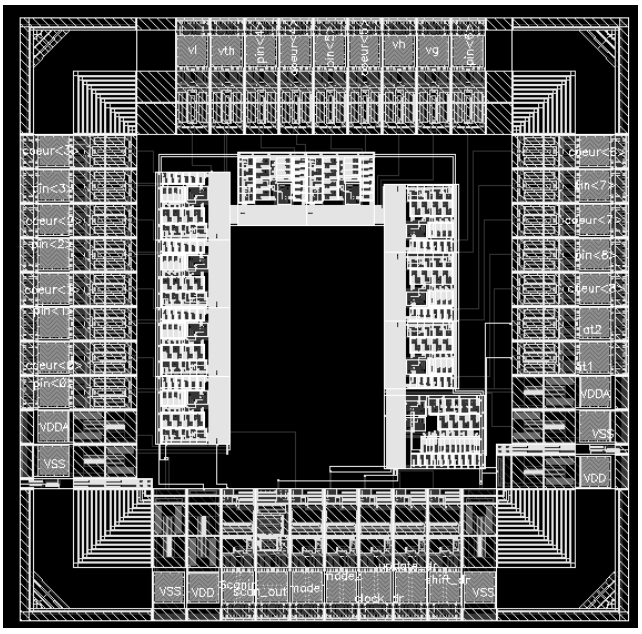


Figure 3: Preliminary test chip layout

## 2.2 Modified Dot 4 test chip version

The second version of the Dot 4 test chip will include some modifications, which address certain deficiencies in the preliminary design as well as facilitate the simulation of optional functions included in experimental 1149.4 compatible designs. The later will also allow the implementation of alternative test and measurement procedures based on existing Dot 4 infrastructure.

Considering both implementation guidelines and measurement methodology proposed by the standard, we decided to apply the following modifications to the ABM switching architecture:

– The core disconnect switch was excluded from the original cell implementation and will be implemented as a separate cell consisting of a low resistance ($R_{ON}$ < 50 Ω) CMOS transmission gate. This fature will allow the user to decide whether to use the on−chip switch, to include the core disconnect facility into the functional output of his analog design or not to implement it at all.

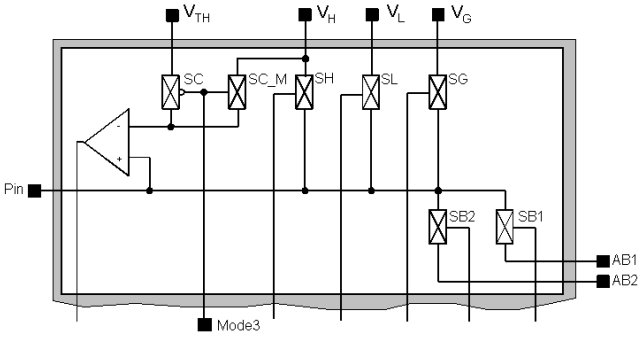


Figure 4: Simplified illustration of modified switching architecture in ABM cell

| Mode3 | SH | SL | SG | Function |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | Pin to $V_H$ |
| 0 | 0 | 1 | 0 | Pin to $V_L$ |
| 0 | 0 | 0 | 1 | Pin to $V_G$ |
| 1 | 1 | 0 | 0 | Vcmp to $V_H$ |
| 1 | 0 | 1 | 0 | Vcmp to $V_L$ |
| 1 | 0 | 0 | 1 | Vcmp to $V_G$ |

Table 3: Proposed decode logic modification

– Three modified ABM cells were also designed with additional switching resources, which allow to connect the compare voltage input of the comparator to either $V_{th}$ or one of the $V_H$, $V_L$ or $V_G$ reference voltages (Figure 4, Table 3).

Finally, the test control circuitry will be implemented on−chip, releasing valuable pad resources required by input/output control signals and simplifying the use of the Dot 4 test chip. A schematic representation of the modified test chip is illustrated in Figure 5.

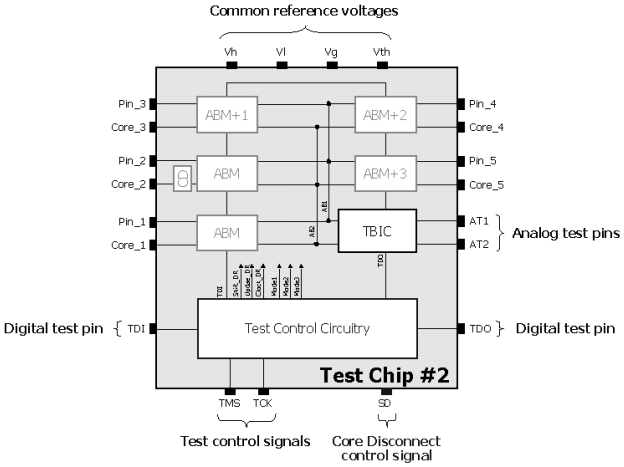


Figure 5: Block diagram of the modified Dot 4 test chip

## 3. Applications of extended ABM functionality

Besides mandatory instructions (PROBE, BYPASS, SAMPLE/PRELOAD and EXTEST) various optional test instructions (INTEST, RUNBIST, HIGHZ,...) are also proposed by the IEEE 1149.4 standard, which can be implemented in Dot 4 compliant components [3].

These instructions basically follow the rules set by the IEEE 1149.1 standard. There are however certain differences in how they apply to the digital and to the analog part of a mixed−signal device, which is a consequence of the functional differences between ABMs and digital boundary modules (DBM). This may in turn affect the efficiency of mixed−signal test procedures based on Dot 4 infrastructure.

The 1149.4 digital boundary modules provide the same functionality as the 1149.1 boundary scan cells. These allow to apply test stimulus and monitor the response of the digital part of the mixed−signal core during an internal test (INTEST) with the core being isolated from input/output pins. On the other hand, the implementation of the ABM, as proposed by the standard, does not allow to disconnect the analog core from input/output pins while maintaining the ability to access the core functional inputs/outputs through the on−chip analog test bus. Consequently, analog INTEST can only be performed with external circuitry connected to the analog core. This requires some means of control over external on−board circuitry in order to provide appropriate operating conditions to the core or to ensure that the inputs are quiescent.

To overcome this deficiency we propose an additional test access node, which is placed on the "core" side of the core disconnect switch (SD). This node would provide access to the analog core functional input/output through the on−chip analog test bus (AB1, AB2) and two additional small−size CMOS switches (SB1_INT, SB2_INT), which bypass the core disconnect switch.

The proposed ABM enhancement would allow to perform analog core internal test (INTEST) without the need for control over external circuitry, therefore simplifying the overall test procedures. Furthermore, functional test of chip cores and external circuitry could be also performed by means of on−board IEEE 1149.4 infrastructure. As demonstrated in [6], selected analog functional blocks can be reconfigured into a self−testing structure by establishing connections via the Dot 4 analog test bus and efficient GO/NO−GO functional tests can then be performed. The enhanced ABM structure would also allow to perform reconfiguration based functional test procedures internally to the chip and could be exploited for the implementation of efficient analog built−in self−tests (ABIST), [7].

The necessary ABM modifications would minimally impact its original structure: with core disconnect switches (SD) being controlled by a global chip signal, an additional global signal provided by the 1149.4 instruction decoder during INTEST would be sufficient to activate the core analog test bus switches (SB1_INT, SB2_INT) and disable the standard switches (SB1, SB2). Only minor modifications in ABM control logic are therefore required in order to generate adequate control signals.

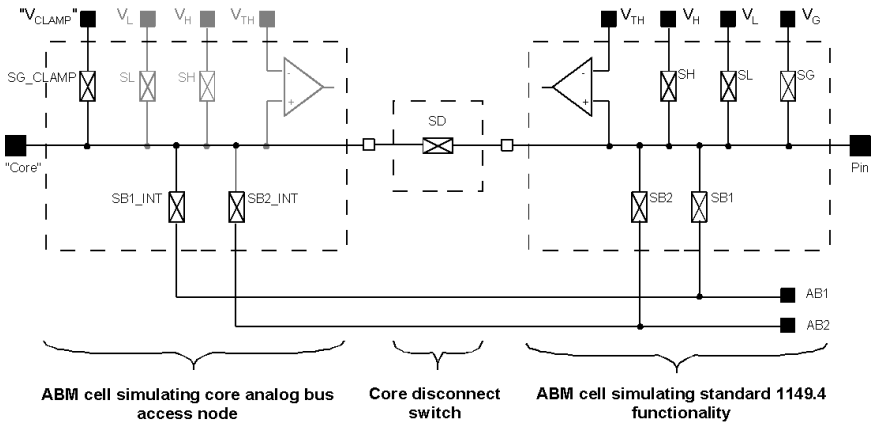


Figure 6: Simulating core access from analog test bus during INTEST

A possible disadvantage of the enhanced ABM structure is the influence it might have on the analog transfer function. The two switches connected to the analog core functional input/output introduce additional parasitic capacitances into the signal path and should be carefully modelled in order to minimize their impact on the analog design functionality.

The modified Dot 4 test chip, which implements the core disconnect switch as a separate block, can be exploited to simulate the enhanced ABM. Two ABMs and one SD are connected as illustrated in Figure 6, providing a structure similar to the proposed enhanced ABM. Such a configuration can be primarily used to experimentally evaluate alternative test procedures, based on analog blocks reconfiguration.

The second modification in the ABM cell consist of additional switching resources, which allow to connect the compare voltage input of the comparator to either $V_{th}$ or one of the $V_H$ , $V_L$ or $V_G$ reference voltages. This feature could prove useful during interconnect test as it provides augmented diagnostic capabilities, allowing one to distinguish between multiple input voltage levels. An illustrative example is given in the following.

Consider the situation of a bridging fault encountered during interconnect test (EXTEST) as illustrated in Figure 7. In the preliminary chip implementation, SH and SL are implemented with identical CMOS transmission gates which exhibit substantial ON−resistance connected in series with reference voltage sources. As noted by the IEEE 1149.4 standard, in this case the voltage appearing at the combined (shorted) net is likely to be at some value between the $V_H$ and $V_L$ levels. The compare voltage $V_{th}$ should be chosen such that it is clearly different from possible input voltage levels while on the other hand the standard limits $V_{th}$ to a value in the range $(V_H + V_L)/2 \pm (V_H - V_L)/4$, which might cause intermediate input values to overlap with the uncertainty region of the comparator, resulting in possible fault masking. This is confirmed by SPICE simulation (Figure 7) which places the resulting voltage uncomfortably close to $(V_H + V_L)/2$. A possible solution to this problem is to use the proposed modified ABM switching scheme to shift the comparator treshold level away from the hazardous intermediate area by switching the compare voltage to either $V_H$' or $V_L$', according to the expected fault−free input value ($V_H$ or $V_L$), Figure 8.

According to IEEE 1149.4 standard, $V_H$ and $V_L$ should always be available on both input and output pins and they can be pin specific i.e. they are not necessarily the same on all pins. Therefore adequate $V_H$' and $V_L$' values can be chosen on the input pins $In_1$ and $In_2$, such that a sufficient noise margin (NM) is maintained for both fault−free input voltage levels.

Although other approaches are possible, such as providing dominant/recessive $V_L/V_H$ drivers in the ABM design, the presented solution might prove advantageous both in terms of parasitics impact on the functional pin and the required additional implementation area.

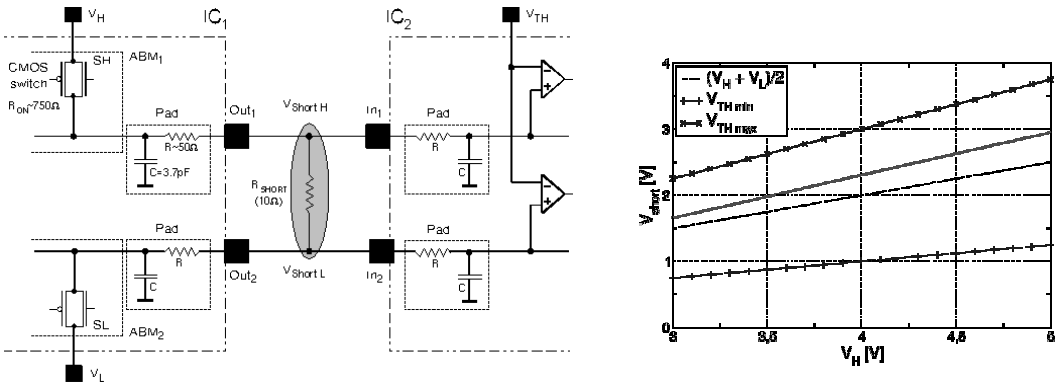


Figure 7: Bridging fault producing an intermediate voltage level during EXTEST

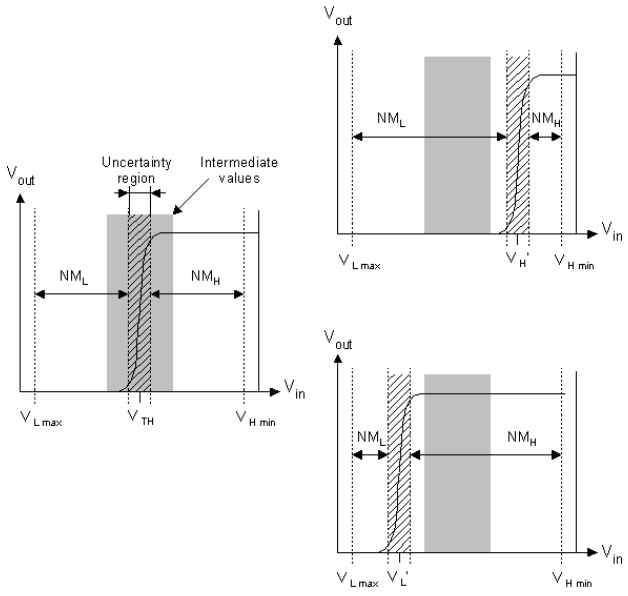


Figure 8: Controlling $V_{th}$ during EXTEST

## 4. Conclusion

The paper reports current results in the design, implementation and applications of an IEEE 1149.4 test chip with extended ABM functionality. The work is performed by LIRMM and JSI in the frame of bilateral french−slovenian PROTEUS project. The first lot of the preliminary test chip version has recently become available and is currently in debug and evaluation stage. We are currently evaluating the functionality and identifying deficiencies of both analog and the digital parts of the design before integrating them in the second Dot 4 chip version. Besides, the prototype will be used in the early development stage of enhanced measurement procedures briefly described in Section 3. Corresponding software support for our home−brewed boundary scan tester is currently under development.

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