A Remote Access to Engineering Test Facilities for the Distant Education of European Microelectronics Students

Yves Bertrand, Marie-Lise Flottes, Florence Azaïs, Serge Bernard, Laurent Latorre, Régis Lorival

▶ **To cite this version:**

Yves Bertrand, Marie-Lise Flottes, Florence Azaïs, Serge Bernard, Laurent Latorre, et al.. A Remote Access to Engineering Test Facilities for the Distant Education of European Microelectronics Students. 32nd Annual Frontiers in Education (FIE), Nov 2002, Boston, MA, United States. pp.T2E-24, 10.1109/FIE.2002.1157943 . lirmm-00269423

HAL Id: lirmm-00269423

https://hal-lirmm.ccsd.cnrs.fr/lirmm-00269423v1

Submitted on 3 Apr 2008

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

A REMOTE ACCESS TO ENGINEERING TEST FACILITIES FOR THE DISTANT EDUCATION OF EUROPEAN MICROELECTRONICS STUDENTS

Yves Bertrand, Marie-Lise Flottes, Florence Azaïs, Serge Bernard, Laurent Latorre and Régis Lorival[1]

Abstract *¾ The European network for Integrated Circuit testing education described in this paper addresses the shortage of skill in mixed-signal production testing by encouraging students at pre- and post-doctoral levels to attend innovative training courses in the field, jointly supported by industry. The objective of the present educational experience is to strengthen given leading educational centers in Europe, in the critical field of mixed-signal testing, with the active support and guidance of industry. The project is an expansion of the successful French experience on engineering test education which allows any distant student to have a remote access to one - and one only - test resource center equipped with up-to-date/high-tech testers.*

Index Terms ¾ European network, IC testing education, mutualization of educational resources, remote access labs.

ECONOMICAL CONTEXT

The cost of the production test for mixed-signal circuits is a very strategic challenge for the competitiveness of the microelectronics industry. Such circuits are mixed-signal devices that contain both digital and analogue blocks. They may be:

- high added-value ASICs (Application Specific Integrated Circuits)
- composite MCMs (Multi-Chip Modules) with mixed technologies
- new-age SoCs (Systems-on-Chip) designed from IP (Intellectual Property) modules.

These mixed-signal circuits constitute the major part of modern communication devices and their fabrication is strongly boosted by the tremendous growth of the multimedia/telecom market.

Nowadays, testing mixed-signal circuits (the so-called mixed-signal testing) is a very critical economical challenge. In some cases, the test of a multimedia/telecom circuit may constitute up to 50% of its total cost [1]. Moreover, due to the growing complexity of IP-based SoC devices, this high percentage is planned to increase significantly in the years to come. The global test cost for a given circuit mainly includes the cost for test development, the cost for implementing the full characterization test on high-tech engineering testers and the cost for using highly efficient production testers. To give an idea of the economical importance of testing problems, we have to keep in mind that the production test floor of a circuit founder typically consists of about one hundred 1M€ testers. Such testers are used in three eight-hour shifts per day and all year round.

OBJECTIVE

The objective of the European network for test education presented here is to address the shortage in microelectronics engineers with testing skills. Considering the economical context described above, four main levels of test competence are required for future microelectronics engineers, depending on their role in the production process.

- **Test engineers**: Due to the increasing cost of production tests for multimedia/telecom circuits it is mandatory that test engineers have a full knowledge of up-to-date high-tech ATE (Automatic Test Equipment). In addition, these test engineers have to master the theoretical context of circuit testing: fault modeling, fault simulation, Automatic Test Pattern Generation (ATPG), Design-for-Test (DfT) techniques and Built-In Self-Test (BIST) methods.
- **Test program engineers**: The major role played by time-to-market in the economical strategy of circuit manufacturers implies that the time needed for test development has become of critical importance. Thus, it is now mandatory for test program engineers to have a good knowledge of characterization and production test in addition to their traditional software skills.
- **Product engineers**: By definition product engineers must have adequate knowledge in both circuit design and circuit testing.
- **Design engineers**: In the context of a modern Design-for-Test approach, design engineers are nowadays required to be aware of testing issues and to have notions of engineering testing implementation.

In all these test fields, the microelectronic industry suffers an important shortage in microelectronics engineers having sufficient skills in test development, especially for mixed-signal circuits. In Europe, initial education in that

[1]Centre de Ressources de Test du CNFM (CRTC), Pôle CNFM de Montpellier (PCM)
Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM),
University of Montpellier, 161 rue Ada, 34392 Montpellier cedex 5, France
Yves Bertrand, bertrand@lirmm.fr, Marie-Lise Flottes, flottes@lirmm.fr, Florence Azaïs, azais@lirmm.fr
Serge Bernard, bernard@lirmm.fr , Laurent Latorre, latorre@lirmm.fr, Régis Lorival, lorival@lirmm.fr

0-7803-7444-4/02/$17.00 © 2002 IEEE **November 6 - 9, 2002, Boston, MA**
32nd ASEE/IEEE Frontiers in Education Conference

field is too little developed and, to our knowledge, restricted to the current French experience (about 200 students and engineers trained per year).

Taking into account the context described above, there is a strong demand from the microelectronics industry in engineers having knowledge ranging from the simple awareness of testing problems to the full skill and competence in IC testing. It is the objective of the present educational project to respond to this demand by implementing a European network for test education both in initial and continuing education context. The project aims at educating European microelectronics students in IC testing through the implementation of dedicated training courses on highly efficient ATEs. Such testers are intensively used by circuit manufacturers during either the characterization phase of new designs or the production phase of mature devices.

This educational project is based upon the successful experience [2]-[6] of CRTC, the common test resource center for French universities. The expansion at European level includes four new academic partners, namely UPC Barcelona (Spain), Politecnico di Torino (Italy), University of Stuttgart (Germany) and Institute Josef Stefan of Ljubljana (Slovenia). Agilent Technologies is the key industrial partner of the project for providing up-to-date equipment and specific training on clearly identified hot test topics.

CRTC is the leading educational center of the project. Because CRTC is hosted by a research laboratory (LIRMM) which is internationally renowned in the field of circuit testing, it benefits from the competence of its researchers. The teaching staff of CRTC is composed of researchers and professors fully implicated in various research projects on the design and test of integrated circuits and systems. Such projects include DfT and BIST for digital, analogue and mixed-signal circuits [7] and the design and test of fully integrated microsystems [8].

Besides, all the other participants in the consortium have a full competence and expertise in the field of IC testing. This ensures both a solid theoretical background and an up-to-date test knowledge for the trainees.

On the other hand, the present project benefits from the active support of Agilent Technologies. This partnership allows taking advantage of the latest technological developments for ATEs and ensures skill and practical knowledge achievement for trainees through the use of advanced test equipment.

ENGINEERING TEST IN EE CURRICULUM

The issue of improving the quality of engineering testing education of Electronics Engineers (EE) in the US was raised in the early 90's by R. Absher's paper in *IEEE Design and Test of Computers* [9] and a Round Table at the *1991 International Test Conference* [10]-[14]. At that time, it was noticed that engineers had to cope with complicated testing issues of modern microelectronic devices. Moreover, the very limited number of strong research centers capable of spanning the entire spectrum of testing problems was pointed out. As a result there was no testing component in the undergraduate curricula and a significant missing element was the educational link to the realities of manufacturing engineering. Later on, the situation improved a little with the introduction of some theoretical test topics such as : fault modeling, fault simulation, test generation, DfT, BIST, etc. Nowadays, the situation of test education has become critical again.

On the one hand, we witness the amazing event of the System-on-Chip (SoC) revolution which permits any electronic designer to create a complex system on a single chip by using sophisticated IP (Intellectual Property) cores from various design providers. It is now also possible to easily mix analog and digital blocks on the same chip to design the so-called mixed-signal circuits that are boosted by the multimedia and telecom markets.

On the other hand, manufacturing testing is strongly boosted by research advances with the development of new testing techniques such as scan path, boundary scan, Iddq testing, delay testing, mixed-signal testing etc. At the same time, there is a strong demand from consumers for highly complex circuits at low cost, high quality, high reliability and reduced time-to-market. Automatic Test Equipments (ATEs) have thus undergone a strong technological mutation so as to be able to integrate these new techniques and requirements.

As a result of this combined evolution of design and test contexts, the test of new-generation mixed-signal SoCs through the use of new-generation sophisticated test tools become a very critical economical problem, as the first section of this paper underlines.

Under these conditions the education of engineering test in undergraduate and graduate curricula has to be reconsidered. The idea of making ATE accessible to Academic Institutions to make manufacturing testing a part of EE curriculum becomes imperative. This will undoubtedly help microelectronic students to be aware of modern testing problems.

Graduate Level

Our main idea when initiating CRTC five years ago was to bridge the gap between academic testing teaching and effective industrial testing needs [2] [3]. Indeed, we observed that during their job interview students often encountered problems when discussing about IC testing. The reason is a certain misunderstanding about the exact meaning of the word *test*. When educated in academic IC testing, microelectronics students are aware of theoretical topics such as: fault modeling, fault simulation, test generation, Design-for-Test (DfT), Built-In Self-Test, etc. When speaking about industrial testing, the employer essentially refers to topics such as: characterization test, production test, wafer sort, Average Quality Level (AQL),

Automatic Test Equipment (ATE), Shmoo plot characterization, test flow, multi-site testing, etc. Obviously, the vocabulary as well as the underlying concepts differ. Accordingly, we found it mandatory to give our microelectronic graduates a better electronic education by including engineering testing in their curriculum.

From the five-year experience of CRTC we have noticed that students with knowledge in engineering testing undoubtedly have a good added-value when competing to get a job in microelectronics industry.

Undergraduate Level

ATE test training has also proved to be very profitable in the context of undergraduate education. In fact, the only prerequisites for testing a standard IC are the basics of fundamental electronics. In a first approach of circuit testing, it is not necessary to have full knowledge of theoretical test methods.

We have noticed that the development of a complete test program for a classical standard IC strongly contributes to the students' better understanding of electronics. Indeed, during their training period, students often realize the major role played by the so-called *circuit data sheet*. As an example, a majority of students are completely unaware of the importance of critical parameters such as *set-up time* and *hold time* for a satisfactory design of a sequential circuit. The lab part of the training gives them the opportunity to visualize and measure these timing parameters.

TRAINING CONTENTS

The training courses we propose to implement at European level will be open for pre- and post-doctorate students from universities or engineering schools. These training courses will permit to contribute to address the shortage of skills in circuit testing for the microelectronics industry. In particular, it is aimed at allowing the trainees to acquire a solid knowledge in the strategic domain of mixed-signal and SOC testing.

The two main training courses we propose in order to initiate students and engineers to digital IC test stem from those developed by Agilent (ex Hewlett Packard) for the 83000 tester [15]. After completing level 1 training, each trainee will be able to make a competent use of any digital ATE to test a device for its performance parameters and specifications, to build up a test flow to automate the test execution and to create a test program to be executed on the production test floor. After completing level 2 training, he/she will have gained the know-how to test complex devices, to convert simulation data and to make an optimum use of tester resources. Both training courses use a standard digital circuit as DUT (Device Under Test) simply to illustrate all testing functions. Each training is built up on lessons and related lab exercises. The network configuration of CRTC allows any trainee in any distant center to prepare lab exercises using local resources. Moreover, the correctness of both input signal shapes and output strobe locations may be locally checked. Only the test execution itself requires a remote connection on the CRTC tester in Montpellier.

Level 1 training

Level 1 training lasts five days (3 days for accelerated version). The contents is as follows:

- Hardware/Software Overview
- Test Preparation
  - Pin Configuration
  - Level Definition
  - Timing Definition (Period, Edges)
  - Vectors Set up
- Test Execution and Result Analysis
  - Functional test
  - Continuity Test
  - Output Voltage Sensitivity
  - AC Test (Propagation Delay)
  - Input Leakage
  - Sweep Test (Shmoo Plots)
- Advanced Test Concepts
  - Device Cycle
  - Sequencer Use
- Tester Resources Optimization
  - Physical/Logical Waveform
  - MUXIO Mode
  - Frequency Doubling Mode
- Automating the Test
  - Testflow Definition
  - *Smart Test*® Tool
  - Test Program

Level 2 training

Level 2 training lasts five days. The contents is as follows:

- Timing Use Optimization
  - Refreshing Level 1 Training
  - Multi Mode
  - Pin Margin Testing
- Equation Based Test
  - Basics
  - Timing Specifications
  - Output-dependent Timing
  - Level Specifications
- Test Program Translation
  - Simulation Data
  - ASCII Translator
- Advanced Testflow Programming
  - User Procedures
- Multi-Site Testing

REMOTE TEST LABS

European network for test education is mainly based on CRTC experience. So, let us first shortly review this experience.

CRTC Creation

CRTC ("Centre de Ressources de Test du CNFM") has been created in France by CNFM ("Comité National de Formation en Microélectronique") to respond to the industrial demand in engineers with a double Design & Test competence. The CNFM is the French institution which coordinates initial training and continuous education in microelectronics. For more than 10 years, the CNFM has been in charge of the coordination between universities, microelectronics industries and French authorities. This is a consortium that groups the 11 French universities and academic centers involved in microelectronics education. This consortium aims at bringing together heavy soft (CAD tools) and hard resources (clean rooms, ATEs,…) for a common use, at a lower price.

Remote Testing

In 1997, the CNFM decided to create a common test resources center (the so-called CRTC) which concentrates up-to-date and high-tech test resources in a single CNFM center, the so-called PCM ("Pôle CNFM de Montpellier"). A mixed approach has been chosen for test education implementation, that combines both distributed and centralized test resources (Figure1). Indeed, considering the huge cost of high-tech IC testers, the policy of CNFM was to develop one and one only test center for all the French academic centers. So in 1998, the LIRMM was chosen to implement the CRTC. In addition, to avoid any excessive travel expense for students from their university to CRTC in Montpellier, the implementation has been thought to make the CRTC testers reachable by net from any remote center.

CRTC is mainly equipped with up-to-date/high-tech ATEs such as Agilent 83000-F330t VLSI tester and Agilent 93000 SoC tester. In each of the 11 CNFM centers, a server with test software facilities is implemented to allow the local development of test programs (Figure 1).

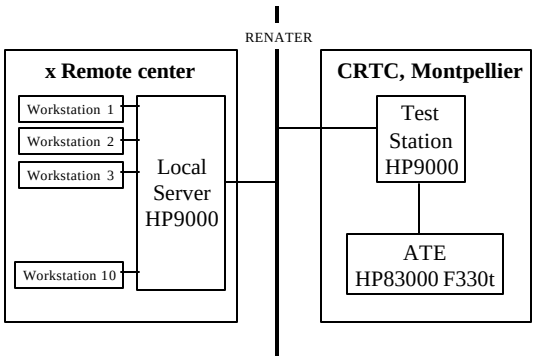

FIGURE. 1
NETWORK IMPLEMENTATION FOR REMOTE TEST.

At the very last moment of the physical test, trainees connect to CRTC tester through the net (RENATER) and execute the test of the Device-Under-Test (DUT). Such an original remote testing implementation enables to save money, first by equipping a single test center with efficient resources, and second by avoiding expensive costs induced by trainee traveling and accommodations.

CRTC Activity

The 3-year evaluation of CRTC clearly demonstrates its full success. The specificity of using a remote connection for acceding test resources makes this project a very original pedagogical experimentation that has permitted to train about 200 engineers per year in both initial and continuing education context (Table 1).

TABLE I
PER YEAR EDUCATION ACTIVITY OF CRTC (1998/2001)

	# training courses	#trainees
Initial Education	12	160
Continuing Education	10	40
Total	22	200

The CRTC teaching team has first organized training sessions for the trainers of the 11 CNFM academic centers (25 trainers have been educated in Montpellier in 1998). Nowadays, the CRTC organization allows each of the 11 CNFM academic centers to organize local test training, combining their own local test resources with a remote access on a common test center. Using this implementation about 160 students per year have been trained in engineering testing through the 11 CNFM centers (Table II).

TABLE II
PER YEAR INITIAL EDUCATION ACTIVITY OF CRTC (1998/2001)

Universities	# training curses per year	# trainees per year
Bordeaux (1)	1	18
Bordeaux (2)	2	32
Grenoble	1	18
Limoges	1	16
Lyon	2	16
Montpellier (1)	2	20
Montpellier (2)	1	20
Toulouse	1	16
Strasbourg	1	4
Total	12/year	160/year

Also, CRTC is very active in the framework of continuing education with about 40 trainees per year coming from circuit manufacturers (ST-Microelectronics), tester manufacturers (Agilent Technologies) and other companies (ISIS, Dassault, …) (Table III). CRTC organizes several one-week training sessions in the field of digital testing (level 1: basics on characterization/production test, level 2: advanced knowledge on engineering testing,) and mixed-signal testing. Each one-week training course is made of a theoretical part (based on slides) combined with effective labs on highly efficient industrial testers.

TABLE III
3-YEAR CONTINUING EDUCATION ACTIVITY OF CRTC (1998/2001)

Companies	# trainees
Agilent (ex-HP)	2
Dassault	2
ISIS-MPP	2
STM-Rousset	58
STM-Crolles	25
STM-Grenoble	6
STM-Edimbourg	2
STM-Agrate	4
STM-Catane	2
Total	**103**

EUROPEAN DIMENSION

The basic idea for the constitution of a European test center (Figure 2) is to start from the CRTC experience as a seed action, and to take advantage of the natural links between LIRMM and its European academic partners to induce the synergy needed to reach this objective. Each of these partners is a center of excellence with international renown in the field of IC testing (new algorithms for ATPG, advanced DfT/BIST architectures, methods for analogue test, test standard development, IDDQ testing, ...). The strong CRTC/Agilent partnership makes high quality industrial testers (Agilent 83000 F330t, Agilent 93000) available at CRTC. Both testers come with their respective software and are fully equipped with servers and workstations. Classroom for lectures and practice are also available at CRTC. This entire environment will support the project. Additional hardware and software for European extension are relatively limited and include (i) a server station per remote center plus 8 workstations connected to it in each center, (ii) an upgrade of the CRTC test server station to manage the extra connections, (iii) different other equipment as new DUTs, design of adapted DUT boards, …

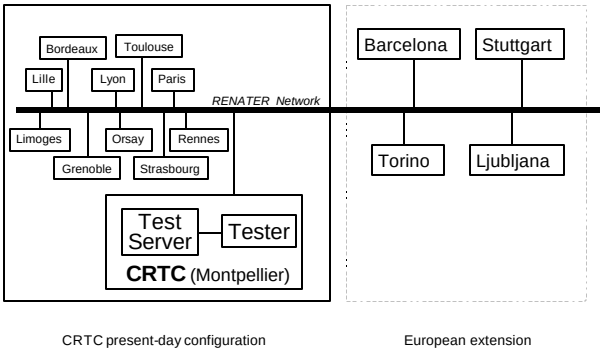

FIGURE. 2
EUROPEAN NETWORK FOR TEST EDUCATION.

Hardware and software resources having been clearly identified, the project success mainly necessitates a large amount of highly qualified human resources. The key point is to dispose of a test engineer at CRTC to manage all the technical problems induced by the project extension. In addition to its classical technical and administrative missions (tester and software maintenance, upgrade survey, training schedule, etc.), the CRTC test engineer has to guarantee a hotline every time a center is connected. For instance, when a distant center performs a training course for 16 students developing test programs in parallel on 8 workstations, the center has to manage the sequential connections to the CRTC tester, and in case any problem occurs, such a hotline becomes mandatory.

The schedule for project planning is described in Figure 3.

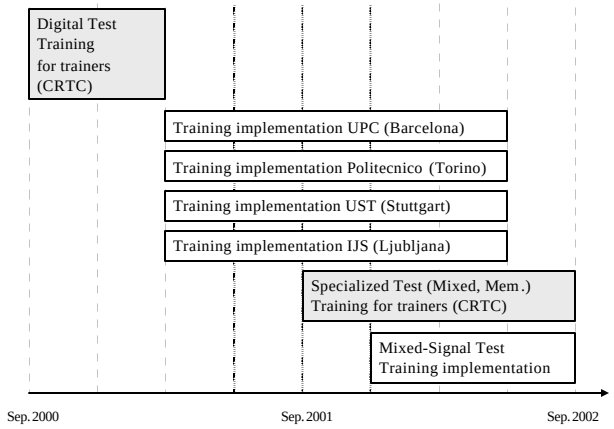

FIGURE. 3
PROJECT PLANNING.

The future trainers of each academic partner will be first trained to engineering test on the Agilent 83K tester of CRTC in Montpellier. Next, these trainers will perform the same training course to their students concurrently in each center. Sixteen students per academic center will thus be trained. Finally, the industrial partner (Agilent Technologies) will train academic participants to more specific test techniques at CRTC. So that, in the future, each academic center will specialize its teaching team in a given test field: mixed-signal test and/or memory test.

As an unfortunate consequence of remote testing policy, distant students never see the tester on which they work. Because this may be a little bit frustrating, we decided to complete the training by providing a web document that presents the tester (mainframe, test head, inside view) and introduces the main practical works to perform before running a test.

By the end of the project, engineering test knowledge dissemination will results in three European centers of competence in Mixed-Signal testing and three European centers of competence in Memory Testing (Table IV).

This configuration will allow a year-round offer in engineering testing education in Europe to be:

- 5 training courses in Digital Test

- 3 training courses in Mixed-Signal Test
- 3 training courses in Memory Test

A coordinated training schedule should permit any European student to dispose of several annual time slots for basic and/or specialized test training.

TABLE IV
EUROPEAN CENTERS OF COMPETENCE IN TEACHING ENGINEERING TEST

Center	Digital Test	M-S Test	Memory Test	Teaching Language
Montpellier (F)	X	X	X	French English
Barcelona (E)	X	X		Spanish English
Torino (I)	X		X	Italian English
Stuttgart (D)	X		X	German English
Ljubljana (SI)	X	X		Slovenian English

ACADEMY/INDUSTRY PARTNERSHIP

Five years ago, French academia was challenged by the microelectronics industry to provide students in microelectronics with a high level education in engineering IC testing. Our original idea of developing one and one only test center, remotely reachable by any French Academic center, was made possible by the strong partnership initiated between CRTC and Agilent Technologies. Of course, a partnership is only durably viable if the two partners can profit from it. In an academic point of view, CRTC is able to propose any European student to attend high-level test training on high-tech industrial ATEs. Also the partnership is fully profitable for the industrial partner considering that about 200 people per year are trained on Agilent testers.

CONCLUSION

The paper deals with a European experience of education in engineering test of ICs and SoCs, using remote testing facilities. The project addresses the issue of the shortage in microelectronics engineers aware of the new challenge of testing mixed-signal circuits for multimedia/telecom market. The project aims at providing test training facilities on a European scale, in both initial and continuing education contexts. This will be done by allowing the academic and industrial partners of the consortium to train engineers using the common test resource center (CRTC). CRTC test tools include up-to-date/high-tech testers (Agilent 83000F330-t and Agilent 93000C400) that are fully representative of real industrial testers, as used on production testfloors. Once the project has been completed, we are planning to reach a normal rate of about 16 engineers/year/center. Each trainee will have attended at least one one-week training using the remote test facilities of CRTC.

ACKNOWLEDGMENT

The **European Network for Test Education** presented here is partly funded by European Community, through IST-2000-30163 Project: **EuNICE-Test** "**Eu**ropean **N**etwork for **I**nitial and **C**ontinuing **E**ducation in VSLSI/SoC **Test**ing using Remote ATE facilities".

REFERENCES

[1] Roberts, G., W., "Improving the Testability of Mixed-Signal Integrated Circuits", *in Proceedings of the IEEE Custom Integrated Circuits Conference, Santa Clara, California*, 1997, pp. 214-221.

[2] Bertrand, Y., Lorival, R., and Cambon, G., "Training Electronics Engineers using Remote Facilities: Experiences in Teaching a Course in Integrated Circuit Testing", *in Proceedings of the 7th World Conference on Continuing Engineering Education, WCCEE'98, Torino, Italy*, May 10-13, 1998, pp. 44-49.

[3] Bertrand, Y., Lorival, R., Robert M., and Cambon, G., "Remote Education Experience on Learning IC Characterization/Production Test", *in Proceedings of the 2nd European Workshop on Microelectronics Education, EWME'98, Noordwijkerhout, The Netherlands*, May 14-15, 1998, pp. 127-130.

[4] Bertrand, Y., Azaïs, F., and Lorival, R., "Test Facilities with Distributed Remote Access for Initial and Continuing Education", *in Proceedings of the SEMICON Singapore 99 Conference, Singapore*, May 4-6, 1999, pp. 65-70.

[5] Bertrand, Y., Azaïs, F., Flottes M-L., and Lorival, R., "A successful distance-learning experience for IC test education", *in Proceedings of MSE'99: International Conference on Microelectronics Systems Education, Arlington, Virginia, USA*, July 19-21, 1999, pp. 20-21.

[6] Bertrand, Y., Azaïs, F., Flottes, M-L., and Lorival, R., "Mixed-Signal Test Training at CRTC", *in Proceedings of the 3rd European Workshop on Microelectronics Education, EWME2000, Aix en Provence, France*, May 18-19, 2000, pp. 251-254.

[7] Azaïs, F., Bernard, S., Bertrand Y., and Renovell, M., "Optimizing Sinusoidal Histogram Test for Low Cost ADC BIST", *Journal of Electronic Testing: Theory and Application (JETTA), Kluwer Academic publishers*, Vol. 17, N° 3/4, 2001, pp.255-266.

[8] Beroulle, V., Bertrand, Y., Latorre, L., and Nouet, P., "Test and Testability of a Monolithic MEMS for Magnetic Fields Sensing", *Journal of Electronic Testing: Theory and Applications (JETTA), Kluwer Academic publishers*, Vol 17, 2001, pp. 441-452.

[9] Absher, R., "Test Engineering Education is Rational, Feasible, and Relevant", *IEEE Design and Test of Computers*, 1991, pp.52-62.

[10] Absher, R., "Can Undergraduate Test Engineering Education be Faster, Better and Sooner", *International Test Conference*, 1991, pp. 1117-1117.

[11] Hawkins, C., and Williams, R., "EE Curriculum - Continuous Process Improvement?", *International Test Conference, 1991*, pp. 1118-1118.

[12] Maly, W., "Improving the Quality of Test Education", *International Test Conference*, 1991, pp. 1119-1119.

[13] Maxwell, P., "The Interaction of Test and Quality", *International Test Conference*, 1991, pp. 1120-1120.

[14] Rose, K., "Quality in Test Education?", *International Test Conference*, 1991, pp. 1121-1121.

[15] HP83000 F330 System Training, Part 1&2, *Hewlett Packard GmbH, Böblingen Semiconductor Test Division*, 1997