A New Methodology for ADC Test Flow Optimization

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Abstract

Testing of Analog-to-Digital Converters is classically composed of two successive and independent phases: the histogram-based test technique evaluating static specifications and the spectral analysis technique evaluating the dynamic performances. Consequently, the fundamental objective here is to investigate the feasibility of an alternative test flow involving exclusively spectral analysis to replace these two time consuming and expensive phases. The viability of this solution depends on the ability of spectral analysis to detect static specifications. In this context, this paper presents a new methodology based on a statistical approach to quantitatively evaluate the efficiency of detecting static errors from dynamic parameter measurements. This methodology has been implemented in an in-house automatic tool allowing one to process any ADC specifications. It is then possible to choose a priori the best test flow for a given application considering the most adequate trade-off between test time and test efficiency.

1 Introduction

In high volume production of Integrated Circuits (ICs), manufacturing costs are strongly affected by testing costs. It is usually admitted that this situation may be critical for mixed-signal circuits when analog blocks are involved. For mixed-signal circuits, it is interesting to note that the cost for the analog part often dominates the total cost of testing while the analog circuitry represents only a small percentage of the total area. A very critical component frequently encountered in mixed-signal systems is the Analog-to-Digital Converter (ADC). So deriving an efficient and economically viable test procedure for these components could significantly lower the testing cost of a mixed-signal system.

An Analog-to-Digital Converter is considered as fully characterized by two different types of parameters:

- the parameters related to the static behavior of the ADC, i.e. related to the transfer function of the ADC,
- the parameters related to the dynamic behavior of the ADC, i.e. related to some kind of degradation of the converted signal.

It is clear that ADC testing procedures used in an industrial context try to identify these two kinds of parameters and so two very different tests are classically applied to ADCs. A histogram-based test is usually applied [1][2] to determine the static parameters (offset and gain errors, as well as Differential and Integral Non-Linearity) while dynamic parameters (SINAD, SFDR, THD) are measured from a spectral analysis [3]. These two tests allow one to fully characterize an ADC [4].

From a pragmatic point of view, the main drawback of the histogram test technique is the very high number of samples required to obtain satisfactory statistical results, implying a long and expensive test time. On the contrary, relatively small sample sets are usually sufficient to get good estimates of the ADC dynamic parameters, implying a short test time and reasonable costs. Obviously, replacing the two previous tests by only one could reduce the test costs. According to the above comments, we could say that reducing the two tests to only the short and fast spectral analysis could drastically cut down the test costs. Nevertheless, spectral analysis, which leads to a global evaluation of the deformations induced by the ADC on the converted signal, does not give direct access to local information such as Differential Non-Linearity. But, in practice, the detection of the Integral Non-Linearity should allow us to bind the maximal value of DNL.

Following this idea, the objective of this paper is to evaluate the possibility of detecting static errors using only a dynamic test, i.e. the spectral analysis. In other words, the objective is to evaluate the coverage of static errors using a spectral analysis. The paper is organized as follows. Section 2 presents the overall objective. Section 3 details the proposed method. Then, this method is illustrated on a case study in section 4. Section 5 then proposes a validation of the procedure using a specific in-house tool.

2 Objective of the study

2.1 Overview

In an industrial test context, two successive test procedures are used to test ADCs: the histogram-based test to extract static parameters and the Fast Fourier Transform (FFT) test technique to evaluate dynamic performances. The test conditions are different from one test technique to the other. The histogram-based test requires a lot of samples in order to achieve satisfactory statistical results. For this technique, the stimulus may be a sine wave or a linear signal with peak-to-peak amplitude A_{in} higher than the Full Scale range of the ADC under test ($A_{in} > FS$). On the contrary, the FFT test technique requires fewer samples and uses a sine wave signal with input amplitude lower than FS ($A_{in} < FS$) [5]. Generally, the test flow is optimized in terms of total test time by processing firstly the FFT test, and then the histogram-based test. Such a classical test flow can be described as shown in figure 1.

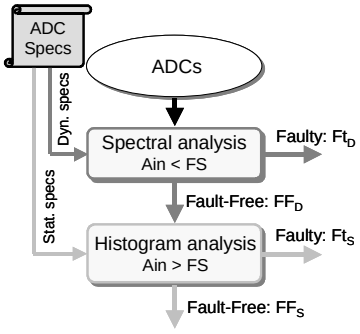

Figure 1. Classical ADC Test flow

Firstly, the FFT test is applied to each ADC in order to detect the ones whose dynamic parameters are beyond the dynamic specifications. These circuits, which are faulty in terms of dynamic performances (Ft_D), are rejected, while the fault-free circuits (FF_D) are secondly put through a histogram-based test to detect those whose static parameters overrun specifications. Faulty devices with respect to static specifications (Ft_S) are rejected while fault-free devices (FF_S) pass the test. By the end of the test flow, only ADCs meeting both dynamic and static specifications are binned as healthy circuits.

Processing successively the two test techniques is both time and hardware resources consuming. Each of these techniques only allows one to test one kind of ADC specifications. However, as both static and dynamic parameters define the overall ADC behavioral performances, they should be dependent on each other. In this context, the idea is to study this dependency and more particularly to quantitatively evaluate the efficiency of measuring dynamic parameters extracted from a classical FFT test to detect static errors. This analysis would then permit one to choose whether performing only a FFT test is a viable option or whether the histogram-based test must be included in the global test procedure.

We can suppose that a testing procedure restricted to the sole classical spectral analysis will not achieve the same detection performances as the complete test flow. In order to improve the number of rejected faulty devices, we can investigate the contribution of an additional test procedure also based on spectral analysis. Figure 2 presents the corresponding alternative ADC test flow.

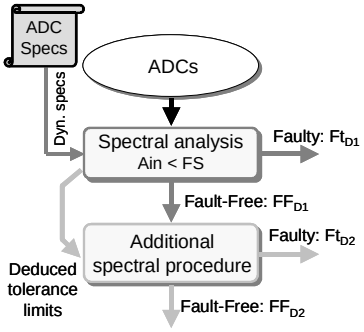

Figure 2. Alternative ADC Test Flow

The objective of the alternative test flow is to enhance the detection of faulty instances while preserving the ADC production yield. This constraint means that none of the fault free components (instances meeting both static and dynamic specifications) should be rejected by the additional spectral procedure. In this aim, we have to extract from the previous classical spectral analysis the adequate tolerance limits for the parameters evaluated by the complementary spectral procedure.

The final aim of the study is to choose the best test flow for a given test application. This involves an estimation of each possible test flow performances in terms of faulty device detection efficiency and testing time.

2.2 Test efficiency definition

The test efficiency corresponds to the ability of the different test flows to detect faulty devices. Actually, as the classical FFT-based test procedure detects by definition all the faulty devices with respect to dynamic specifications, the test efficiency represents the aptitude of the considered test flow to detect faulty devices in terms of static specifications that would be detected by a histogram-based procedure.

In a population of ADCs to be tested, each instance is either fault-free (FF_S) or faulty (Ft_S) versus given static specifications, and either fault-free (FF_D) or faulty (Ft_D) versus considered dynamic specifications. Considering the correlations between static and dynamic parameters, we expect that several components which are faulty in terms of static specifications are also faulty versus

dynamic requirements and will be rejected by a spectral analysis. The efficiency of the dynamic test procedure is thus defined as follows:

$$\xi = \frac{n_{(Ft_S \cap Ft_D)}}{n_{Ft_S}} \quad (1)$$

where $n_{(Ft_S \cap Ft_D)}$ represents the number of faulty instances according to static specifications whose measured dynamic parameters are also beyond dynamic specifications, and n_{Ft_S} is the total number of faulty instances in the population with respect to static specifications.

3 Method

To evaluate the efficiency of the test flows, we adopt a statistical approach rather than an analytical one [6][7]. In order to study a population of ADCs, we built a database of behavioral ADC models affected by the different possible combinations of static errors in a given range. We can then simulate every converter model in the population, estimate its dynamic features through a given spectral-based procedure and perform subsequent analysis on the distribution of the measured dynamic parameters.

3.1 Model of ADC testing environment

The typical test setup for ADC dynamic testing on a classical Automated Test Equipment (ATE) is illustrated in figure 3. The waveform synthesizer generates a sine wave signal with input frequency f_{in}, amplitude A_{in} and offset V_o. This stimulus is applied to the converter input and resulting output codes are transferred to the DSP (Digital Signal Processor) for further processing: extraction of the dynamic parameters from a FFT performed on the digital sample set. Note that coherent sampling is usually used to guarantee that each sample carries unique and independent information. Coherence consists in acquiring an integer number N of samples at frequency f_s that are equally spaced over an integer number M of identical signal periods, with N and M relatively prime. When coherent sampling is achieved, the stimulus fundamental component and each of its harmonics fall precisely on single lines of the spectrum in the frequency domain. This fact allows a more precise module measurement of the spectral components, leading to better results in terms of dynamic parameter measurements. Coherence also permits one to minimize the number of samples considered for the test.

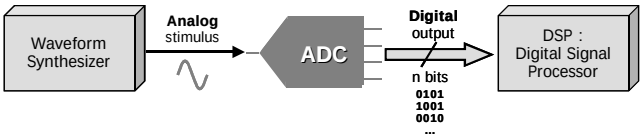

Figure 3. ADC testing environment

This experimental setup has been implemented using the *LabView* software.

Test conditions defining the test stimulus can be configured in the waveform synthesizer model and the DSP model allows us to perform any kind of spectral procedure.

We consider a behavioral model of ADC presenting a stair shaped transfer function. In case of an ideal *n*-bit ADC, the transfer function exhibits (2^n-*1*) equally spaced transition levels over the full scale range (*FS*) of the converter. The width of a step (between two successive transition levels) is a quantum or Least Significant Bit (*LSB*), given by:

$$q = 1\ \mathrm{LSB} = \frac{FS}{2^n} \quad (2)$$

In case of a real converter, the transfer function is affected by some non-idealities characterized by the static parameters. An offset error can be simply modeled by adding (or subtracting) the same quantity to all transition levels, resulting in a horizontal shift of the ideal transfer function. A gain error is modeled by multiplying all transition levels by the same factor, resulting in a compression or dilation of the ideal transfer function. Non-linearity errors are modeled by individual variations of the transition levels, resulting in a deviation of the actual transfer function from the ideal one.

3.2 Statistical efficiency evaluation

We have developed an in-house automatic tool allowing us to evaluate the statistical efficiency of the test flows for any test context. The tool is composed of two modules.

The first module has been defined to generate various ADC populations varying the ADC resolution, the number of instances in the population and the discretization step and ranges of the injected static errors.

The second module uses the model of ADC testing environment previously described to evaluate the test detection efficiency. To this end, we have to specify, for a given population, the test procedure requirements, i.e. the test conditions, ADC specifications and the kind of spectral analysis procedure. The automatic tool then extracts the dynamic parameters associated to the test procedure and displays the histograms of the corresponding dynamic parameter measurement distributions over the considered ADC population. On these histograms, the tool distinguishes between devices

within and beyond the static specifications. It finally forecasts the efficiency of the considered test flows to reject faulty ADCs with respect to static specifications.

4 Case study

As an illustration of the proposed evaluation method, we consider a practical case study defined as follows:

ADC Under Test: - resolution = 8 bits

Static specs: - offset max = ± 2 LSB
- gain error max = ± 1 LSB
- INL max = ± 1 LSB

Dynamic specs: - SINAD min = 48
- SFDR max = -55 dB
- THD max = -55 dB

Test conditions: - number of samples = 1024
- number of periods = 103
- stimulus p-p amplitude = FS–4 LSB

First of all, we have to define a statistically valid population of ADCs. We have considered all the possible combinations of offset, gain and maximum INL values ranging between ± 6 LSB for the offset value, ± 3 LSB for the gain value and ± 3 LSB for the INL value with a discretization step of 0.1 LSB. This results in a total number of 450,241 different transfer functions that constitute the population under test. Note that we arbitrarily choose to confine the errors within the range of 3 times the nominal specifications. Hence, 18,081 among the 450,241 transfer functions correspond to ADCs with static parameter values within specifications, which relates to about 4% of the population.

4.1 Evaluation of a sole conventional FFT test procedure efficiency

We have simulated the complete population and recorded for each different transfer function the resulting measurement value of the dynamic parameters extracted from the classical FFT. Results are summarized on the distribution histograms given in figure 3: for each measured value of a given dynamic parameter, the white bin shows the total number of ADCs presenting the same dynamic feature and the dark bin indicates the corresponding number of ADCs satisfying the static specifications. Figure 3 also points out the value of the tolerance limits from the dynamic specifications for each dynamic parameter.

The efficiency of the single test procedure depends on the number of faulty devices (with respect to static specifications) detected as faulty by the dynamic test. As an illustration, table 1 summarizes the efficiency results obtained considering each dynamic parameter individually.

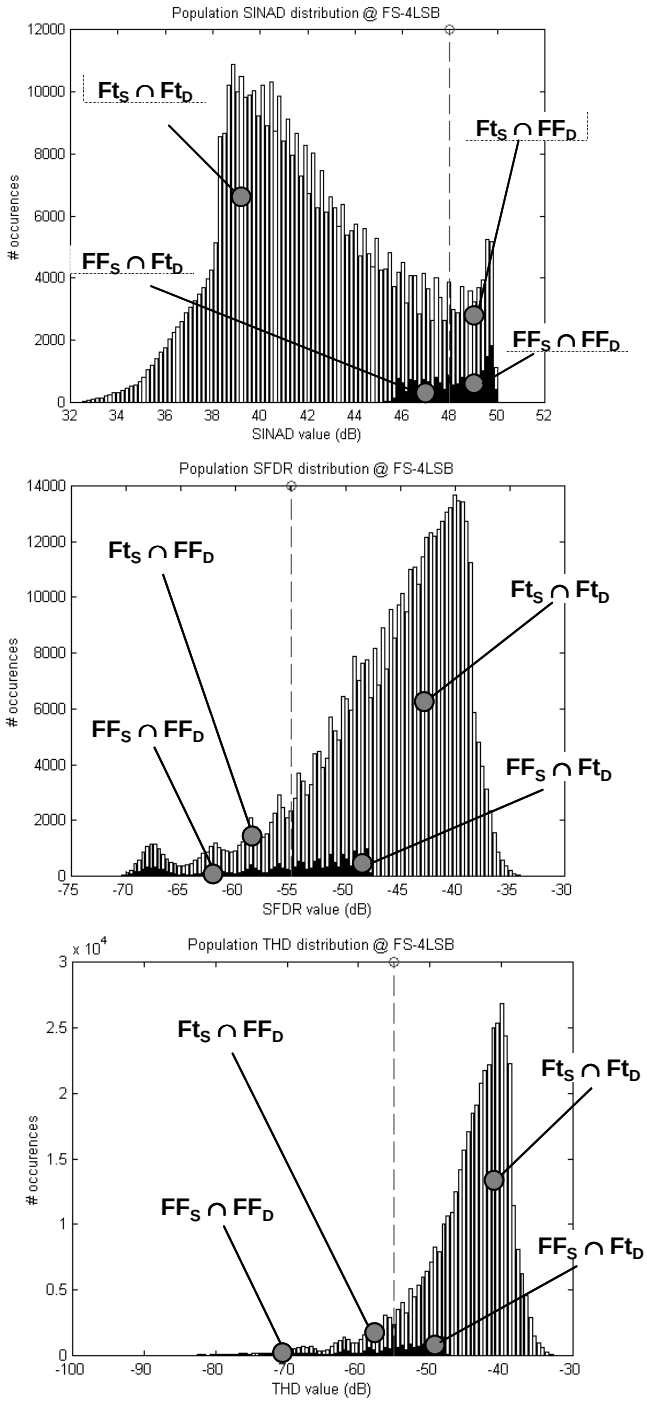

Figure 4. Distribution of the measured dynamic values for each dynamic parameter (SINAD, SFDR & THD) over the population with Ain < FS

Parameter	Dyn. Spec.	n_{Ft_S}	n_{Ft_D}	$n_{(Ft_S \cap Ft_D)}$	ξ
SINAD	> 48 dB	432160	410832	402841	**93.21%**
SFDR	< - 55 dB	432160	404888	394630	**91.31%**
THD	< - 55 dB	432160	416272	405971	**93.94%**

Table 1. Single test efficiency considering each dynamic specification individually

where $n_{Ft_S}, n_{Ft_D}, n_{(Ft_S \cap Ft_D)}$ represent respectively the total number of faulty instances with respect to static specifications, the total number of faulty instances with respect to dynamic specifications and the number of devices meeting neither static nor dynamic specifications. At this point, we should highlight that the test efficiency strongly depends on the considered dynamic tolerances. However for this case study, one can note that rather high efficiency rates are obtained. In particular, the THD measurement enables the best rejection with 93.94% of the faulty devices in the static field detected.

We can improve this result by correlating the detection results of each dynamic parameter measurement. Indeed, a given instance in the population may meet dynamic specifications for one parameter whereas overrun other parameters specifications. In practice, an ADC is considered as faulty as soon as one of its dynamic features does not fit specifications. Table 2 gives the result obtained with this combined analysis in the same conditions as previously.

Parameters	n_{Ft_S}	n_{Ft_D}	$n_{(Ft_S \cap Ft_D)}$	ξ
SINAD & SFDR & THD	432160	418970	408652	**94.56%**

Table 2: Test efficiency considering all dynamic specifications together

This result means that statistically for this case study, more than 94.5% of the faulty ADCs with respect to static specifications will be rejected via the dynamic parameters evaluation and combined analysis. This percentage can be satisfactory for some applications, allowing one to skip the histogram-based test. However, for more stringent applications, 5.5% of non-detected faulty devices may not be a viable option. In order to investigate whether this efficiency can be enhanced, we propose to complete the classical FFT test technique with an additional spectral test procedure. The combination of the classical spectral analysis with a complementary spectral procedure defines an alternative test flow.

4.2 Evaluation of the alternative test flow efficiency

Many solutions can be considered for the additional spectral procedure of our alternative test flow.

For example, we can perform a second spectral analysis using different test conditions than the first one. Note that unlike the histogram-based test conditions, the input stimulus in case of a classical FFT test procedure does not cover the full scale range of the converter (FS). Hence, the FFT analysis might not be representative of the same ADC behavior as the histogram-based test. Moreover, we have shown in [8] that some of the dynamic parameters are more sensitive to offset and gain errors when applying an input signal higher than FS, while others are more sensitive to non-linearity errors with an input signal lower than FS. Consequently, we propose to investigate whether adding a second FFT procedure with an input signal higher than FS would permit one to increase the efficiency of detecting static errors through the measurement of dynamic parameters. Note that even if one uses two FFT test procedures, the global test time will significantly be reduced in comparison with a classical test.

Regarding the second FFT test, the non-conventional test conditions imply that the measured dynamic parameters in this case are not representative of the datasheet dynamic specifications. It is therefore not possible to directly use the dynamic specifications to discriminate between fault-free and faulty circuits. Instead, new tolerance limits have to be set for the second FFT test.

The aim of the second FFT test is to detect faulty devices with respect to static specifications that escape the first FFT test, but without rejecting globally fault-free ones. Hence, we can simulate all converters passing the first FFT test and analyze the distribution of the dynamic parameters measured by the second FFT for converters satisfying the dynamic specifications. Tolerance limits are simply positioned so that none of the fault-free devices (with respect to static specifications) are rejected.

The new ADC test flow involving the two FFT tests is illustrated in figure 4. All the faulty converters from the dynamic point of view (Ft_{D1}) are rejected by the first spectral analysis since the dynamic specifications are used as tolerance limits. Among the converters that pass the first test, some of them present static parameters within specifications ($FF_S \cap FF_{D1}$) while others overrun static specifications ($Ft_S \cap FF_{D1}$). The second non-conventional FFT test is then applied to these converters using a tolerance box derived from the limits of the fault-free converter distributions.

This second test permits one to reject additional faulty devices (Ft_{D2}) while ensuring that all fault-free devices are still classified as fault-free.

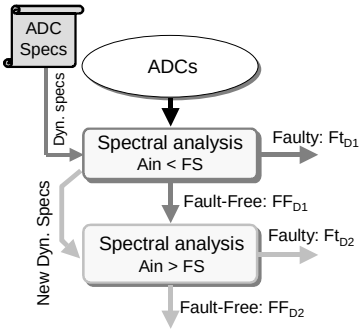

Figure 5. Two FFT test procedure

In order to evaluate the efficiency improvement induced by this second FFT test procedure, we have simulated, with input signal amplitude of FS+4LSB, the remaining population of ADCs not rejected by the first FFT test and measured the corresponding dynamic parameters. Figure 5 shows the distribution of the ADC dynamic parameters measurements: the clear bins give the total number of transfer functions within the first dynamic specifications (FF_{D1}) and the dark bins correspond to the number of instances satisfying both the static and datasheet dynamic specifications ($FF_S \cap FF_{D1}$). From these dynamic performance distributions, we can set the tolerance box at the limit of the dark bins range (fault free devices distribution range). This allows us to detect additional faulty devices together with ensuring that all fault free converters pass the test.

The test efficiency enhancement is directly related to the additional number of faulty devices detected by this second test procedure ($Ft_{D2} = Ft_S \cap FF_{D1} \cap Ft_{D2}$). Table 3 summarizes the global detection efficiency for each dynamic parameter individually and with a combined analysis of all dynamic parameters measurements:

Parameter	n_{Ft_S}	$n_{Ft_S \cap FF_{D1}}$	$n_{(Ft_S \cap FF_{D1} \cap Ft_{D2})}$	ξ
SINAD	432160	29319	4797	**94.3 %**
SFDR	432160	37530	14619	**94.6 %**
THD	432160	26189	4713	**95.0 %**
Combined	432160	23508	6307	**96.0 %**

Table 3: Global efficiency of the two-phase spectral test technique

where n_{Ft_S} and $n_{Ft_S \cap FF_{D1}}$ represent respectively the total number of faulty instances with respect to static specifications and the number of those of them that also pass the classical FFT test. The number of these last ones that fail the second FFT test is $n_{(Ft_S \cap FF_{D1} \cap Ft_{D2})}$, which then represents the additional number of faulty devices detected by the second FFT test procedure.

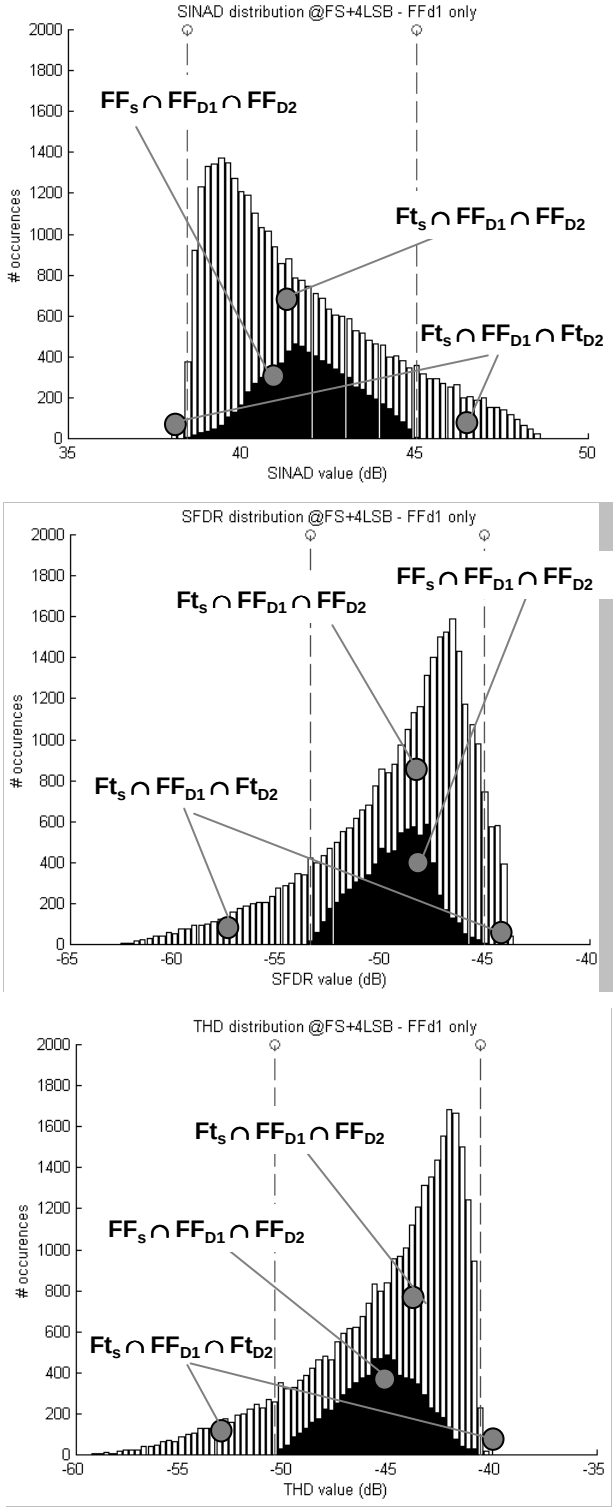

Figure 6. Distribution of the measured dynamic values (with A_{in} > FS) for each dynamic parameter (SINAD, SFDR & THD) over the population appreciated as fault-free by the classical FFT procedure (FF_{D1})

Thanks to the second spectral analysis procedure, 96% of the faulty ADCs in terms of both static and dynamic specifications can be detected without a time consuming histogram-based test technique. This statistical computed efficiency enables to choose a priori the best test flow for a given trade-off between test time and test selectivity.

4.3 Testing time issue

To summarize, when a spectral-only test procedure gives satisfactory efficiency, the gain in terms of test time is proportional to the difference between the number of samples required for a classical test flow on the one hand and for our optimized test flow on the other hand. Each FFT test procedure requires as a minimum one sample per ADC code bin [3], whereas the histogram-based test requires at least 10 samples for each code in order to achieve satisfactory statistical results with a coherent sampling [9]. Consequently, the histogram-based procedure lasts ten times longer than a single spectral test, and hence a complete classical test procedure with both FFT and histogram tests is eleven times more time consuming than a single optimized FFT test procedure. Even if the desired efficiency implies to compute a second spectral analysis with different test conditions, the optimized test flow is still more than five times shorter than the classical one.

5 Validations

We have illustrated through a case study the methodology we propose to evaluate the efficiency of measuring ADC dynamic parameters to detect ADC static errors. As a generalization, it is interesting to study the different tendencies of this FFT-based test strategy depending on ADC specifications. Moreover, we can validate our method by applying it to existing ADC specifications.

5.1 Specification influence

It is obvious that the efficiency of the spectral test procedure to detect ADC static errors strongly depends on the specified tolerance limits for both static and dynamic parameters. Thanks to the automatic tool described previously, we are able to evaluate this efficiency for any kind of specifications. As an illustration, we consider three different types of ADC specifications:

#1: relaxed dynamic specifications in comparison with static specifications. In other words the number of fault-free instances with respect to dynamic specifications is higher than the number of instances satisfying static specifications.

#2: tight dynamic specifications in comparison with static specifications. In this case the number of fault-free devices with respect to dynamic specifications is lower than the number of instances satisfying static specifications.

#3: equivalent tolerances on static and dynamic specifications. The number of fault-free devices is about equivalent according to dynamic or static specifications.

The evaluation tool has been run on these three test contexts considering both a single FFT test procedure with input signal amplitude lower than FS and a double FFT test procedure with input signal amplitude lower than FS and higher than FS. Results are summarized in table 4.

	Offset (LSB)	Gain (LSB)	INL (LSB)	SINAD (dB)	SFDR (dB)	THD (dB)	ξ FFT1	ξ FFT1 + FFT2
#1	2	1	1	40	-40	-40	**34.3%**	**63.2%**
#2	2	1	1	49	-67	-68	**99.5%**	**99.8%**
#3	2	1	1	44	-50	-50	**85.9%**	**89.6%**

Table 4: Test flow efficiency according to each kind of specification

At first glance, these results demonstrate that the efficiency of a sole classical dynamic test to detect faulty devices might be really significant. According to our statistical prediction, up to 99.5 % of faulty ADCs can be detected by a sole classical FFT test procedure in the case #2. This case corresponds to the best achievable detection rate as far as the chosen dynamic limits meet the dynamic parameters values that a perfect ADC would exhibit, i.e. the most stringent dynamic specifications.

In the case #1 we can see that a single classical FFT test procedure only allows one to detect 34% of the faulty ADCs (with respect of static specifications). In this case where the dynamic tolerance limits are excessively relaxed the second FFT test procedure significantly enhances the global detection of faulty ADCs. In spite of the second test detection improvement, the poor efficiency value in this kind of applications forces us to use a classical test flow.

An exploration of the specification influence tendencies on the expected detection efficiency has been developed in [10].

5.2 Application to manufacturer ADC datasheets

The above exploration of the specification influence on the forecasted detection efficiency is derived from the arbitrary specification set of the previous case study. It reveals that the proposed alternative spectral-only test flow is not a generic solution viable in any test context,

but can be a valuable time-saving option in case of stringent applications. Generally, the specifications from manufacturers' component catalogues mentioning constraints for both static and dynamic parameters are rather tight. We can then expect that our alternative method will be attractive for many applications. For illustration, we present in table 5 the predicted statistical efficiency for three real sets of tolerance limits corresponding to 8-bit converters available on the market:

A. Specifications associated to component TLV571 from *Texas Instruments*.

B. Specifications associated to component AD7822 from *Analog Devices*.

C. Specifications associated to component AD7468 from *Analog Devices*.

	Offset (LSB)	Gain (LSB)	INL (LSB)	SINAD (dB)	SFDR (dB)	THD (dB)	ξ FFT1	ξ FFT1 + FFT2
A	0.8	1	0.5	47	-52	-51	**89.7%**	**95.7%**
B	1	2	0.75	48	-55	-55	**94.6%**	**95.3%**
C	0.5	0.5	0.5	49	-65	-65	**98.3%**	**99.8%**

Table 5: Test flow efficiency in case of real specifications

The efficiency of a sole conventional spectral analysis in specification case A only allows to detect 90% of the devices whose static parameters are beyond tolerances, but a complementary spectral procedure using non-conventional test conditions leads to the additional detection of 6% of the faulty instances in the population. Hence, the alternative flow combining two FFT procedures can be an interesting trade-off between test time and test selectivity depending on the application. In case B, the additional spectral analysis using an input signal amplitude superior to the full scale range of the converter under test does not improve significantly the expected detection efficiency of the classical spectral analysis. When the application allows that about 5% of the faulty components escape the test, the sole conventional dynamic procedure seems therefore to be the best trade-off as far as it requires a testing time twice shorter than the other alternative solution. Finally, the high detection efficiency expected in case C for both proposed FFT-only test procedures should enable their use in most application contexts.

6 Conclusion

In this study, we have investigated the possibility of replacing the classical ADC test procedure by a shorter and less expensive one solely based on spectral analysis. In order to evaluate the viability of such an approach, we have developed a methodology allowing one to predict the ability of a spectral-based analysis to detect ADC static errors. The prediction of the test efficiency is based on a statistical analysis of the distribution of the measured dynamic parameters according to given tolerance limits for a wide population of ADCs. The methodology has been implemented in an automatic tool allowing us to handle different test conditions, different converter specifications and different test procedures. In particular, we have investigated whether complementing the classical FFT test by a second FFT test with non-conventional test conditions would permit to enhance the efficiency of detecting static errors. Thanks to the test efficiency prediction, one can choose a priori the best test flow for a given application and a given trade-off between test time and test selectivity.

Results have demonstrated that the efficiency of a classical FFT test might be really significant. However, this efficiency is strongly related to the converter specifications and to the considered population. The more stringent the dynamic specifications, the higher the efficiency. When relaxing the dynamic specifications, the efficiency quickly decreases. In this case, the use of a second FFT test under non-conventional test conditions permits the detection of some additional faulty devices, and therefore leads to an improvement of the efficiency. However for very relaxed specifications, this improvement may not be sufficient to guarantee the selectivity of this double FFT test procedure.

In order to further increase the efficiency of a dynamic-only test procedure, we are currently analyzing the faulty devices that escape the test. In particular, we are trying to identify some common features that would help us in understanding the weakness of the current procedure. This analysis may provide some clues towards the definition of additional parameters to evaluate that would maximize the detection of static errors.

Other work in progress concerns the population considered for the statistical analysis, with a detailed study of the impact of the faulty to fault-free ratio within the population, and the customization of the population with respect to a given process to enhance the validity of the statistical prediction of test efficiency.

7 References

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