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# Efficient Scan Chain Design for Power Minimization During Scan Testing Under Routing Constraint

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## Abstract

*Scan-based architectures, though widely used in modern designs, are expensive in power consumption. In this paper, we present a new technique that allows to design power-optimized scan chains under a given routing constraint. The proposed technique is a three-phase process based on clustering and reordering of scan cells in the design. It allows to reduce average power consumption during scan testing. Owing to this technique, short scan connections in scan chains are guaranteed and congestion problems in the design are avoided.*

## 1. Introduction

The full-scan design is considered to be the best DfT discipline [1]. It can be automated using commercially available design tools. Over the years, it has gained widespread acceptability in system design environments and is now commonly used to test digital circuitry in integrated circuits (ICs) or System-on-Chip (SoC) cores. However, scan-based architectures are expensive in power consumption as each test pattern requires a large number of shift operations with a high circuit activity [1]. This elevated test power may be responsible for several kinds of problems: instant circuit damage, increased product costs, decreased system reliability, performance degradation and decrease of overall yield. A survey of these problems is given in [2].

It is of course possible to reduce average power during scan testing by simply scanning at a lower frequency. However, this increases test application time. Another solution is to add logic to hold the output of the scan cells at a constant value during scan shifting [3]. The drawbacks of this approach are the area overhead and the performance degradation that it incurs, as well as the negative impact on the design flow. Some other solutions have been proposed recently to cope with the power problem during scan testing [4-9].

Actually, a simple alternative solution for minimizing power consumption during scan testing is to use test vector ordering or scan cell ordering techniques. Test vector ordering has been investigated in [10-12] with the objective to define the order in which test vectors of a deterministic test set have to be applied to the circuit or core under test (CUT) to minimize toggling. Scan cell

ordering has been investigated first in [10] and more recently in [13]. In the latter technique, a simple yet effective heuristic procedure is proposed. The inputs to this procedure are i) a given set of scan flip-flops and ii) a sequence of deterministic test vectors with the corresponding output responses. The output is an ordered scan chain with minimum test power. To tackle this NP-hard problem efficiently, the heuristic procedure operates in two steps: the first one consists in determining the chaining of the scan cells so as to minimize the occurrence of transitions in the scan chain during shifting operations, the second one consists in identifying the input and output scan cells of the scan chain to limit the propagation of transitions during scan operations. This approach works for any conventional scan design - no extra DfT logic is required - and reduces test power up to 58 % without modifying the initial fault coverage and test length.

However, one of the main concern when designing a scan chain in traditional DfT flows is to take care of the scan routing. After scan synthesis, connecting all the scan cells together may cause routing congestion during the place-and-route stage of the design flow, resulting in area overhead and timing closure issues. To avoid congestion problems, scan chain optimization is traditionally used after placement. Formally, scan chain optimization is the task of finding a new order for connecting the scan elements such that the wire length of the scan chain is minimized. Several scan chain reordering solutions have been proposed recently to address the above stated problems [14-17].

The main drawback of the scan cell ordering technique proposed in [13] is that power-driven chaining of scan cells cannot guarantee short scan connections and prevent congestion problems during scan routing. In this context, the use of a power-driven scan ordering solution, though efficient, is questionable. To avoid this situation, we propose a new solution that allows to design power-optimized scan chains under a given routing constraint. The routing constraint is defined as the maximum length accepted for scan connections, but it can also be defined as a maximum value for the total wire length of the scan chain. The proposed solution consists in the three following steps. First, scan cells that belong to a same region of the chip are grouped together to form clusters.

The number of clusters is a user-defined parameter established with respect to the routing constraint. Next, the power-driven scan cell ordering procedure given in [13] is used to reorder scan cells in each cluster. Each cluster thus contains a sub scan chain with minimum test power and has definite input and output scan cells. Finally, the output scan cell of each cluster is linked to the input of its closest neighbor according to a predefined cluster ordering.

The proposed technique for designing power-optimized routing-constrained scan chains offers numerous advantages. It works for any conventional scan design – no extra DfT logic is required – and can be easily inserted in any traditional DfT flow – by simply reporting the scan chain optimization stage after ATPG. The proposed technique does not modify the fault coverage and the test time, and can be easily extended to deal with industrial designs that contain multiple scan chains and multiple clock domains. Owing to this technique, short scan connections are guaranteed and congestion problems are avoided. Experiments on the biggest ISCAS'89 benchmark circuits have shown significant reductions in terms of power consumption during scan testing compared to layout-driven ordering solutions provided by an industrial synthesis tool.

The remainder of the paper is organized as follows. In the next section, we remind the power-driven scan chain reordering technique proposed in [13]. In Section 3, we present the approach proposed to design scan chain with minimum test power under routing constraint. In Section 4, experimental results obtained on the benchmark circuits are reported and discussed.

## 2. Power-driven scan chain reordering without routing constraint

In [13], a simple yet effective heuristic procedure is proposed to minimize test power by appropriately ordering the scan cells of a given scan chain. The inputs to this procedure are i) a given set of scan flip-flops and ii) a sequence of deterministic test vectors with the corresponding output responses. The output is an ordered scan chain with minimum test power. The heuristic procedure operates in two steps. The first one consists in determining the order in which the scan cells have to be connected to minimize the occurrence of transitions in the scan chain during scan-in and scan-out operations. The set of scan vectors (test vectors and output responses) is used for this task. The second step consists in appropriately identifying the input and output scan cells of the scan chain to minimize the propagation of transitions in this scan chain during shifting operations. For more details on this procedure, the reader is asked to refer to [13].

Although it can significantly reduce the power consumed during scan testing, the main drawback of the ordering technique proposed in [13] is that it can create routing congestion and/or too long scan connections in the design. This is simply due to the fact that no routing constraint is

considered during scan cell reordering. To highlight this point, we report in Figure 1 the scan chain routing obtained with the above technique on circuit s9234. (ISCAS'89 family - 228 scan flip-flops). Only one scan chain and only one clock domain have been assumed for this experiment. In the graph shown in Figure 1, nodes represent the position of scan cells in the chip and edges represent connections between scan cells. The position of scan cells has been obtained after synthesis with the tool "Silicon Ensemble" of Cadence Design System [18]. Scan connections have been determined by the algorithm given in [13]. Although the reduction in average power consumption during scan testing achieves 22.4 % (compared with a layout driven ordering provided by "Silicon Ensemble"), it can be seen that the resulting wire length is highly non-optimal and that the scan routing has a high degree of congestion. In addition to area overhead and congestion issues, timing closure is another issue in such situation. The problem in this case is due to the existence of long scan connections that additionally load scan cell outputs and hence decrease the chip performance.

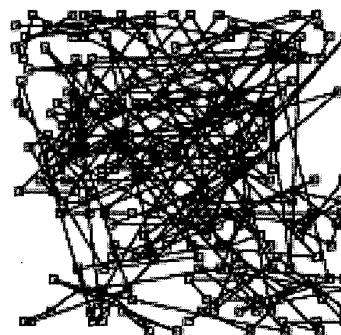


Figure 1: Power-driven scan chain routing on circuit s9234 without routing constraint

Complete results on the biggest ISCAS'89 circuits are provided in Section 4 of this paper. For each circuit, it is shown that the same conclusion can be drawn: performing power-driven scan chain reordering without considering routing always leads to a high degree of congestion and to long scan connections in the design. A solution to solve this problem is given in the next section.

## 3. Scan chain design with minimum test power under routing constraint

### 3.1. Overview of the proposed approach

With sub-micron technologies, routing in VLSI systems has become a critical factor. Wire delays may represent up to 75 % of the total delay path in a design, and with ever smaller feature sizes, this ratio can only grow. Meanwhile, the silicon area due to wiring in a design is unceasingly increasing. In this context, the use of a power-driven scan optimization technique as the one proposed in [13], though efficient, is questionable.

To guarantee short scan connections and prevent congestion problems during scan routing, we propose a new solution that allows to design power-optimized scan chains under a given routing constraint. The routing constraint is defined as the maximum length accepted for scan connections, but it can also be defined as a maximum value for the total wire length of the scan chain. The proposed solution is a three-phase process that can be applied once scan synthesis, placement and ATPG tasks have been performed. First, scan cells that belong to a same region of the chip are grouped to form clusters. Next, the power-driven scan cell ordering procedure presented in [13] is used to reorder scan cells within each cluster. Finally, the output scan cell of each cluster is connected to the input of its closest neighbor according to a predefined cluster ordering. The full scan chain obtained by this way is guaranteed to offer a good tradeoff between test power reduction and minimum scan routing. Each one of these three phases is described in the following sub-sections.

### 3.2 Clustering in the design

Clustering in the design consists in grouping together cells that belong to a same region of the chip to further allow scan connections only between cells of a same region and hence avoid long scan connections in the design. Clustering also allows the degree of congestion to be reduced – by transforming the most congested area into several less congested sub-areas - and the total wire length to be minimized.

The number of clusters in the design and the number of scan cells in each cluster is a user-defined parameter established with regard to the routing constraint. Formally, the stronger will be the constraint on the longest scan connection, the higher will be the number of clusters. On another hand, the higher will be the number of clusters, the lower will be the reduction in test power on the final scan chain. In fact, with a high level of clustering, most of the scan cells are connected based on the closest neighbor criteria and only a few of them are connected according to test power optimization. Consequently, the best tradeoff between test power reduction and length of the longest scan connection has to be found by the user to efficiently determine the number of clusters for each design.

A lot of different solutions can be used to perform the clustering operation. As for defining the number of clusters, the way to make these clusters will be defined by the user considering parameters such as placement of flip-flops in the design (in order to deal with situations in which flip-flops are not equally distributed over the design), compatibility with the number of scan chains and clock domains (see details in §3.5), existence of one or more groups of pre-connected scan cells, ... In our experiments, clustering has been performed simply by defining a number of clusters and operating a squaring on the design with respect to this number. Each cluster is thus defined geographically with respect to the design and

contains scan cells of a same region. For simplicity, all the clusters in our approach have the same area but may contain a different number of scan cells. It is however very easy to modify the clustering process so that the number of scan cells in each cluster being the same. An example of the clustering process applied on circuit s9234 is reported in Figure 2. In this example, the number of clusters is 16 and the number of scan cells within each cluster ranges from 4 to 21.

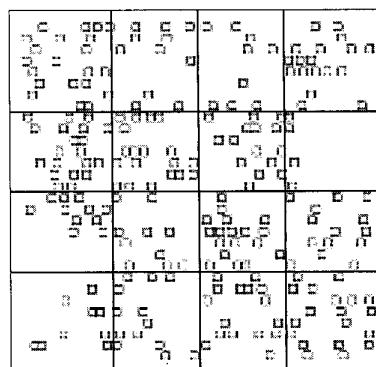


Figure 2: Clustering in circuit s9234 - 16 clusters

### 3.3 Scan cell reordering within a cluster

Once clusters in the design have been defined, scan cell reordering within a cluster is done by using the power-driven scan cell ordering procedure presented in [13]. Here, the inputs to this procedure are i) the set of scan cells belonging to the considered cluster, and ii) the corresponding bits of these scan cell in the sequence of deterministic test vectors and output responses. For example, consider the test set shown in Figure 3, which is composed of four test vectors ( $V_1$  to  $V_4$ ) and the corresponding four output responses ( $R_1$  to  $R_4$ ).

	sc1	sc2	sc3	sc4	sc5	sc6	sc7	...	scn	
$V_1 = 1$	1	0	1	0	1	0	...	1		
$R_1 = 1$	0	1	1	0	0	0	...	1		
$V_2 = 0$	0	1	0	0	1	1	...	0		Cluster Ck
$R_2 = 0$	0	0	0	1	0	1	...	0		sc2
$V_3 = 0$	1	1	1	1	1	1	...	1		sc3
$R_3 = 1$	1	0	1	1	1	0	...	0		sc5
$V_4 = 0$	1	0	1	1	0	0	...	0		sc6
$R_4 = 1$	1	0	0	0	1	0	...	1		

Figure 3: A scan chain before reordering within a cluster

This set of vectors is provided by an ATPG tool assuming a random initial order of the scan cells in the scan chain. In this example, scan cell 1, denoted as sc1, corresponds to bit 1 in each scan vector, scan cell 2, denoted as sc2, corresponds to bit 2, and so on. Consider now that four scan cells (sc2, sc3, sc5, sc6) among the  $n$  scan cells of the design are in the same region and hence belong to the same cluster Ck. In this example, the subset of bits to

consider during scan cell reordering within cluster  $C_k$  will be the one highlighted in grey in Figure 3.

From the scan cells in the considered cluster and the corresponding subset of bits, it is then possible to determine the best scan cell order within the cluster. The best scan cell order is the one that assures a minimum toggling during scan operations within the cluster. It is obtained by applying the procedure described in [13] and, in our example, leads to the following result: the final order of scan cells within cluster  $C_k$  is  $sc2-sc6-sc3-sc5$ , where  $sc2$  is the input cell and  $sc5$  the output cell of cluster  $C_k$ . Details to obtain this result can be found in [13]. The next step in this phase consists in performing scan cell reordering within another cluster, and to continue until all clusters in the design have been reordered.

### 3.4 Cluster ordering

The last phase of the proposed scan chain design technique consists in connecting all clusters in the design so as to obtain the final scan chain. This is done by connecting the output scan cell of each cluster to the input of its closest neighbor according to a predefined cluster ordering. In addition to reduce routing congestion and prevent long scan connections, the full scan chain obtained by this way is guaranteed to offer a good tradeoff between test power reduction and full scan routing minimization.

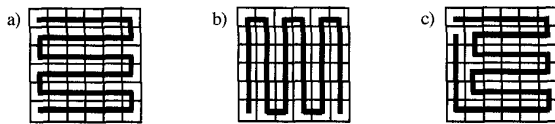


Figure 4: Different styles of cluster ordering

Connecting clusters to form one or several scan chains can be done following different ways. The only requirements are i) to have each cluster connected to one of its closest neighbors to satisfy the constraint on the longest scan connection, and ii) to get through all clusters in the design to have all scan cells included in the final scan chain (s). Due to its exponential nature, solving this problem optimally is not a good option (this is an NP-hard problem). A better option is to use linear-time algorithmic solutions. As our main motivation in this work was more to demonstrate the feasibility and efficiency of our approach than proposing a new algorithm for a graph traversal problem, we decided to implement a simple solution based on a given style of cluster ordering. This solution is depicted in Figure 4.a and consists in connecting clusters simply by following the  $x$ -axis direction. Of course, several other simple cluster orderings could be defined, for example by following the  $y$ -axis direction (Figure 4.b) or by considering the position of scan in and scan out pins (Figure 4.c). As for the clustering process described in §3.2, the way to connect clusters to form scan chain (s) has to be defined by the user considering its design knowledge and constraints. In the

rest of this paper, results are all based on the cluster ordering shown in Figure 4.a.

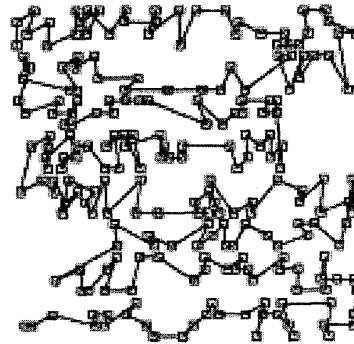


Figure 5: Power-optimized routing-constrained scan chain design for circuit s9234

In order to estimate the global efficiency of our approach, we report in Figure 5 the new scan chain routing obtained on circuit s9234 with the proposed scan chain design technique. Compared to the power-driven scan routing obtained on the same circuit and depicted in Figure 1, it is clear that the new solution greatly reduces the degree of congestion as well as the total wire length of the scan chain. The number of clusters in this example is equal to 64, which allows to guarantee short scan connections. The reduction in average power consumed during scan testing is roughly equal to 6 %. This percentage is a test power comparison between the proposed scan ordering technique and the layout-driven ordering produced by “Silicon Ensemble” [18]. As mentioned at the beginning of the paper, it is possible to tradeoff between test power reduction and scan routing minimization. In the case the number of clusters is equal to 16, the test power reduction is equal to 12.1 % instead of 6 %. However, the degree of congestion is higher and the total wire length of the scan chain is greater than in Figure 5.

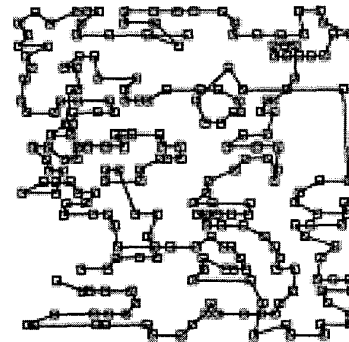


Figure 6: Scan chain routing on circuit s9234 obtained with “Silicon Ensemble”

For further discussion, we report in Figure 6 the scan chain routing obtained on circuit s9234 with the layout synthesis tool “Silicon Ensemble”. Compared to the scan routing

obtained with our technique and shown in Figure 5.a, it can be seen that the degrees of congestion and the lengths of scan connections are quite similar. Our solution, however, has a test power which is 6 % lower than that provided by "Silicon Ensemble".

### 3.5 Practical issues

For the sake of clarity, we presented our approach by making the assumption that only one scan chain and only one clock domain are used in each design. However, it is common in industrial designs to have multiple scan chains and multiple clock domains. Moreover, scan chains in those designs are often balanced, *i.e.* the number of scan cells is roughly the same for all scan chains. The number of scan chains can be equal, greater or smaller than the number of incompatible clock domains [16].

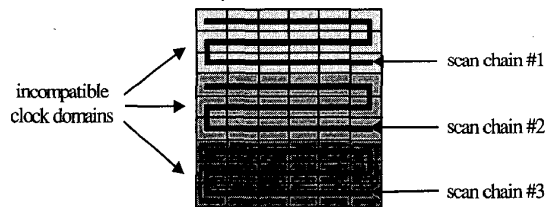


Figure 7: An example with 3 clock domains and 3 scan chains

Extending our approach to the more general case in which multiple scan chains and multiple clock domains exist is very easy. It can be done by adding some preliminary steps to the process described above. For example, before grouping cells that belong to a same region of the chip to form clusters, we can group all scan cells based on the clock domain compatibility. Generally, cells belonging to the same clock domain are also in the same region of the chip. So, this grouping based on the clock domain compatibility delimits a number of zones in the design so that the clustering operation can be done within each zone separately. For example, consider a design in which three clock domains and three scan chains are required (Figure 7). Extending our approach in this example may consist in performing clustering and scan chain design in each zone separately and then obtain the result shown in Figure 7.

## 4. Experimental results

The benchmarking process described here was performed on biggest circuits of the ISCAS'89 benchmark suite. Power consumption in each circuit was estimated by using PowerMill [19], assuming a clock frequency equal to 200 MHz and a power supply voltage of 2.5 V. Experiments performed on each circuit have been done with technology parameters extracted from a 0.25 $\mu$ m digital CMOS standard cell library. The goals of the experiments we performed have been i) to measure the reduction in test power obtained with the proposed scan optimization technique according to the number of clusters defined in each circuit, and ii) to analyze the impact of clustering on

the overall scan chain routing (having in mind that the degree of congestion is always reduced and that short scan connections are always guaranteed).

Circuit	# scan cells	# gates	# patterns	FC (%)
s5378	179	2225	145	99.05
s9234	228	4678.5	249	93.99
s13207	669	6395.5	354	98.99
s15850	597	7987	279	97.84
s35932	1728	16726.5	112	100

Table 1: Main features of the experimented circuits

First, structural characteristics and test parameters of the experimented circuits are reported in Table 1. All experiments are based on deterministic testing from the ATPG tool "TestGen" of Synopsys [20]. The missing faults in the fault coverage (FC) column are the redundant or aborted faults. The first part of Table 1 shows the number of scan cells and the number of gates for each benchmark circuit. The primary inputs and primary outputs were not included in the scan chain, but were assumed to be held constant during scan-in and scan-out operations. In the second part, we report the test length of each test sequence and the corresponding fault coverage. An important point to note is that the proposed scan optimization technique does not modify these values.

Results obtained on the ISCAS'89 benchmark circuits are listed in Table 2 and Table 3. The results were obtained following the style of cluster ordering shown in Figure 4.a. For each circuit, we first report the average power reductions (P %) obtained during scan testing with respect to the number of clusters. These results are expressed in percentage and represent a test power comparison between the proposed scan ordering technique and the routing-driven ordering produced by "Silicon Ensemble". The average power reductions are those measured in the scan chain of each circuit and not those measured in the logic part of the circuit. For CPU time reasons, simulating all the deterministic patterns for measuring the power consumption in the logic part of each circuit cannot be done, while this is possible for measuring the power consumption in the scan chain. Although the power consumed in the scan chain is normally lower than the power consumed in the logic part of a circuit, the correlation between both has been demonstrated more than once and can be easily verified [6]. In these conditions, power reductions in the scan chain are as representative as power reductions in the logic part of each circuit to highlight the effectiveness of the proposed technique.

The main conclusion we can draw from these results is that power reduction decreases when the number of clusters increases. For circuit s9234, the power reduction ranges from 22.4 % with 1 cluster to 3.5 % with 128 clusters. Results obtained with 1 cluster are actually those obtained with the technique presented in [13] in which no

routing constraint is considered. Regarding the proposed technique, these results were totally predictable.

Clusters	s5378		s9234		s13207	
	P %	WL	P %	WL	P %	WL
1	29.1	9.7E+4	22.4	1.2E+5	26.4	5.9E+5
2	19.2	7.2E+4	20.6	9.4E+4	19.5	4.4E+5
4	19.8	5.1E+4	15.8	8.2E+4	17.9	3.1E+5
16	12.3	3.4E+4	12.1	5.5E+4	14.4	1.8E+5
32	7.9	2.6E+4	7.6	4.3E+4	14.4	1.4E+5
64	2.7	1.8E+4	5.8	3.5E+4	8.1	1.1E+5
128			3.5	2.9E+4	3.9	8.9E+4
256					1.7	7.4E+4
Wire length obtained with "Silicon Ensemble"						
-		1.19E+4		2.01E+4		5.08E+4

Table 2: Average power reduction and total wire length w.r.t. number of clusters

Clusters	s15850		s35932	
	P %	WL	P %	WL
1	17.8	5.0E+5	19.6	3.3E+6
2	14.9	3.9E+5	18.0	2.5E+6
4	15.2	2.7E+5	16.6	1.6E+6
16	11.3	1.6E+5	13.1	8.3E+5
32	8.9	1.3E+5	11.1	6.2E+5
64	6.6	1.0E+5	8.9	4.2E+5
128	3.7	8.4E+4	6.1	3.3E+5
256	3.3	7.2E+4	3.3	2.4E+5
512	6.8	6.2E+4	0.5	2.0E+5
1024			0.0	1.7E+5
Wire length obtained with "Silicon Ensemble"				
-		5.00E+4		1.29E+5

Table 3: Average power reduction and total wire length w.r.t. number of clusters

Next, we give the values of the scan wire length (WL - in  $\mu\text{m}$ ) obtained with the proposed technique. These results show that the total wire length of the scan chain decreases when the number of clusters increases, thus proving the efficiency of our clustering process. For circuit s9234, it can be seen that there is almost one order of magnitude between the wire length with 1 cluster and the wire length with 128 clusters. In the latter case, we can see that the test power reduction is still equal to 3.5 %, whereas the wire length of the scan chain obtained with the layout-driven ordering provided by "Silicon Ensemble" - 2.01E+4 - and that obtained with our technique - 2.90E+4 - are in the same order of magnitude. These results also show that it is possible to efficiently tradeoff between test power reduction and wire length minimization for big circuits. Thought not formally proven by experimental results, it is important to recall that the degree of congestion is always reduced and that short scan connections are always guaranteed with the proposed technique.

A last comment on these results is about the time taken by the proposed technique to provide a power-optimized routing-constrained scan chain for a given circuit. This time is always less than one hour for the biggest ISCAS'89

benchmark circuits and increases only linearly with the number of scan cells in the circuit.

Among the possible ways to continue this work, a first direction will be to extend our approach to deal with more representative designs containing multiple scan chains, multiple clock domains and lockup latches. Also, work will be done for optimally defining the clusters and for optimally defining the cluster ordering.

## References

- [1] M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing", Kluwer Academic Publishers, ISBN 0-7923-7991-8, 2000.
- [2] P. Girard, "Survey of Low-Power Testing of VLSI Circuits", IEEE Design & Test of Computers, Vol. 19, N° 3, pp. 82-92, May-June 2002.
- [3] A. Hertwig and H.J. Wunderlich, "Low Power Serial Built-In Self-Test", IEEE European Test Workshop, pp. 49-53, 1998.
- [4] S. Wang and S.K. Gupta, "ATPG for Heat Dissipation Minimization for Scan Testing", ACM/IEEE Design Auto. Conf., pp. 614-619, 1997.
- [5] J. Saxena, K.M. Butler and L. Whetsel, "A Scheme to Reduce Power Consumption During Scan Testing", IEEE Int. Test Conf., pp. 670-677, 2001.
- [6] R. Sankaralingam, R. Oruganti and N. Touba, "Static Compaction Techniques to Control Scan Vector Power Dissipation", IEEE VLSI Test Symp., pp. 35-42, 2000.
- [7] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault and S. Pravossoudovitch, "A Gated Clock Scheme for Low Power Scan Testing of Logic ICs or Embedded Cores", IEEE Asian Test Symp., pp. 253-258, 2001.
- [8] K-J. Lee, T-C. Huang and J-J. Chen, "Peak-Power Reduction for Multiple-Scan Circuits during Test Application", IEEE Asian Test Symp., pp. 453-458, 2000.
- [9] A. Chandra and K. Chakrabarty, "Combining Low-Power Scan Testing and Test Data Compression for System-on-a-Chip", ACM/IEEE Design Auto. Conf., pp. 166-169, 2001.
- [10] V. Dabholkar, S. Chakravarty, I. Pomeranz and S.M. Reddy, "Techniques for Reducing Power Dissipation During Test Application in Full Scan Circuits", IEEE Transactions on CAD, Vol. 17, N° 12, pp. 1325-1333, December 1998.
- [11] P. Girard, C. Landrault, S. Pravossoudovitch and D. Severac, "Reducing Power Consumption during Test Application by Test Vector Ordering", IEEE Int. Symp. on Circuits and Systems, CD-Rom proceedings, 1998.
- [12] P. Girard, L. Guiller, C. Landrault and S. Pravossoudovitch, "A Test Vector Ordering Technique for Switching Activity Reduction during Test Operation", IEEE Great Lakes Symp. on VLSI, pp. 24-27, 1999.
- [13] Y. Bonhomme, P. Girard, C. Landrault and S. Pravossoudovitch, "Power Driven Chaining of Flip-flops in Scan Architectures", IEEE Int. Test Conf., pp. 796-803, 2002.
- [14] M. Hirech, J. Beausang and X. Gu, "A New Approach to Scan Chain Reordering Using Physical Design Information", IEEE Int. Test Conf., pp. 348-355, 1998.
- [15] S. Makar, "A Layout-Based Approach for Ordering Scan Chain Flip-flops", IEEE Int. Test Conf., pp. 341-347, 1998.
- [16] L. Guiller, F. Neuveux, S. Duggirala, R. Chandramouli and R. Kapur, "Integrating DFT in the Physical Synthesis Flow", IEEE Int. Test Conf., pp. 788-795, 2002.
- [17] D. Berthelot, S. Chaudhuri and H. Savoj, "An Efficient Linear-Time Algorithm for Scan Chain Optimization and Repartitioning", IEEE Int. Test Conf., pp. 781-787, 2002.
- [18] "Silicon Ensemble", Cadence Design System Inc., 2000.
- [19] PowerMill, Version 5.4, Synopsys Inc., 2000.
- [20] TestGen, Version 5.3, Synopsys Inc., 1999.