A Novel SCR-Based Protection Structure Against ESD with Efficient Multi-Finger Triggering

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Abstract:

In this paper, a new SCR-based protection structure is presented relying on the bimodal operation of a LSCR. STMSCR is multi-finger compliant thus allowing area-efficient design of pad-located ESD protection. Without any process customisation, an HBM failure threshold over 115V/µm is reached for the first time while always ensuring current uniformity in multi-finger structures.

1. Introduction

With technological scaling, the largest width in a pad available for local ESD protection is dependent on the IO pitch and can be smaller than 40µm for the advanced designs. Even by considering the most efficient ESD protection devices, protection level requirements cannot be met in such a small width without considering multi-finger protection structures.
In nowadays CMOS technologies, the most common protection structures are based on GGNMOS or LSCRs [1-5]. Recently, multi-finger triggering issue has been successfully addressed for GGNMOS-based structures (MFT-NMOS [1]) but their ESD protection level per surface is inherently limited by the performances of the GGNMOS itself (as defined in [6-7]). In contrast, LSCR-based structures are known to exhibit a very high ESD protection level per surface. However, LSCR multi-finger triggering has never been reported up to now.
This paper presents a novel SCR-based structure with multi-finger triggering ability. It is called STMSCR standing for Smart Triggered Multi-finger SCR [8]. The principle of the structure is first introduced in section 2. Design issues regarding triggering voltage adjustment and latch-up immunity are then discussed in section 3. Silicon results are finally presented in section 4 demonstrating the superior ESD performances of the proposed STMSCR.

2. STMSCR Principle

The proposed protection device is based on a classical LSCR with minimum design rule dimensions. Such a LSCR exhibits very different behaviours depending on the Nwell tap biasing. The basic idea is to exploit these different behaviours to develop a bimodal protection structure controlled by an external triggering circuitry. STMSCR can then switch from a transparency mode to a protection mode as soon as an ESD event is detected. In addition, the structure width as well as the number of fingers can be adjusted in order to meet the protection level requirements and to fit into any IO cell.

2.1. Transparency mode

Fig.1 shows the cross-section and the simplified schematic of a SCR in transparency mode where both substrate and cathode taps are tied to the ground whereas the Nwell tap is tied to the anode. This mode is equivalent to use a regular LSCR device.

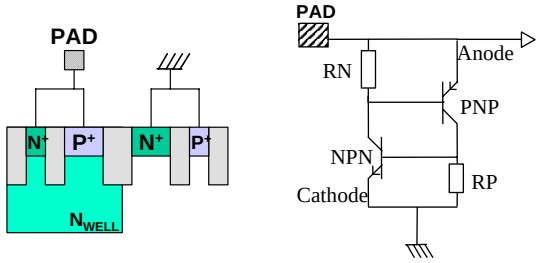

Fig.1. Biasing configuration in transparency mode.

Fig.2 presents the experimental DC curve measured for such a LSCR in a 0.18µm technology. The central junction being reverse-biased, only the leakage current of the Nwell/Psub junction is observed. The triggering of this structure may only occur if an overshoot above the breakdown voltage of this junction happens. Since breakdown voltages of the technologies are always far above supply voltages, this guarantees the transparency of the structure during normal operations. As a consequence, it appears immune against false triggering.

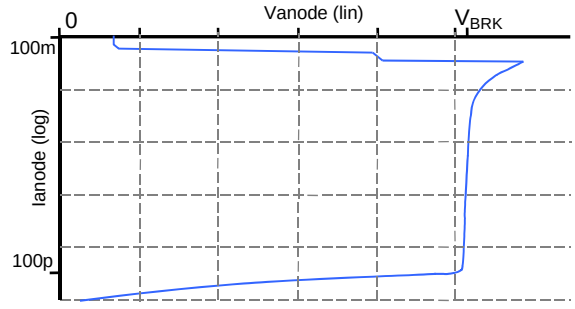

Fig.2. Experimental SCR I-V curve in transparency mode.

2.2. Protection mode

Fig.3 shows the cross-section and the simplified schematic of the proposed SCR in protection mode where both substrate and cathode taps are tied to the ground whereas the Nwell tap is connected to the ground through a resistive element.

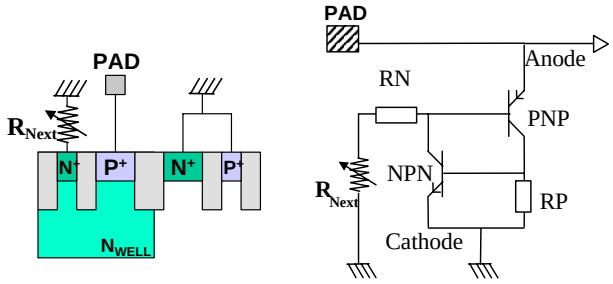

Fig.3. Biasing configuration in protection mode

Fig.4 depicts the experimental DC I-V curves of the structure in this configuration with two different values of the external resistance. Before the triggering, the PNP emitter-base junction (P+/Nwell junction) is forward-biased and the PNP bipolar transistor is active whereas NPN base-emitter voltage is not large enough to allow it to drive current. Thus, current can flow from the pad to the ground through the base and collector of the PNP with a well-controlled rise of the pad voltage. When the PNP delivers enough current to the NPN base-emitter voltage to reach a specific value (roughly 0.8V), the classical SCR triggering occurs. So, the triggering current is provided by the PNP bipolar action and not by any avalanche mechanism. Thus, the current is easily spread uniformly along the width of the structure and between the fingers.

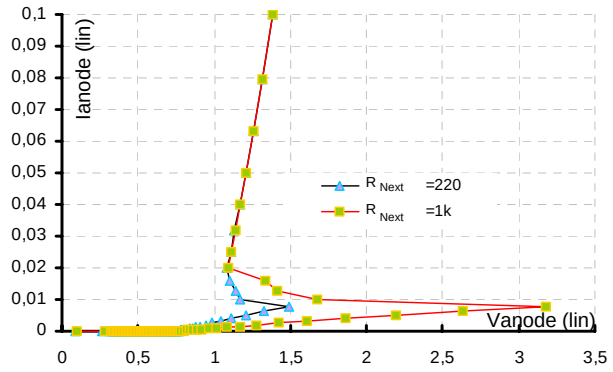

Fig.4. Experimental SCR I-V curves in protection mode with two different external resistance values.

Compared to the previous situation it can be observed that the triggering point is highly reduced whereas holding point does not change (V_H is around 1V, far smaller than the one of GGNMOS-based structures). This means that the triggering condition can be easily dissociated from the operating behaviour. Depending on the external resistance value, it is therefore possible to adjust the triggering point without impacting ESD efficiency unlike previous solution as LVTSCR for example.

2.3. Mode switching circuitry

Fig.5 show the cross-sectional view and the simplified schematic of the proposed bimodal protection structure. The transition from one mode to the other is driven by an external triggering circuit including a CMOS inverter and a CR ESD detector. The CMOS inverter allows to connect the Nwell tap either to the anode through the PMOS transistor (transparency mode) or to the ground through the NMOS transistor (protection mode). The CR ESD detector is used to control the state of the CMOS inverter. Essentially during ESD stress conditions, a voltage transient on the pad will be detected by the CR cell and causes the state of the inverter to commute from PMOS-driven to NMOS-driven so that the STMSCR turns from its transparency mode into its protection mode.

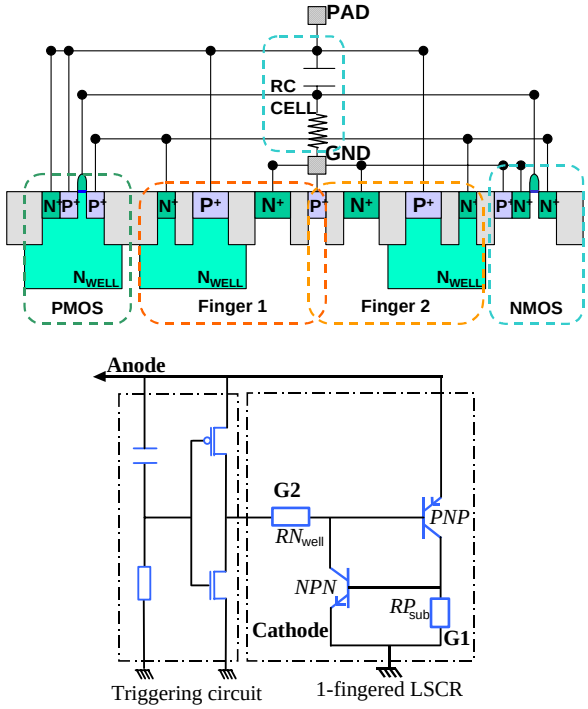

Fig.5 . Cross section of a 2-fingers STMSCR (top) and circuit schematic (bottom) of a 1-finger STMSCR.

3. STMSCR Design

The design of the STMSCR is based on a modular approach. Each device part can be designed, verified and optimised to tailor the final device regarding IC design specifications and required ESD performances. In particular, an electrical model of a 1-finger LSCR has been developed allowing to probe the current flowing through the anode and the Nwell tap. This model has been validated against silicon with an excellent agreement between simulated and measured I-V characteristics. In this section, we use this model to analyse multi-finger LSCRs with their associated triggering circuitry, leading to a straightforward design.

3.1. Inverter design

The inverter acts as a resistance connecting the Nwell tap either to the anode or to the ground depending of its control gate voltage. The main parameter of the CMOS inverter is the drain-to-source resistance of the NMOS transistor, which determines the triggering voltage. PMOS dimensions are also critical since it reduces the risk of triggering during normal operations. Guidelines to design this transistor are the same than those published in [9]. Yet, attention must be paid to minimize its capacitance with respect to the anode.

In order to minimize area, the NMOS transistor can be designed with minimum length; its width then permits to adjust its on-resistance. The only constraint is that the NMOS transistor must be wide enough to drive the pre-trigger current (base current of the PNP transistor) without failure. Experiments have established that this current typically remains in the range of few tens of milliamps. Hence, the NMOS transistor can be implemented without salicide blocking, resulting in a reduced area.

However the ESD protection level may be limited by the snapback triggering of the NMOS transistor. Indeed, if the SCR resistance is too high, the anode voltage may increase over the NMOS snapback voltage for high current magnitudes. In that case, the inverter design can be adapted by inserting a resistance in series with the inverter and reducing accordingly the NMOS on-resistance (increased W). The NMOS drain voltage is then a smaller part of the anode voltage, avoiding snapback triggering and resulting in higher protection level.

Fig.6 shows simulated TLP I-V curves (zoomed in the triggering region) with three different NMOS widths. These curves are obtained by applying TLP pulses directly on the anode and on the inverter gate, without using the RC detector. It clearly appears that the triggering voltage V_{t0} can be reduced at convenience by increasing the NMOS width. The proper sizing of the NMOS transistor therefore allows to adjust the triggering voltage in the desired ESD protection window.

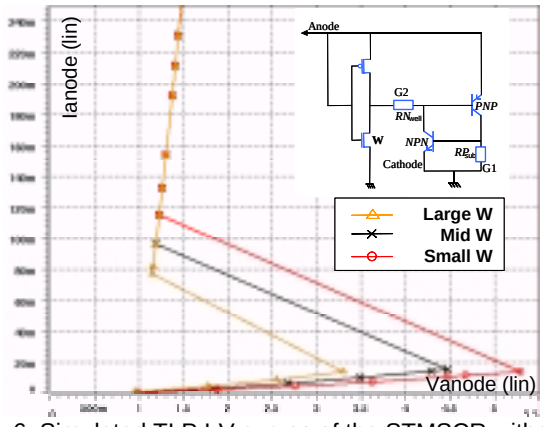

Fig.6. Simulated TLP I-V curves of the STMSCR without RC cell with three different NMOS widths.

Such a STMSCR (with its gate tied to the anode) directly acts in a protection mode as soon as the gate (i.e. anode) voltage is above the NMOS' threshold voltage. As a consequence, it would not be transparent during normal operation: even if the triggering voltage was above the supply voltage, the leakage current would be too large during the normal operation. This is the reason why an ESD detector has been added.

3.2. CR cell design

The CR cell provides the control gate voltage of the CMOS inverter. It is intended to generate a gate voltage above the threshold voltage of the NMOS as soon as an ESD event occurs while maintaining a gate voltage below the threshold voltage of the NMOS transistor during normal operation.

Hence, the ESD detector basically consists in a high-pass filter since an ESD event typically exhibits very fast transient (e.g. 1 to 10ns rise time for an HBM ESD event). The STMSCR triggering voltage then depends on the time constant of the CR cell.

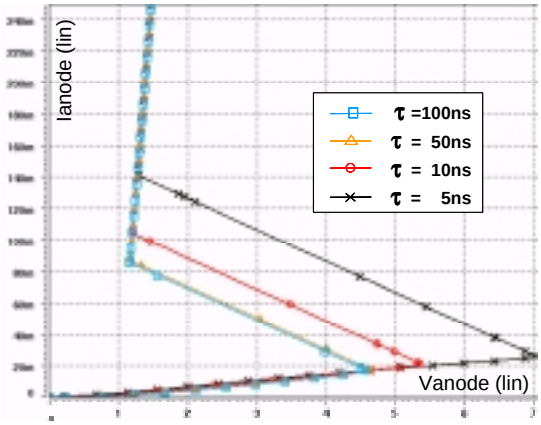

Fig.7 . Simulated I-V curves of the STMSCR with three different τ when applying a current ramp.

For illustration, Fig.7 gives simulated STMSCR I-V curves with four different time constant values when applying a current ramp. A duration of 10ns was chosen for the ramp since an HBM ESD event with a rise time tr_{ESD}=10ns corresponds to the worst case energy that must be discharged by the protection circuit. As expected, results show that the triggering voltage V_t decreases as the time constant τ increases. However, it should be pointed out that further increasing the time constant will not decrease the triggering voltage anymore. In fact, with $\tau > 5\ tr_{ESD}$, the lower achievable triggering voltage V_{t0} for this structure has been reached (see fig.6).

Regarding practical implementation, the CR cell design can be optimized through mere electrical simulations including the rest of the circuit in order to meet the specifications in terms of area, transparency, speed, trigger voltage and latch-up immunity. It should be emphasized that unlike NMOS-based clamping device [10] where the CR signal should detect an ESD event and drive the cell as long as the ESD event is present, once triggered the STMSCR will remain on by its own latching mechanism. The RC signal is therefore no more needed to control the operation of the protection. Compared to NMOS clamping system, a small capacitance can be used for the STMSCR reducing the total area consumed by the ESD protection.

4. Results and discussion

STMSCR structures were implemented in 0.18µm, 0.13µm and 0.09µm technologies. They were successfully validated in 0.18µm and they are currently being validated in 0.13µm and 0.09µm.

This section reports silicon results demonstrating multi-finger operation with an EMMI picture and ESD performances with TLP and HBM results.

4.1. EMMI (Emission Microscopy

Fig.8 is a dynamic EMMI picture of a 4-finger STMSCR after triggering. This picture has been obtained by applying 200ns-wide TLP pulses during 15s of exposition. The four stripes of light indicate that the current is flowing uniformly in each finger after triggering.

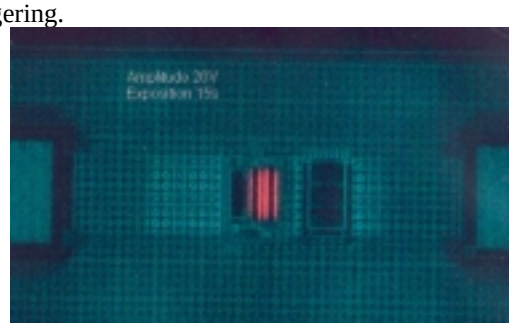

Fig.8. Dynamic EMMI picture of a 4-finger STMSCR.

4.2. TLP results

Fig.9 reports TLP measurements obtained in a 0.18µm technology for a set of 4-finger STMSCRs. Herewith, both NMOS size and CR detector were modified. Results show that the triggering voltage is adjustable by the designer depending on the triggering circuit specifications. Moreover, the same behavior is observed for all structures once triggered. Since the EMMI pictures show a uniform conduction of the current among the fingers, this means multi-finger triggering is ensured whatever the design of the triggering circuitry.

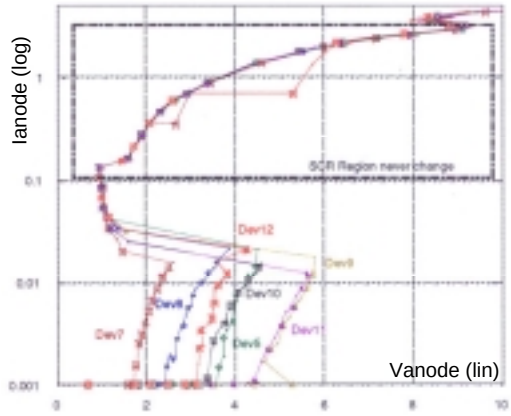

Fig.9. Experimental TLP I-V curves of the STMSCR with different triggering circuits.

The measured holding voltage is very low, roughly 1.2V. First experiments in 0.13µm and 0.09µm technologies have pointed out that the holding voltage remains above this value, hence guaranteeing intrinsic latch-up free operation.

4.3. HBM results

STMSCR exhibits very high protection level compared to previous art SCR-based structures. HBM results obtained in a 0.18µm technology are shown in table 1. Failure threshold over 8 kV_{HBM}, limited by the ESD tester, is observed for a structure involving two fingers of 35µm each. This corresponds to a protection level higher than 115 V_{HBM}/µm and 6 V_{HBM}/µm^2, which is the best reproducible result ever reported [5] for multi-finger structures.

Table1. HBM results for various SCR-based structures

	LSCR	*MLSCR*	*LVTSCR*	***STMSCR***
HBM failure threshold [V]	4.75 k	3.5 k	4.5 k	**>8 k**
HBM result per micron[V/µm]	85	50	64	**>115**

5. Conclusion

This paper presents a novel SCR-based ESD protection structure called STMSCR. It is optimised for multi-finger devices. Silicon proven results were obtained with 2 and 4-finger STMSCRs in 0.18µm and are expected in 0.13µm and 0.09µm. EMMI pictures, TLP and HBM results show a uniform conduction of the current between the fingers, a good control of the triggering voltage, and high protection capability. In this structure, latch-up immunity is achieved during normal operation by disabling the trigger capability of the LSCR in a 0.18µm technology. Latch-up issue will be less critical in 0.13µm and 0.09µm. Furthermore, STMSCR is designed without salicide blocking and does not require any extra process step.

Acknowledgments:

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