Power Conscious Testing

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Abstract. Test power relates to the power consumed during test of integrated circuits or embedded cores. Test power is now a big concern in large System-on-Chip designs. In this paper, we propose to shortly review the state-of-the-art in this domain. We first survey the recent approaches proposed for minimizing test power. Next, we propose some interesting directions for the development of new low power testing techniques by enumerating the relevant criteria that have to be satisfied.

1. Introduction

The System-on-Chip (SOC) revolution has brought some new challenges to both design and test engineers. Among these challenges, power dissipation is one of the important issues [1]. Generally, a circuit may consume more power in the test mode than in the normal mode [2]. It has been shown in [3] that the test power can be as high as twice the power consumed in the normal mode. There are several reasons for this increased test power. First, the test efficiency has been shown to have a high correlation with the toggle rate; hence in the test mode, the switching activity of all nodes is often several times higher than the activity during normal operations. Secondly, in a SOC, parallel testing is frequently employed with the aim to reduce the test application time; this may result in excessive energy and power dissipation. Third, the design-for-testability (DfT) circuitry embedded in a circuit to reduce the test complexity is often idle during normal operations but may be intensively used in the test mode. Another reason is that successive functional input vectors applied to a given circuit during system mode have a significant correlation, while the correlation between consecutive test patterns can be very low [4]. This can cause significantly larger switching activity in the circuit during test than that during its normal operation. Since power dissipation in CMOS circuits is proportional to switching activity, this excessive switching activity during test may be responsible for cost, reliability, performance verification, autonomy and technology related problems [5]. For example, in battery-powered devices, the power consumed during application of power-up or periodical on-line tests, which are often implemented resorting to the Built-In Self Test (BIST) approach, can dramatically shorten the battery lifetime. Another example of such problems is that increased circuit activity and hence power consumption leads to increased current flows during test, making the use of expensive packages for the removal of excessive heat an imperative need. Increased heat leads also to serious silicon failure mechanisms, such as electro-migration, that reduce the reliability of a system operating under such conditions. A detailed description of these problems is proposed in [5].

2. Terminology

As discussed earlier, one of the current concerns, which may turn into a major engineering problem in the future of SOC development, is test power [6]. As both the SOC designs and the deep-submicron geometry become prevalent, the hugeness of designs, the tightening of timing constraints, the rising of frequencies, and the lowering of applied voltages all affect the power consumption systems of silicon devices [7]. These concerns involve energy, average power, peak power, instantaneous power and thermal overload. Below are some definitions.

Energy: the total switching activity generated during test application. Energy has impact on the battery lifetime during power up or periodic self-test of battery operated devices.

Average Power: the total distribution of power over a time period, which is generally the amount of power consumed during the application of a test. The average power is given by the ratio between the energy and the test time. Elevated average power adds to the thermal load that must be vented away from the device under test. It may cause structural damage to the silicon (hot spots), to bonding wires or to the package.

Peak Power: the highest value of power at any given instant. The peak power determines the thermal and electrical limits of components and the system packaging requirements. If the peak power exceeds a certain limit, the correct functioning of the entire circuit is no longer guaranteed. - In fact, the time window for the definition of the peak power is related to the thermal capacity of the chip, and forcing this window to one clock period is sometimes just a simplifying assumption. For example, if the circuit has a peak power consumption during only one cycle but it has power consumption within the limit of thermal capacity of the chip for all other cycles, the circuit will not be damaged because the energy consumed, which corresponds to the peak power consumption times one cycle, will not be enough to elevate chip temperature over the limit of thermal capacity of the chip (unless the peak power consumption is far higher than normal power consumption). In order to damage the chip, high (not only highest) power consumption should last for several cycles to consume enough energy that can elevate chip temperature over the limit.

3. Related work on test power

Until now, a number of ad hoc solutions have been practiced in industry for considering power consumption during test. These solutions consist in over-sizing power supply, package and cooling to stand the increased current during testing, or reducing the test operation frequency. Unfortunately, these solutions increase either hardware costs or test time, and may lead to a loss of defect coverage as dynamic faults may be masked. Thereby, a number of novel solutions have been proposed to cope with the power and energy problems during test. These approaches can be classified as follows:

1) *Test Scheduling Algorithms* [3,8,29,30,31,35,38]. The goal in these approaches is to determine the blocks of a complex SOC design to be activated in parallel at each stage of the test session in order to reduce the number of concurrently tested modules. The average test power is reduced and consequently, the temperature related problems avoided by the increase of the test time duration.

2) *Vector Filtering BIST Techniques* [9,10]. As each vector applied to the CUT consumes power but not every vector generated by the pseudo-random TPG contributes to the final fault coverage, the vector filtering architectures consist in preventing application of non-detecting vectors to the CUT. This approach is very effective in reducing average test power without reducing fault coverage.

3) *Low Power BIST Test Pattern Generators* [4,11-14]. TPGs based either on LFSRs or Cellular Automata (CA) are carefully designed to reduce the activity at circuit inputs, thus reducing power consumption. These approaches effectively reduce test power but sometimes at a cost of sub-optimal fault coverage.

4) *Circuit Partitioning Techniques for BIST* [15]. This approach consists in partitioning the original circuit into structural sub-circuits so that each sub-circuit can be successively tested through different BIST sessions. The average power, the peak power and the energy consumption during BIST are minimized at a low expense of area overhead and with no loss of fault coverage.

5) *Low Power ATPG Algorithms* [16-18]. New ATPGs are proposed with the intent of generating test patterns able to reduce test power in addition to the classical ATPG objectives (fault coverage and test length).

6) *Vector or Scan Latch Ordering Techniques* [19-21,32,33,34,36,37,40]. These are techniques in which the switching activity of a CUT is reduced by modifying either the order in which test vectors of a given test sequence are applied to this CUT, or the order in which the scan flip-flops are chained to form the shift register, or the way according which Xs in test vectors are assigned to 0 or 1. These techniques are normally usable during ATE testing.

7) *Static Compaction and Input Control Techniques* [22,23]. The goal of these techniques is to minimize the scan vector power dissipation. This is done by either appropriately compacting test vectors of a test sequence, or by applying a specific blocking vector at the beginning of each scan shifting operation.

8) *Scan Path Modification Techniques* [24-26]. These techniques propose to modify the scan architecture in such a way that the switching activity in the CUT is minimized during scan shifting operations. This is accomplished by either adding delay buffers among the scan chains [24], or by segmenting the original scan chains into several sub-scan chains [25,26].

9) *Clock Scheme Modification Techniques* [27,28,39,41]. These techniques consist in modifying the clock scheme connected to the CUT and/or to the scan chains to either partially disable the clock signal, or to reduce the clock rate during the test session without increasing the test time. In certain cases this technique is improved by rearranging the test vectors.

4. Discussion

As can be observed, the number and the diversity of the available techniques are quite important, and hence the selection of one of them by a designer or a test engineer who is interested in implementing such a technique depends on a number of parameters. Obviously, the first one is the context in which the technique has to be implemented; external testing, scan testing, scan-BIST, parallel BIST, … will lead to completely different choices. For example, a test vector ordering technique can be utilized during ATE or scan testing, but cannot be used in a BIST situation where vectors' order is firmly defined by the generator. The second parameter concerns the way we want to act on the test power minimization; do we want to act on the test sequence or on the test architecture ? In the first case, we will select test vector ordering or compaction techniques (for ATE or scan testing). In the second case, we will prefer techniques as those presented in [25,26,27]. The third parameter is the possibility a designer or a test engineer has to relax some of the classical test constraints when implementing such a low power testing technique. Actually, there is a number of relevant criteria that must be considered when selecting solutions for minimizing test power. Fault coverage and test time, which are among the main test constraints, have to be unaltered by the implemented technique. The area overhead due to hardware modifications must be acceptably low [33]. The circuit performances have to be maintained. The impact on the design flow, and hence on the design time, must be low enough for the solution to be acceptable. Consequently, according to the importance attached by the designer or test engineer to each one of these constraints, the selection of a low power testing technique among the available ones will be different. This is due to the fact that the existing techniques, although they all minimize test power, have a different impact on the above criteria. For example, the test scheduling technique proposed in [3] for test power reduction during BIST will be used in situations where the test time is not a crucial test criterion. On the other side, techniques as those presented in [13,28] will be preferred if the test time has to be unmodified.

In addition to the above mentioned selection criteria, one of the most important point a designer or a test engineer has to take into account when selecting a solution for minimizing test power is the clock power. Results in [6] suggest that the clock power, which is the power dissipated in the clock tree each time the clock makes a transition, is a significant component of the total power during test. In some cases, it may dominate the logic power dissipated when logic gates in the circuit switch. For this reason, special care must be taken to the clock power. This means that the clock tree has to be designed as small as possible, or that clock signals can be disabled as often as possible as it is the case in traditional low-power systems.

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