An I.P. Migration and Prototyping Strategy Using Transistor Level Synthesis
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Abstract— Designers are today facing two challenges of conflicting objectives. In one hand they need to design for optimum performance and in the other hand they need to design in a minimum time frame (“time to market”) while using the latest up-to-date available technology. It becomes necessary for the designers to very quickly prototype IP blocks for any given technology. This paper describes a new approach based on transistor level layout synthesis for CMOS IP cores rapid prototyping (~100k transistors).

Index Terms—layout synthesis, virtual library, prototyping, technology migration, incremental optimization, transistor level, analytical modeling

I. INTRODUCTION

STANDARD cell libraries have been successfully used for years. However with the emergence of new technologies and the increasing complexity of designs, this concept becomes less and less attractive. Most of the time, cells are too generic and not well suited to the block being created. As a result the final design is not well optimized in terms of timing, power and area. Depending on the target application, today’s SoC may need to integrate the same IP block optimised using different criteria’s (Platform based design [1], [2]). Standard approaches try to resolve this problem by providing the designer with multiple libraries containing cells optimized under specific electrical constraints. As a consequence, IP’s generated using such a library will, most of the time, respect one specific constraint but will be over-fitted regarding other constraints. Moreover the development needed for every new technology and the maintenance of these standard libraries are very costly in term of time and in term of human resources. This can seriously impact time-to-market consideration during migration process.

Designers must be able to handle and quickly evaluate the design performance in the newest technology. Fast prototyping enables to increase the control on the trade-off between parameters such as speed, area and power consumption.

In this paper, we describe an investigation towards the use of transistor level layout synthesis to avoid employing a standard cell library and to allow designers to very quickly prototype “application-fitted” IP blocks for any given technology. It avoids the costs due to developing a standard cell library and mostly allows a quick evaluation of the performances of different flavours of a same IP.

The paper is organized as follows. In section II, we describe the standard cell approach and the newly emerging flows. In section III, we present our new flow based on transistor level layout synthesis and all the currently developed tools. And finally in section IV, we analyze the results obtained with this new “transistor level layout synthesis” tool called FP² before to conclude in section V.

II. DESIGN METHODOLOGIES

A. The standard cell based approach

In the “Standard Cell” flow [3], the layout of the design is directly generated from a behavioral description. First, it proceeds to a logical optimization and maps the Boolean equation to the target library. Then after placing and routing all the pieces of layout, representing the individual pre-characterized cells, the final layout is generated. The use of standard cells presents a well-understood trade-off. On the positive side, a standard cell library normally provides a set of pre-packaged functionalities. Each cell is speed and power characterized. Furthermore, the existing industrial EDA tools are relatively well adapted to this approach.

On the other hand some drawbacks appear:

• With new UDSM technologies where interconnects are of significant importance. It is more difficult to predict the cell drive and to satisfy the timing constraints. Various iterations are needed between each point-tool of the flow. This can seriously damage the flow convergence.

• In fact, it is well known that the quality of designs highly depend on the library that is being used [4] and of the variety of functionalities and sizes for each primitives gates [5]. Most of the designers recognize that standard cells are populated with "too generic" cells [6], and that significant improvements can be achieved just by resizing some existing cells (drive continuity) or by adding a few customized cells (design dependency) in the initial library.
B. New alternatives

New emerging approaches are proposed by industrial companies so as to avoid these problems:

- Timing consistency problem is resolved by using tools built around a unified data model [7]: data requirements relative to the physical design can be reached quickly by the tools thanks to this unique data structure.
- Problem concerning "drive continuity" is partly resolved by using the "Liquid Library" [8] concept: In this approach, a static base library is used for design synthesis. Then the structural representation is placed and routed. Usually during the optimization step, we notice that some cells of the base library are not well suited to the design. Afterward needed design dependent cells are automatically generated by a "cell Factory" and are engineering Change Order (ECO) placed (if possible) in the design.

Nevertheless, one main drawback still exists on these approaches: they are based on an already existing target library populated by a few hundred of logic gates specified to satisfy very specific area-performance tradeoffs. Consequently, the resulting IP block structures are forced to stay within the predetermined library precluding an optimal solution based on the total available design space of the available transistor structures.

Furthermore, the effectiveness of the standard flow methodology is highly dependent on the library development and process migration, which is costly.

III. AN ADAPTIVE LIBRARY CONCEPT BASED ON LAYOUT SYNTHESIS

We propose a standard cell independent based approach, working at transistor level. Theoretically, layout synthesis offers the possibility of overcoming deficiencies of the standard cell approach. The idea is that from a structural HDL description of a circuit, a synthesis tool would generate the optimized layout for the specified technology and timing constraints.

The main motivations for this approach are:

- First to avoid supporting the library and standard cell generation. This dependency is very costly in term of time (around 6 months to develop and characterize a library) and in term of human resources (around 5 people/month) while it only requires less than a day, using 1P2, to migrate to a new process by creating a new technology file.
- Secondly his approach enables to work at transistor level. Using the proposed methodology, each transistor can be individually sized or re-sized continuously (no discrete size limitations) at every stage of the flow.

Although this approach is not based on a standard cell library, we have to supply the logical synthesis commercial tool with a functionality set. We call this set the “virtual library”. To each function, we associate a virtual cell that can be considered as a set of connected transistors (at symbolic level, no layout generated). Virtual cells appear as an interface between synthesis, place and route and the layout generation. The vast set of functionalities in the virtual library is expected to imply less transistor count in the design.

The proposed flow takes as input a behavioral description of the circuit function (VHDL or Verilog). It is composed of the following steps:

- During the first one a high-level logic synthesis and optimization, and a technology mapping are realized using the virtual library.
- A transistor level synthesis step, at which the layout of the circuit is generated, using a set of constraints, a structural description of the design and the virtual library as inputs. This includes placement, routing, timing analysis, optimization and physical layout generation.

We develop a tool which achieves this last step. As it is illustrated in the Fig.1, the “transistor level layout synthesis” tool starts from a structural description of the circuit and generates the layout.

![Fig.1. 1P2 description.](image_url)

This approach is constituted of two major steps:

- The first one consists in creating the virtual cells from their functionality, resulting in an associated transistor network.
- The second phase achieves placement and routing based on physical estimations obtained from the targeted layout style. Timing analysis and optimization is realized during these two steps. This feature enables, step-by-step, more optimized and refined performance results regarding initial design constraints. Information exchanged between these tools is made through the common data structure as it is shown on the Fig. 2. The physical layout of each row is then automatically generated, with full respect of the technology rules.

The main problems to be addressed in constructing such a flow are as follows. It is firstly necessary to provide a transistor netlist with an optimal number of transistors for the required functionality. Another challenge is to predict and
optimize the timing and power characteristics of the circuit before the final layout availability. The last challenge consists in generating a dense layout of the netlist, based on well-specified technology rules.

Let us now consider in more detail the different steps of this layout synthesis approach.

A. Layout style

As virtual cells don’t have predefined layout, it is necessary to deal with layout generation. The chosen style for the transistor-level generation is a variant of the popular “linear-matrix” [9]. The layout of the circuit is constructed by a sequence of NMOS and PMOS transistor rows. This style is principally characterized by the minimization of the space between the two N and P diffusion zones. Routing is realized over the diffusion zones (gain in terms of area) and avoids the use of metal 2 to save the porosity of each row and to facilitate the routing step.

B. “Virtual Library” a new concept

The set of cells constituting the “Virtual Library” is mostly composed of complex gates. As a consequence the number of cells available is virtually unlimited (in terms of logical functionality). The constraints are only fixed by the target technology and performance limitations (maximum number of serial transistors).

In addition, as the final layout will be automatically generated, the driving capability of all these “virtual cells” can be continuously adapted, at the contrary of the discrete drive possibility offered in usual standard cell design.

1) Logic Optimization / Technology Mapping: the library free technology-mapping problem concerns the ability to use complex gates instead of using pre-characterized libraries. The main problem with “Virtual Libraries” is that the number of cells available can be very high and we can assume that the logic synthesis commercial tools are not especially well adapted to this kind of library.

In Table 1, we give an illustration of the number of different logic functions available in CMOS technology for a given limitation of N and P transistors in series.

<table>
<thead>
<tr>
<th>Number of serial PMOS transistors</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>7</td>
<td>18</td>
<td>42</td>
<td>90</td>
</tr>
<tr>
<td>3</td>
<td>18</td>
<td>87</td>
<td>396</td>
<td>1677</td>
</tr>
<tr>
<td>4</td>
<td>42</td>
<td>396</td>
<td>3503</td>
<td>28435</td>
</tr>
<tr>
<td>5</td>
<td>90</td>
<td>1677</td>
<td>425803</td>
<td>425803</td>
</tr>
</tbody>
</table>

Table 1. Number of logic functions available for a given limitation of serial transistors.
For instance, for a maximum of four serial transistors (for each plan, N and P) we may dispose of a library with 3503 different functionalities. Moreover, we have a continuous sizing for each logical function that results in an almost infinite number of elements, considering the continuous transistor sizing facility.

Several approaches to realize technology mapping onto Virtual Library have already been proposed [11], [12], either as industrial products or in academic tools. Once the technology mapping on the virtual library cells has been completed, each logical function is transformed into the corresponding transistor network that is associated to a virtual cell. The network creation consists of generating a BDD for each virtual cell used in the design. Then an optimization of this BDD allows the generation of a transistor netlist for the circuit.

2) Timing & Power Modeling, Transistor Sizing:

In this section, we will summarize the problem of timing analysis (already presented in one of our previous work [13]) using transistor sizing in association with the inherent problem concerning the transistors structure modeling. In [14], [15], [16] it has been shown that it is possible to develop a simple analytical model of the performance of CMOS gates with a good accuracy compared to electrical simulations. An efficient implementation of this model has been integrated. Concerning the problem of transistor sizing, [17] and [18] show that for most of the circuits, a local re-sizing of only a few selected transistors in the circuit can significantly reduce the power consumption.

C. Place and Route, Layout generation

The place and route and layout generation tools of the “transistor level layout synthesis” approach have been vastly presented in previous work [13]. In this section, we will briefly recapitulate the strategy of these tools.

1) Virtual cell Place and Route: placement and routing steps is performed from the “Virtual Cell” structural netlist representation. These operations use the predictive analytical models presented in the previous paragraph and is composed of three steps.

• First, a placement based on an iterative partitioning and global routing between each partition is performed [19]. Then cells are placed in each partition to allow rows creation. A local routing step is lastly done to generate virtual channels.

• Secondly, we create the symbolic view of each virtual cell (using the Euler trail solution [20]). Afterward the symbolic transistors rows are created then optimized (flipping, merging etc ...) and routed (“inner Row” maze routing).

• Finally, all the remaining connections are routed by a virtual channel router using detail routing algorithms (constraint graphs and multi-layer maze router).

2) Layout generation: the layout generation of each row requires as inputs the symbolic view of each row and the technology rules for the targeted process. From a constraint graph, we obtain a “compacted” layout inherent of the “linear-matrix” style. The main advantage offered by this procedure is the technology independence (rules are described in an user file).

IV. RESULTS AND VALIDATION

A. The implementation

As said previously, in order to converge most efficiently during the optimization phase, the architecture of the software prototype is based on a unique data-structure done in C++. This prototype integrates plug and play facilities to ease the exchange of the different “engines” under development

B. Validation strategy

Validations have been done in a 0.13µm CMOS technology. The comparison has been done with respect to the standard flow using an In-House library. We have run our prototype on some industrial and ISCAS85 circuits. We proceed to various comparisons on transistor number (logic synthesis efficiency), transistor density (area), timing and power performances (transistor width) to evaluate our tool.

C. Logic synthesis and associated area

The technology mapping step has been completed using Design Compiler (Synopsys). The number of transistors required in the final netlist is the benchmark metric to evaluate the impact of using a virtual library for the mapping. Moreover we obtain a first estimation of the final circuit area, given by the sum of the cells area.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Standard number</th>
<th>Area (mm²)</th>
<th>Transistor number</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C3540</td>
<td>3860</td>
<td>0.0081</td>
<td>2998</td>
<td>0.0060</td>
</tr>
<tr>
<td>C5315</td>
<td>4712</td>
<td>0.0095</td>
<td>4518</td>
<td>0.0092</td>
</tr>
<tr>
<td>C6288</td>
<td>9876</td>
<td>0.0151</td>
<td>7424</td>
<td>0.0150</td>
</tr>
<tr>
<td>C7552</td>
<td>7008</td>
<td>0.0116</td>
<td>5902</td>
<td>0.012</td>
</tr>
<tr>
<td>Uniphx</td>
<td>30168</td>
<td>0.0473</td>
<td>13952</td>
<td>0.026</td>
</tr>
<tr>
<td>Multi32</td>
<td>47586</td>
<td>0.0785</td>
<td>40354</td>
<td>0.086</td>
</tr>
</tbody>
</table>

Table 2. Logical synthesis and associated area

The results given in the Table 2 illustrate the decrease of the number of transistors required to realize the same circuit with our prototype, compared to a standard approach. Actually, the transistor number is decreased by an average of 27 %. Meanwhile the circuit area is not reduced in the same amount (i.e. equivalent area for smallest circuits). The reason is that automatically generated cells are not as small as standard cell.
D. Flow validation versus standard approach

To evaluate the whole flow of our approach versus the standard approach, we run a set of benchmarks on different circuits that should reach the same timing constraint for both approaches. The benchmark metric is the sum of the transistors width and the final area:

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Average</th>
<th>Area</th>
<th>Density</th>
<th>Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>transistors width (µm)</td>
<td>(mm²)</td>
<td>(tr/mm²)</td>
<td>(ps)</td>
</tr>
<tr>
<td>C3540</td>
<td>0.957</td>
<td>0.008</td>
<td>374750</td>
<td>1653</td>
</tr>
<tr>
<td>C5315</td>
<td>0.869</td>
<td>0.013</td>
<td>362462</td>
<td>1736</td>
</tr>
<tr>
<td>C6288</td>
<td>0.832</td>
<td>0.020</td>
<td>371200</td>
<td>5389</td>
</tr>
<tr>
<td>C7552</td>
<td>0.855</td>
<td>0.016</td>
<td>368880</td>
<td>3474</td>
</tr>
<tr>
<td>Uniphy</td>
<td>1.003</td>
<td>0.065</td>
<td>214650</td>
<td>1773</td>
</tr>
<tr>
<td>Mult32</td>
<td>0.851</td>
<td>0.104</td>
<td>388020</td>
<td>9312</td>
</tr>
</tbody>
</table>

Table 3. Standard flow results

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Average</th>
<th>Area</th>
<th>Density</th>
<th>Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>transistors width (µm)</td>
<td>(mm²)</td>
<td>(tr/mm²)</td>
<td>(ps)</td>
</tr>
<tr>
<td>C3540</td>
<td>0.357</td>
<td>0.0072</td>
<td>416390</td>
<td>1690</td>
</tr>
<tr>
<td>C5315</td>
<td>0.308</td>
<td>0.013</td>
<td>347540</td>
<td>1650</td>
</tr>
<tr>
<td>C6288</td>
<td>0.459</td>
<td>0.018</td>
<td>412450</td>
<td>4870</td>
</tr>
<tr>
<td>C7552</td>
<td>0.347</td>
<td>0.016</td>
<td>368880</td>
<td>2030</td>
</tr>
<tr>
<td>Uniphy</td>
<td>0.486</td>
<td>0.031</td>
<td>450060</td>
<td>1850</td>
</tr>
<tr>
<td>Mult32</td>
<td>0.368</td>
<td>0.119</td>
<td>339110</td>
<td>12930</td>
</tr>
</tbody>
</table>

Table 4. 1P+ flow results

As shown in the two tables above, the areas obtained with both methods are similar except for the Mult32 circuit. This degradation is due to the complexity of the place and route step which increases the interconnect length and so impacts the results in area and timing (developed place and route tools are not yet as efficient as commercial ones). The Fig. 4 represents an area and an average transistor width comparison for circuits satisfying almost the same timing constraint:

Average transistor width comparison shows a significant advantage for the presented approach compared to the standard cell implementation (average reduction around 50% improvement). This result shows clearly that the possibility to resize smartly only needed transistor (specific and continuous transistor resizing) allows to significantly reduce the global width of the transistors. As a direct effect, we can expect to obtain a substantial power dissipation reduction compared to standard cell approaches (validation concerning power reduction is currently in progress using commercial power estimation tools).

Additionally, by reducing the number of transistors required to realize the same circuit (section IV-C), we can expect significant power reduction. Indeed, with new UDSM technologies, leakage current becomes of significant importance even if the transistor is not toggling.

E. Run time analysis

These results concerning area, timing and power are quite encouraging mostly if we consider the facility obtained in generating and migrating macro-blocks in very short time intervals as shown in Table 5:

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Transistors count</th>
<th>Run time (mn)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C3540</td>
<td>2998</td>
<td>3</td>
</tr>
<tr>
<td>C5315</td>
<td>4518</td>
<td>5</td>
</tr>
<tr>
<td>C6288</td>
<td>7424</td>
<td>8</td>
</tr>
<tr>
<td>C7552</td>
<td>5902</td>
<td>6</td>
</tr>
<tr>
<td>Uniphy</td>
<td>13952</td>
<td>15</td>
</tr>
<tr>
<td>Mult32</td>
<td>40354</td>
<td>65</td>
</tr>
</tbody>
</table>

Table 5. 1P+ tools: run time

These results, obtained on UltraSparc II 480Mhz machine, strengthen one of the main advantages offered by this approach: the possibility to quickly prototype IP block. Moreover, we remove the time associated to the development of a library and this enables fast technology migration every time a new technology is available.

F. Layout example and migration facilities

On the example given in Fig.5, a benchmark circuit done in a 0.13µm CMOS technology synthesized with our transistor-level layout generator is presented:

Fig 4. Area and average transistor width comparison.

Fig 5. Layout of the c3540 (2998 transistors) circuit
We have validated the migration possibilities of our methodology by evaluating the performance of benchmark circuits in new process available. Using 1\textsuperscript{st}P\textsuperscript{2}, it only requires few time to migrate to a new process.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Density (tr/mm\textsuperscript{2}) 0.18 um</th>
<th>Density (tr/mm\textsuperscript{2}) 0.13 um</th>
<th>Density (tr/mm\textsuperscript{2}) 90 nm</th>
<th>Time needed (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C3540</td>
<td>199870</td>
<td>416390</td>
<td>832780</td>
<td>3</td>
</tr>
<tr>
<td>C5315</td>
<td>173770</td>
<td>347540</td>
<td>728950</td>
<td>5</td>
</tr>
<tr>
<td>C6288</td>
<td>206220</td>
<td>412450</td>
<td>857170</td>
<td>8</td>
</tr>
<tr>
<td>C7552</td>
<td>190390</td>
<td>368880</td>
<td>725690</td>
<td>6</td>
</tr>
<tr>
<td>Uniphy</td>
<td>211393</td>
<td>450060</td>
<td>872000</td>
<td>15</td>
</tr>
<tr>
<td>Multi32</td>
<td>184270</td>
<td>339110</td>
<td>733710</td>
<td>65</td>
</tr>
</tbody>
</table>

Table 6. 1\textsuperscript{st}P\textsuperscript{2} migration from 0.18\mu m to 90nm

Apart from the time necessary to update the technology file (half a day), the circuits have been migrated from one process to another in a very short time as shown in the Table 6.

G. Improvement and future work

We pointed out previously that the physical layout generation can strongly impact the final circuit. In fact the results of the comparison between the area of individual virtual cells compared with the standard cells (for the same functionality and the same technology) show almost equivalent results for combinatorial cell but prove a significant difference for sequential element. The high complexity of the intra cell interconnections of the flip-flop and our choice of topology (initially chosen to generate combinatorial cell) can explain this difference that can be overcome by revisiting some of the algorithms of the physical generation.

Moreover, the first validations of our place and route tool versus Magma’s highlight some light degradation on complex circuits. Some place and route algorithms should be improved so as to reach the same area as we could get using industrial tools.

V. CONCLUSION

In this paper, we have presented an original alternative to the classical standard cell based layout synthesis. By using a “virtual cell library”, we obtain a physical generation at the transistor level, integrating the different steps of physical layout generation, performance estimation and optimization. This may give great facilities in quickly evaluating and prototyping different flavors of IP blocks by using the latest available technology and moreover it removes the time and the prohibitive costs associated to the development of a standard library. We show that our tool which can be seen as an “IP Prototyper” is able to handle simple blocks (order of complexity ~10K to 100k transistors).

REFERENCES