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# CMOS Image sensor dedicated to speed determination of fast moving luminous objects

Benaissa Bellach<sup>a</sup>, Bernard Lamalle<sup>a</sup>, Lew F.C. Lew Yan Voon<sup>a</sup> and Guy Cathebras<sup>b</sup>

<sup>a</sup>LE2I - Université de Bourgogne - 12 rue de la fonderie - 71200 Le Creusot - France

<sup>b</sup> LIRMM 161 - rue Ada 34392 - Montpellier Cedex 5 - France

## ABSTRACT

We present a CMOS image sensor for speed determination of fast moving luminous objects. Our circuit furnishes a 16-gray level image that contains both spatial and temporal information on the fast moving object under observation. The spatial information is given by the coordinates of the illuminated pixels and the temporal information is coded in the gray level of the pixels. By applying simple image processing algorithms to the image, the trajectory, direction of motion and speed of the moving object can be determined. The circuit is designed and fabricated in standard CMOS 0.6  $\mu m$  process from Austria MicroSystems (AMS). The core of the circuit is an array of  $64 \times 64$  pixels based on an original Digital Pixel Sensor (DPS) architecture. Each pixel is composed of a photodiode as the light sensing element, a comparator, a pulse generator and a 4-bit static memory for storing the gray value of the pixel. The working principle of the circuit, its design and some quantitative experimental results are presented in the paper.

**Keywords:** CMOS image sensor, image processing, speed measurement

## 1. INTRODUCTION

Most of the CMOS image sensor developments have been, up to now, directed towards relatively slow speed image capture. But today, there is an increasing interest in the use of such sensors for high speed, high resolution applications that were until recently the exclusive domains of CCD imagers. Besides, contrary to older CMOS sensor architectures such as the passive pixel sensor (PPS) and the active pixel sensor (APS)<sup>1</sup> which have analog readouts, the more recently developed digital pixel sensor (DPS)<sup>2</sup> employs a per-pixel analog-to-digital converter (ADC) in order to produce digital data at the output of the image sensor array. In this paper, we describe a  $64 \times 64$  DPS structure based image sensor with a per-pixel electronic decision unit and digital memory. Our circuit is dedicated to the observation and analysis of fast varying luminous phenomena with time constant smaller than  $1\mu s$ . The innovation in our image sensor resides in the fact that only one image of the moving object needs to be taken and analyzed in order to determine its speed. Moreover, there is a direct relationship between the gray levels of the image and the speed of the moving object. Image acquisition using our sensor is achieved by simultaneously exposing all the pixels under the control of an external clock whose frequency determines the exposure time. The image data are first stored in the memory devices integrated at the pixel level and then readout on the 4 digital outputs yielding a 16-gray level image on which processing is done in order to determine the speed of the observed moving object. The rest of the paper is organized as follows. Section 2 introduces the working principle of the image sensor. Section 3 presents our DPS based sensor architecture and gives its main characteristics. The different modes of operation are described in section 4. Finally, the experimental tests carried out on the sensor and the results obtained are presented and discussed in section 5.

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Further author information:(Send correspondence to B. Bellach)

B. Bellach: E-mail: b.bellach@iutlecreusot.u-bourgogne.fr

## 2. WORKING PRINCIPLE

In order to be able to determine the average speed of a moving object between any two positions, we need to know the distance separating these two positions and the time taken to cover this distance. The average speed is then given by:

$$average\ speed = \frac{distance}{time}$$

To obtain the distance and time information, we have designed an image sensor that operates according to the following principle. We assume that the moving object is highly luminous with respect to the background. At the start of the acquisition of an image of the highly luminous moving object, a main 4-bit counter is initialized and clocked at a frequency ( $f$ ) while all the pixels of the sensor are simultaneously exposed. Each time a pixel detects the moving object for the first time, the value of the main counter is stored in a 4-bit static memory integrated at the pixel level. The acquisition is over when the counter has made a complete turn, that is after 16 clock cycles, and the memories of all the pixels that have not been exposed to the moving object will have as value the maximum value of the counter. The values stored in the pixel memories are next read out and displayed as a 16-gray level image. An example of the image read out at the output of our sensor is represented in Fig. 1.



**Figure 1.** Example of the image produced by our sensor

The image contains both spatial and temporal information that allows us to determine the trajectory, direction of motion and speed of the moving object. The trajectory of the object can be clearly seen on the image. The gray level of the object pixels corresponds to the time at which the object is detected by the pixels, scaled by a factor that depends on the frequency of the clock. The brighter is the pixel the shorter is the time. As a consequence, the direction of motion is given by the variation of the gray levels of the object pixels from the brighter pixels to the darker ones. Concerning the average speed of the object, it can be computed by considering any two pixels of different gray levels according to the following equation (the center of gravity is considered if the object is more than one pixel in width):

$$average\ speed = \frac{K \times d \times pixel\ size}{T \times (G2 - G1)}$$

Where  $d$  is the distance in terms of the number of pixels.  $G2$  and  $G1$  are the gray levels of the pixels considered.  $K$  and  $T$  are the scaling factors that allows the conversion of respectively the pixel distance and the gray levels into real world distance and time.

$K$  is a function of the focal length of the lens and the sensor to scene distance and it can be experimentally determined. If the position of the sensor with respect to the observed scene is such that for a sensor size of  $L \times L \mu m$  the view area is  $l \times l cm$  then  $K$  is given by:

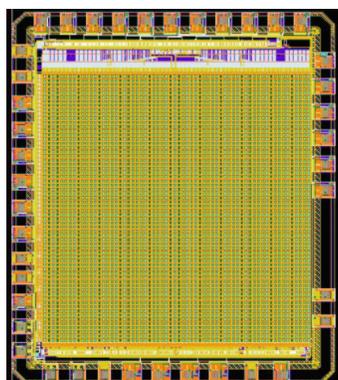
$$K = \frac{L \times 10^{-2}}{l \times 10^{-6}}$$

T depends on the frequency of the clock. It corresponds in fact to the period and it is thus given by:

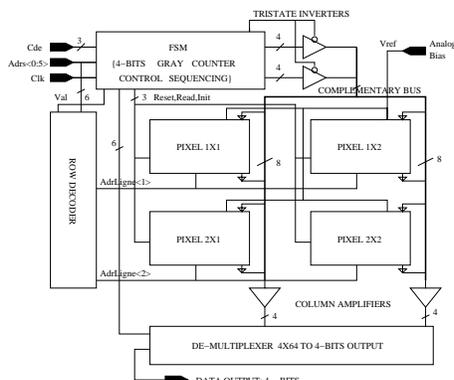
$$T = \frac{1}{f}$$

### 3. CIRCUIT DESIGN

A photomicrograph of the sensor circuit is shown in fig. 2(a) and its main characteristics are listed in table 1. The chip contains around 400 thousand transistors for a circuit size of  $3.7 \times 4.3 \mu\text{m}$  excluding the pads.



(a) Photomicrograph of the  $3.7 \times 4.3 \text{ mm}$  chip



(b) Block Diagram of a  $2 \times 2$  matrix

**Figure 2.** a: Photomicrograph of the  $3.7 \times 4.3 \text{ mm}$  chip b: Block diagram of a  $2 \times 2$  matrix

**Table 1.** Chip characteristics

Technology	0.6 $\mu\text{m}$ 3-metal CMOS process from AMS
Die size	$3.7 \times 4.3 \text{ mm}$
Array size	$64 \times 64$ pixels
Number of transistors	around 400 thousand
pixel size	$49.2 \times 49.2 \mu\text{m}$
Photo-detector type	nMOS photodiode
number of transistors/pixel	55
sensor fill factor	18%

Fig.2(b) shows the main functional blocks of the chip. The core of the chip is the sensor array composed of  $64 \times 64$  pixels. On the periphery of the sensor array are the main 4-bit counter (a Gray code counter), a control sequencing block, a row decoder, a demultiplexer, column amplifiers and tristate inverters that manage the memory access. A row decoder and a demultiplexer are used to transfer signals from the pixel's memory to four digital outputs, through the column amplifiers.

#### 3.1. Pixel design

The pixel schematic and layout are shown in fig.3(a) and fig.3(b). It is implemented with 55 transistors and includes a photodiode, a comparator, a pulse generator and a 4-bit static memory. The fill factor is about 18% for a pixel size of  $49.2 \times 49.2 \mu\text{m}$ .

The photo-detector circuit is implemented as a diffusion-N well photodiode with a reset, an anti-blooming and a Read transistor. Its architecture is based on charge integration for transducing the photocurrent into a voltage. We have chosen this operation mode because it achieves better gain conversion than other modes.<sup>3</sup>

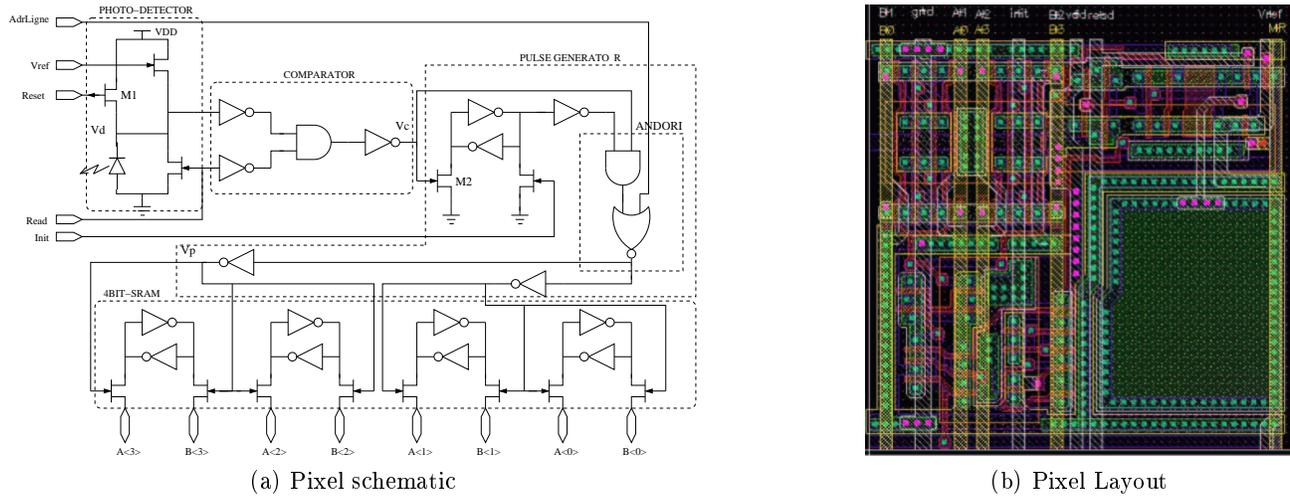


Figure 3. a: Pixel schematic b: Pixel layout

Before an image is acquired, a pulse is applied to the Init input and the read input is set to logic value 0. Then, transistor M1 is first turned ON in order to connect node Vd to the power supply and charge the capacitance at this node. This capacitance is mainly constituted by the parasitic capacitance of the photodiode that depends mostly on its size (eg. perimeter and area) and given by the following expression:

$$C = K_p \cdot 4a + K_s \cdot a^2$$

where a is one side of the photodiode,  $a^2$  the area and  $K_p$  and  $K_s$  the process parameters. For the AMS 0.6  $\mu m$  CMOS process, the process parameter values are  $K_p = 430 \cdot 10^{-12} F/m$  and  $K_s = 380 \cdot 10^{-6} F/m^2$ .

Since for our photodiode  $a = 529 pm$ , the estimated capacitance is  $C = 0.24 pF$ .

Next, the transistor M1 is turned OFF and the charged parasitic capacitor of the photodiode discharges with a constant current which depends on the intensity of the luminous flux falling on the photodiode as shown in fig.4. The higher the luminous flux, the higher is the current and thus the shorter is the discharge time.

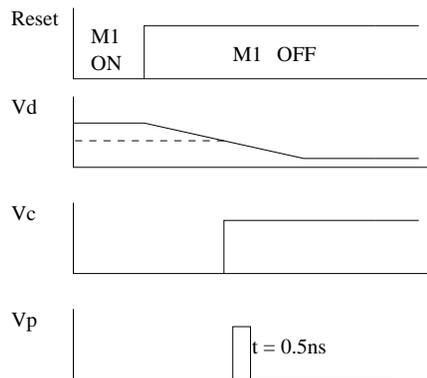


Figure 4. Pixel timing diagram

The voltage at node Vd thus decreases at a constant rate and when it reaches the threshold value the output of the comparator switches from a low logic value to a high logic value and a short memory write pulse is generated by the pulse generator (See Vc, Vd and Vp voltages in fig.4).

The analog bias voltage Vref is used to limit the blooming phenomenon. This phenomenon occurs when the intensity of the luminous flux is too high resulting in a too rapid decrease of the voltage at the node Vd which can even become negative. When this happens, the good functioning of the neighboring pixels is disturbed. The Vref voltage thus allows us to set a limit for the minimum value of the voltage at node Vd.

The comparator consists of CMOS inverters and NAND gates that are tailored to suit minimal power consumption and comparator noise margin requirements. In read or write mode, the comparator as well as the photo-detector must be disabled. This is achieved by setting the Read input to a high logic level. In this case the node Vd is connected to gnd and the comparator output remains at the low logic value.

The pulse generator block uses a SRAM memory structure to create a short width pulse. The comparator output signal Vc is connected to the ANDORI structure through two different paths: a direct path and through the SRAM memory as shown in fig.3(a). The difference in the transit time between the two signal paths is detected by the ANDORI which produces a pulse whose width is fixed by the delay time and depends essentially on the dimensions of the access transistor M2 through its  $C_{gs}$  Capacitance. Setting  $L = 1 \mu m$ ,  $W = 1.4 \mu m$  and the others transistors to minimum size, the pulse delay is around  $0.5 ns$ , which is sufficient for writing data into the 4-bit SRAM memory.

The 4-bit SRAM memory integrated into the pixel is used to store the current state of the common Gray code counter during the acquisition mode before it is read out during the read mode using two buses: a primary data bus and a complementary one in order to avoid deterioration to the signals. Readout is done row by row under the control of the AdrLigne signal.

### 3.2. Control block and Gray code counter

The control sequencing block and Gray code counter work like a synchronous Finite State Machine (FSM) that provides in a synchronous way all the control signals of the DPS chip depending on the chosen operation mode determined by the value of digital signal applied to the Cde inputs fig.2(b). Users can select three different operation modes: The first and main mode is the *acquisition mode*. In this mode the FSM generates the synchronous count that is applied to the complimentary buses A and B. The acquisition is directly synchronized by the external clock which sets the exposure time. The second mode called the *read mode* consists in reading all the digital values memorized in the pixels using the 64 column amplifiers and the 256 to 4-Bit demultiplexer. The third and last mode is the *write mode* which is used to initialize the array of pixels by writing a numeric value in the pixel memories. In order to reduce interconnection, we have chosen to carry out this operation row by row. For each of these operation modes, the FSM furnishes the correct control signals and Gray code counter value.

### 3.3. Memory access

Fig.5(a) shows how the memory device is interconnected to the column amplifiers and the control sequencing block.

The pixel's memory can be accessed by two signals (Vpulse and AdrLigne). The Vpulse signal is generated by the pulse generator block of the pixel and it is used to store the value present on the column bus during the acquisition mode. The AdrLigne signal is generated by the row decoder and it is used, in read mode, to make the value stored in the pixel's memory available to the column amplifiers.

The complementary buses A and B are controlled by the tristate inverters which are respectively driven by Ap, An, Bp, and Bn signals. These signals are controlled by the FSM that applies appropriate logic values to set the complementary bus <A> and <B> in one of these three possible operation modes fig.5(a) :

- The precharge mode by setting simultaneously A and B lines to VDD.
- The write operation mode by setting the lines A to VDD and B to GND (or inversely depending on the logic value to write).

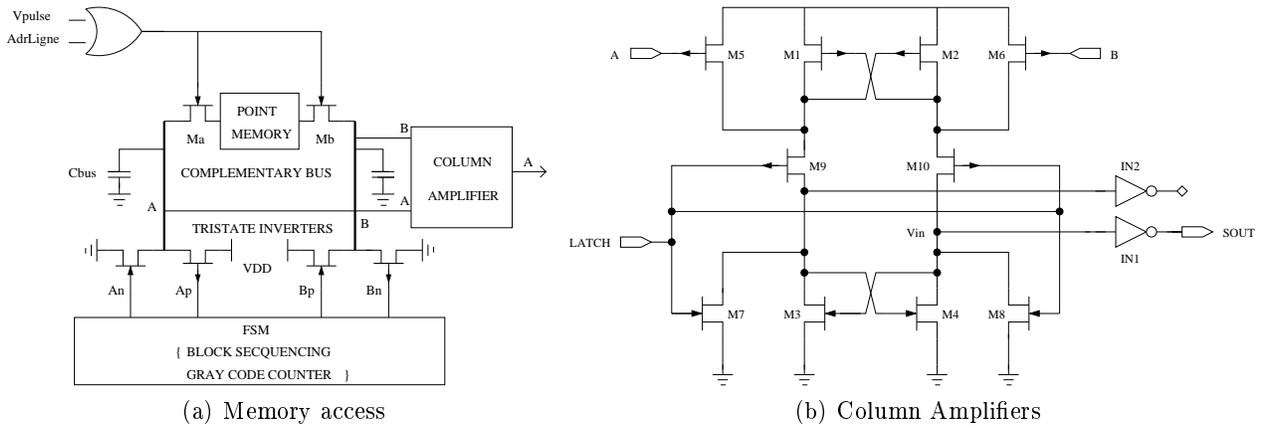


Figure 5. a: Diagram Memory Access b: Column Amplifiers

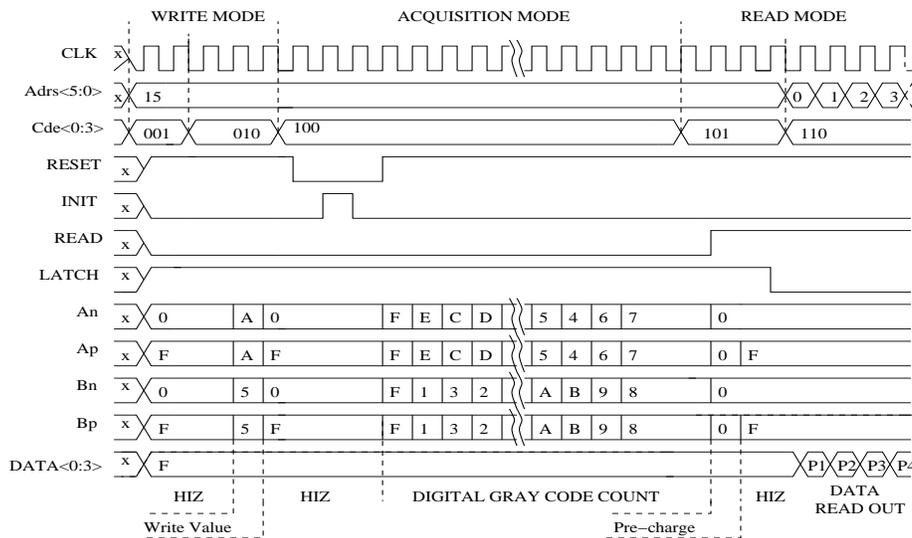


Figure 6. DPS timing diagram

- The HIZ mode in which the complementary buses A and B are simultaneously disconnected (all transistors are turned OFF).

In the read mode,  $M_A$  and  $M_B$  transistors are turned ON. In order to prevent the deterioration of the memorized logic value by the parasitic capacitance  $C_{bus}$  of the bus, we use a classical high speed amplifier that is sensitive to small voltage difference. This capacitance is composed of the capacitance of the bus and that of all the memory access transistors  $C_{gs}$  of  $M_A$  and  $M_B$  on each line.

#### 4. SENSOR OPERATION

In this section, we describe the three main phases in the capture of a single frame. These phases are: *a write or initialization phase, an acquisition phase and a read phase.*

##### Write phase

Before an acquisition is done, all the pixel memories must be initialized with a default value. In this way, all the pixels that have not received enough luminous flux in order to latch the current value of the grey code

counter during the acquisition phase would have as value the default value. To write the default value in the pixel memories, we have to, first, write it in an internal register of the FSM, then make it available on the complementary bus before it is stored in the pixel memories under the control of the (RR/W) signal. At each step, the correct operation code must be applied to the Cde inputs.

### Acquisition phase

Before the acquisition of an image really starts, three rising clock edges are necessary so as to set the correct value for the reset, init and Read/Write Enable signals. These signals are used to initialize the photo-detectors, and to activate the pulse generator. At the fourth rising edge of the clock, the integration phase and the common 4-bit Gray code counter are simultaneously started. Acquisition is over when the counter has made one turn that is after 16 clock edges. The 4-bit grey coded values ( $N_P$ ) stored in the pixel memories during the acquisition represent the time the moving object passes in front of the pixels. These time durations depends on the frequency of the clock and can be calculated according to the following equation:

$$T_s = \frac{1}{f} \times N_P(s) \quad (1)$$

### Read phase

During this phase, data stored in the pixel memories are read out at the outputs of the chip. Column amplifiers are necessary to perform the readout operation because of the high parasitic capacitance value of the column buses. The random initial state of the column buses will deteriorate the memorized value when the memory access transistors pass from OFF to ON state. To prevent this, the read cycle is executed as follows: firstly, when the access transistors are OFF, the parasitic capacitance  $C_{bus}$  is charged to Vdd volts, next the complementary bus is set to the high impedance state (HIZ). Finally, the access transistors are turned ON, resulting in a potential difference between the two columns that is a function of the value stored in the pixel memories. The column amplifiers detect this potential difference and furnished a logic value that is latched and then readout through the  $256 \times 4$  demultiplexer.

## 5. TEST

The DPS chip has been tested and shown to be fully functional. In the following subsections, we briefly describe the test that we have carried out on both stationary and moving objects, and on highly luminous phenomenon and present the results obtained.

### Stationary object

The first test that we have realized consists in the acquisition of the image of a stationary object in 16 grey levels fig.7(a). This test has permitted us to verify that the sensor is fully functional. In this case, our sensor operates like a classical image sensor and the grey level of the pixel depends only on the quantity of luminous flux received.

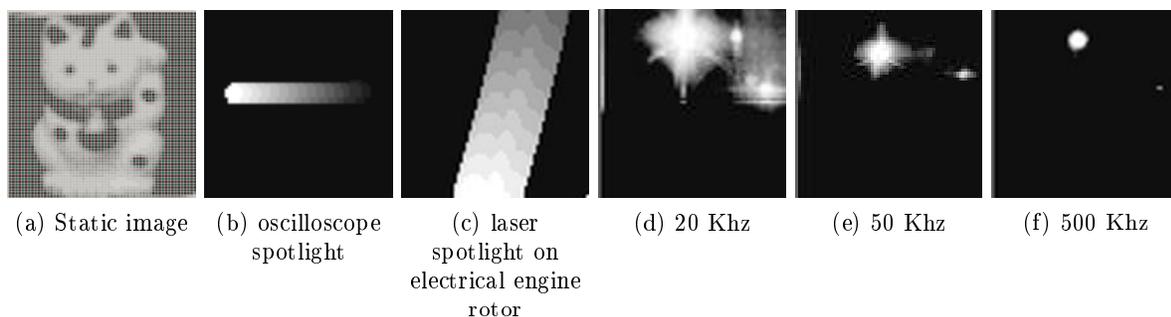
### Moving objects

We have considered in the first place the displacement of the spot on an oscilloscope screen. The time base was set to  $2ms/cm$  which corresponds to a displacement speed of the spot of  $5m/s$ . An image of the spot was taken with a clock frequency of  $800Hz$  which means that the time difference between two consecutive grey levels is  $1/800s$ . Furthermore, knowing that the sensor was placed at a distance of 50 cm from the oscilloscope screen with a lens of focal length ( $25mm$ ) and that the size of the pixel is  $49,2\mu m \times 49,2\mu m$ , we can deduce the true distance travelled by the spot and thus calculate the speed of the spot. We obtain a speed of  $4.94 m/s$  which is in good agreement with the setting of the time base.

Next, we have considered a laser spotlight fixed on an electrical motor. The angular speed of the electrical motor was previously determined using a tachometer, this speed is  $1473rpm$ . The diameter of the circle formed by the revolving laser spotlight is  $9.4cm$  that gives a speed of  $7.24m/s$ . The image obtained with a clock frequency of  $20KHz$  as shown in fig.7(c) has allowed us to calculate the speed of the spotlight, we have found a speed of  $7.19m/s$ . Again the result obtained is quite satisfactory.

### Highly luminous stationary phenomenon

During laser soldering, the interaction of the laser beam with the processed material provokes a high release of luminous energy. Local variations of this luminous scene can provide useful information about the associated physical phenomena. A fast video camera that can provide up to 32,000 frames/secondes is used to observe the interaction, however the sampling rate is not high enough to observe all phenomena. In this application, the phenomenon under study is very luminous and the thermal gradient is in fast evolution, for all these reasons our device is well suited for the study of such phenomenon. We have used our sensor to study the power distribution in the spotlight in a static application, the result of different acquisitions is shown in ( fig.7(d), 7(e), 7(f)) the grey level distribution gives directly the information about the power distribution. The advantage of our sensor over the fast video camera is that we can achieve an image of the soldering zone with a very short acquisition time.



**Figure 7.** a: static 16-gray image b: spotlight speed 10m/s c: speed of laser spotlight 7.19m/s d,e,f: Laser soldering images at three different acquisition rates

## 6. CONCLUSION

We have described a Digital Pixel Sensor (DPS) based chip implemented in a standard digital CMOS 0.6  $\mu m$  process. The core of the 400 thousand transistor chip is an array of  $64 \times 64$  DPS pixels. Each pixel is composed of a photodiode circuit, a comparator, a pulse generator and a 4-bit SRAM. It contains 55 transistors for a pixel size of  $49.2 \times 49.2 \mu m$ . The acquisition rate of our sensor has been tested up to 1 MHz with pixel reset and A/D conversion performed in parallel for all pixels. The experimental results show that the DPS structure can capture moving luminous object and furnishes an image that contains both temporal and spatial information. From this unique image the speed of the moving object can be calculated with a good accuracy.

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