On the Detection of SSN-Induced Logic Errors Through On-Chip Monitoring

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Abstract

Simultaneous switching noise (SSN) is an important issue for the design and test and actual ICs. In particular, SSN that originates from the internal logic circuitry becomes a serious problem as the speed and density of the internal circuit increase. In this paper, an on-chip monitor is proposed to detect potential logic errors in digital circuits due to the presence of SSN. This monitor checks the variations of power/ground lines at the interface between non-coherent logic blocks in order to warn that a logic error is likely to occur. This information can then be used for any scheme that takes corrective actions.

1. Introduction

For years, noise has been an important issue in the design of VLSI systems. In particular, signal and power integrity are becoming crucial problems as circuits operate at higher frequency with short rise/fall times and lower supply voltage. Power and ground bounce in the power and ground distribution network is one of the main contributors to the overall circuit noise. Power and ground bounce, also called Simultaneous Switching Noise (SSN), usually designates some kind of fluctuations in the power and ground voltages due to current flowing through the parasitic inductances and capacitances of the power and ground network, bonding pads and package pins.

Since ground bounce is becoming an important limitation in modern circuits, many researchers have focused on the problem of modeling the SSN, proposing design technique to reduce the SSN, or defining test technique to detect excessive SSN.

Through electrical simulations, earlier works are dedicated to the analysis and modeling of SSN [1,2,3,4,5,6]. The possibility of reducing the level of noise by different design techniques such as decoupling capacitances is studied in some papers [3,7,8]. A few papers propose to model the substrate noise and the impact on analog circuitry [9,10]. Finally, several papers are more dedicated to test problems [11,12,13,14,15]. In these works, authors try to analyze the impact of ground bounce on the logic and timing behavior of digital circuit in order to generate test vectors to detect a possible error. Another aspect is to propose integrated sensor to monitor the power/ground lines to detect excessive noise [16]

In this paper, we focus on the logic behavior of internal digital circuitry. On-chip monitoring of SSN appears as an interesting possibility to obtain information about the presence of excessive SSN. So the main contribution of this paper is the proposal of a monitor for SSN that checks the variations of power/ground lines at the interface between non-coherent logic blocks in order to warn that a logic error is susceptible to occur.

The paper is organized as follows. The analysis of the impact of SSN on the logic behavior of digital circuits is presented in section 2. From this analysis, the desirable characteristics for an on-chip monitor to detect SSN-induced logic errors are derived in section 3 and the on-chip monitor circuit is described. Simulation results are then presented in section 4 to validate the operating mode of the proposed on-chip monitor circuit and to illustrate its ability to alert on potential logic errors at the interface between non-coherent digital blocks. Finally section 5 concludes the paper.

2. Impact of SSN on the logic behavior of digital circuits

In presence of SSN, the current flowing through the parasitic inductances and capacitances of the power and ground lines generates fluctuations of the power and ground voltages. A straightforward consequence of these fluctuations is fluctuations on every node of the circuit including the internal logic nodes but also the input and output nodes. To illustrate this, A Spice simulation of the C432 benchmark circuit has been realized using a 130nm technology with 1.2 Volt of power voltage.

Fig.1 gives the equivalent simulated model where the double cell corresponds to the parasitic components for a typical package pin. These parasitic components model the connection between the external pin and the internal pad trough the lead frame and the bonding wire. In our simulations we use the parasitic values of a typical CPGA package with R=28m□, C=0.1pF, L=7nH for the first parasitic cell and with R=165m□, C=0.5pF, L=4.1nH for the second parasitic cell. One double cell is used in the power connection and another one in the ground connection. Note that design techniques to reduce SSN are not implemented in our simulations because we want to observe and analyze the SSN phenomena and its impact on the circuit behavior.

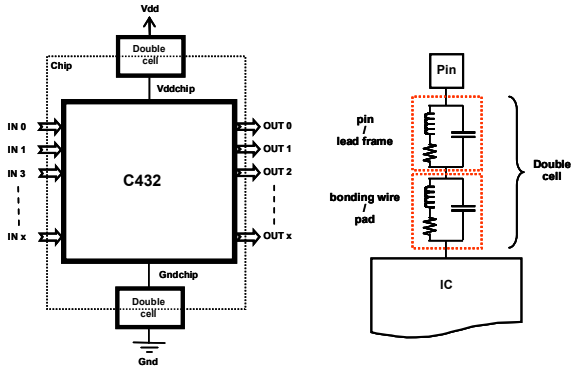


Figure 1: Simulation model of the C432

Figure 2 gives the typical waveforms observed at the output of the logic circuitry together with the power supply voltage variations in presence of SSN. It can be seen that it is merely possible to extract the logic information contained in the output signal at first view: the output voltage presents many oscillations with peak values around 2V and -0.8V, but no clear indication of logic "1" or logic "0". Regarding internal power supply voltages, they present large variations with a maximum value around 0.75V for the GNDchip line and a minimum value around 0.45V for the VDDchip line. This corresponds to extremely large variations, leading to voltage on the GNDchip (resp. VDDchip) line above (resp. below) the typical threshold of logic gates (around 0.6V for 1.2V supply voltage).

Hence, one could suspect that the circuit is affected by a logic dysfunction. Indeed concerning the possibility of having logic errors, the main criterion used in the literature is the modification of the power voltage or ground voltage. A logic error may appear if the power (resp. ground) voltage is lower (resp. higher) than a given limit, classically the logic gate threshold voltage.

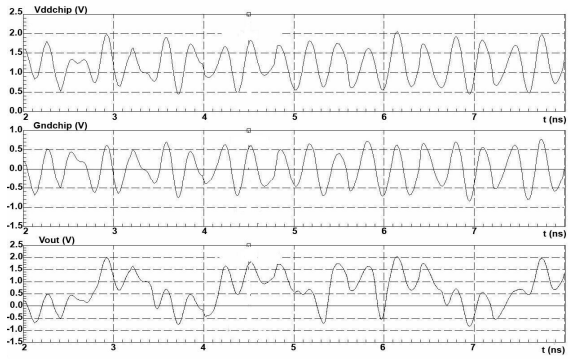
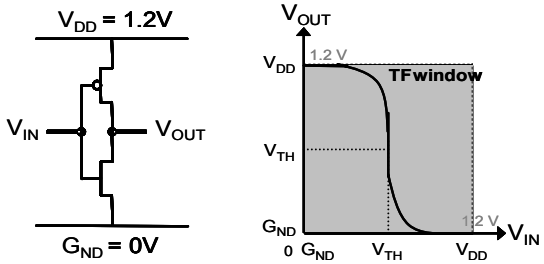
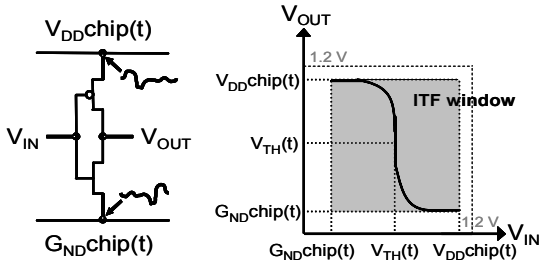


Figure 2: Simulated SSN for the C432

Despite this extremely noisy behavior, it is possible to analyze the logic behavior of the circuit using the concept of "instantaneous transfer function" as introduced in [17]. Indeed in presence of voltage fluctuations in the power/ground lines, the classical Transfer Function (TF) with constant values is no longer valid. Instead, the Instantaneous Transfer Function (ITF) should be considered to take into account voltage fluctuations over the time. As an illustration, figure 3 represents the TF and ITF for a simple inverter. Note that the global shape of the transfer function is not modified; the inverter transfer function is just working in a modified voltage window.



a) Nominal Transfer Function



b) Instantaneous Transfer Function

Figure 3: Inverter transfer function

From the ITF of figure 3.b, we can write:

- $V_{IN}(t)<V_{TH}(t)$ => $V_{IN}(t)$ is recognized as a logic "0" and $V_{OUT}(t)=V_{DD}chip(t)$
- $V_{IN}(t)>V_{TH}(t)$ => $V_{IN}(t)$ is recognized as a logic "1" and $V_{OUT}(t)=G_{ND}chip(t)$

where we define $V_{TH}(t)$ as the instantaneous logic threshold. Its value is around half of the instantaneous swing (Sw):

$$V_{TH}(t) \approx Sw(t)/2$$

with $Sw(t)=V_{DD}chip(t)-G_{ND}chip(t)$.

We observe that there is no fundamental difference between a "normal" TF in fig.3.a and an ITF in fig.3.b. Basically, a "low" input voltage gives a "high" input voltage and vice-versa.

Now let us re-consider the C432 benchmark circuit simulation given in figure 2. Remember that in figure 2, the output signal was very chaotic and impossible to interpret. Using the concept of ITF, we can deduce the logic interpretation of the output signal by comparing it with the instantaneous logic threshold $V_{TH}(t)$ evaluated as a function of $V_{DD}chip(t)$ and $G_{ND}chip(t)$. A "clean 1" (resp. "clean 0") is produced if the output is higher (resp. smaller) than $V_{TH}(t)$. Figure 4 gives the result of the simulation with the noisy output signal and the "cleaned" digital one.

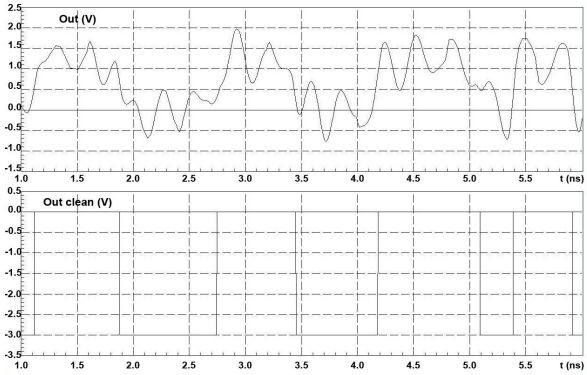


Figure 4: Logic behavior of the C432

In any case, whatever the input vectors used in the simulation, the "cleaned" signal perfectly corresponds to the fault-free response of the circuit. This means that we see this signal as a chaotic and incorrect because it is fluctuating while, in reality, the signal is still carrying the correct logic value! The circuit perfectly works from a logical point of view.

In fact, this demonstrates that the absolute value of the peak of noise is not relevant. The logic interpretation of a signal depends on the value of the logic threshold voltage $V_{TH}(t)$, which in turn, depends on the power voltage $V_{DD}chip(t)$ and the ground voltage $G_{ND}chip(t)$. So considering a logic gate, the absolute value of the input voltage does not matter, the input voltage can be quite high but still interpreted has a low input (logic "0") if its value is lower than $V_{TH}(t)$. Actually, the input voltage has to be in the range from $G_{ND}chip$ to $V_{DD}chip$ for a correct interpretation by the logic gate. In other words, the range of the input signal has to be coherent with the power and ground voltages.

3. SSN on-chip monitor

3.1. On-chip monitor specification

The previous section has allowed us to establish a necessary condition for the correct behavior of a logic gate in presence of SSN, i.e. the input signal must be in the same range the power and ground voltages. A sort of coherence has to be respected. This necessary condition can be further analyzed to establish the desirable characteristics for an on-chip monitor to detect logic errors induced by SSN.

A digital circuit is made of interconnected gates, and so the input signal of a given gate is the output signal of its driving gate. Considering the driving gate, when its output is high (resp. low), the p-transistor (resp. n-) network of the driving gate is ON connecting the power (resp. ground) line to its output. The output signal of the driving gate is therefore just an image of the power (ground) voltage. In case of power and ground lines with SSN, the output signal of the driving gate is then an image of the fluctuating $V_{DD}chip(t)$ or fluctuating $G_{ND}chip(t)$.

Two different situations must be considered at this point:

- SSN within a coherent digital block,
- SSN between non-coherent digital blocks.

A coherent digital block is a set of logic gates connected to the same $V_{DD}chip$ and $G_{ND}chip$ lines as illustrated in figure 5.a. In figure 5.b, the 2 non-coherent blocks have different $V_{DD}chip$ and $G_{ND}chip$ lines. Note that non-coherent blocks may or may not have the same "external" V_{DD} and G_{ND}.

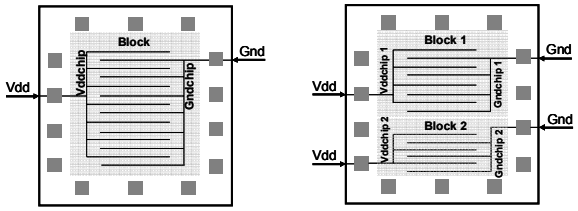


Figure 5: Coherence definition

In case of a coherent digital block, the driving and driven gates have the same $V_{DD}chip$ and $G_{ND}chip$ lines. A driven gate is therefore biased by $V_{DD}chip(t)$ and $G_{ND}chip(t)$, and the range of the output signal of the driving gate is from $G_{ND}chip(t)$ and $V_{DD}chip(t)$. According to the ITF defined in section 3, the driven gate works correctly and perfectly interprets its input signal level. This is true at any time and for any gate in the coherent block. In other words, for a standard CMOS gate operating into a coherent digital block, the input signal range is always coherent with the power and ground voltage whatever the amount of SSN. This

property demonstrates that a coherent digital block exhibits some kind of robustness and performs its correct logic function whatever the amount of SSN. There is therefore no need of implementing an on-chip monitor to detect logic errors within a coherent block.

In contrast, the situation may be very different and much more complicated in a circuit with non-coherent digital blocks. Of course, each block separately could perfectly works as previously mentioned, but problems may arise at the interface between blocks. Indeed, the power and ground lines of the blocks are different and so, in presence of SSN, they vary independently of each other. Let us consider for example the output of one block connected to the input of another block. This output signal is automatically coherent with the power and ground voltages of the first block, but it may happen that this signal is not coherent with the power and ground voltage of the second block. In this case, the signal will be logically misinterpreted by the driven gate of the second block. So clearly, the interface between non-coherent digital blocks is a potential source of logic errors in presence of SSN.

In this context, the use of on-chip monitors located at the interface between these blocks appears as an interesting possibility in order to alert when these blocks are not able to communicate due to SSN.

3.2. On-chip monitor circuit

In order to detect potential logic errors at the interface between non-coherent digital blocks, the main idea consists in permanently checking whether the power/ground voltages of the different blocks are compatible or not. Figure 6 shows the schematic of the proposed on-chip monitor circuit. It is basically composed on two inverters and an XOR gate; all biased with the power and ground lines of the driven block, i.e. V_{DD}chip2 and G_{ND}chip2. The input of one inverter is connected to the power line V_{DD}chip1 of the driving block and the input of the other to the ground line G_{ND}chip1 of the driving block.

Let us analyze the operation of this circuit. We first consider the case where the power and ground voltages of the two blocks are compatible. This means that the first block power voltage V_{DD}chip1 is higher than the threshold voltage of the second block gates $V_{TH}2$, and so this voltage is correctly interpreted as logic "1" by the on-chip monitor circuit. Similarly, the first block ground voltage G_{ND}chip1 is lower than the threshold voltage of the second block gates $V_{TH}2$, and so this voltage is correctly interpreted as logic "0" by the on-chip monitor circuit. Consequently in this situation, the XOR gate is driven by two opposite logic values and delivers logic "1". This corresponds to the "safe" situation where logic errors cannot occur at the interface between the two blocks.

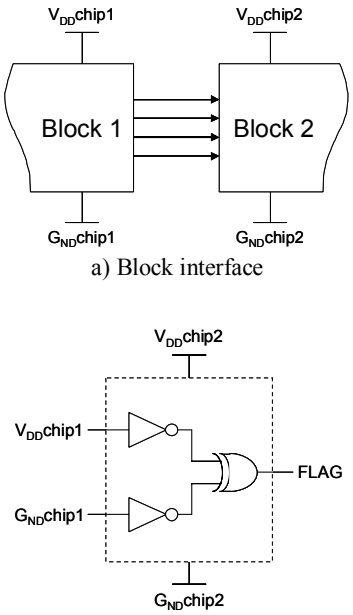


Figure 6: On-chip monitor circuit

Now in presence of SSN, it may happen that the power and ground voltages of the two blocks are not compatible. This means either that the first block power voltage V_{DD}chip1 is lower than the threshold voltage of the second block gates $V_{TH}2$, or the first block ground voltage G_{ND}chip1 is higher than the threshold voltage of the second block gates $V_{TH}2$. In the first case, the inverter driven by V_{DD}chip1 will erroneously interpret the signal as logic "0", and so the XOR gate is driven by two identical logic values and delivers logic "0". In the second case, it is the inverter driven by G_{ND}chip1 that will erroneously interpret the signal as logic "1", leading to logic "0" at the output of the XOR gate. Both these cases correspond to a risky situation where logic errors are susceptible to occur.

To summarize, the on-chip monitor circuit delivers a logic "1" when the power and ground voltages of the two blocks are compatible, indicating a correct communication between the two blocks from the logical point of view. Conversely, it delivers a logic "0" when the power and ground voltages of the two blocks are not compatible, indicating that signals between the two blocks may be logically misinterpreted, and therefore alerts on potential logic errors.

4. Validation

A number of electrical simulations have been performed to validate the proposed on-chip monitor circuitry. Results are summarized in this section.

First, static transfer characteristics have been evaluated under nominal operating conditions, i.e. a stable power supply of 1.2V. These characteristics are given in figure 8. In both cases a logic "1" is obtained for the safe situation, i.e. when V_{DD}chip1 (resp. G_{ND}chip1) is higher (resp. lower) than the logic threshold. Conversely a logic "0" is obtained when V_{DD}chip1 (resp. G_{ND}chip1) is lower (resp. higher) than the logic threshold, indicating a potential logic error at the interface between the 2 blocks since a logic "1" (resp. logic "0") delivered by the driving block will be interpreted as a logic "0" (resp. logic "1") by the driven block. This validates the operating mode of the monitor under a nominal power supply of 1.2V.

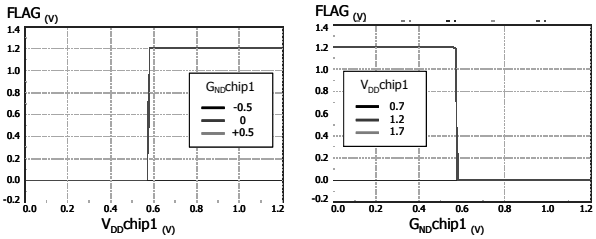


Figure 8: Transfer characteristics under nominal power supply

Then, static transfer characteristics have been evaluated under different operating conditions. Figure 9 gives the transfer characteristics for different swing conditions. It can be seen that the logic threshold is not affected by swing variations and the proposed monitor is able to operate even with a much degraded swing of 0.2V.

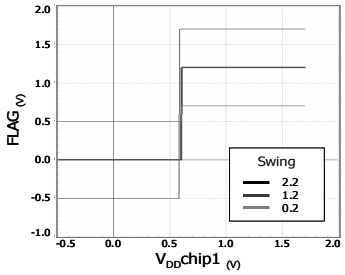


Figure 9: Transfer characteristics with swing variations

Figure 10 gives the transfer characteristics for different power/ground ranges. In all cases, we have a correct operation of the monitor with a commutation between logic "0" and logic "1" at the logic threshold, which is adjusted according to the power/ground range.

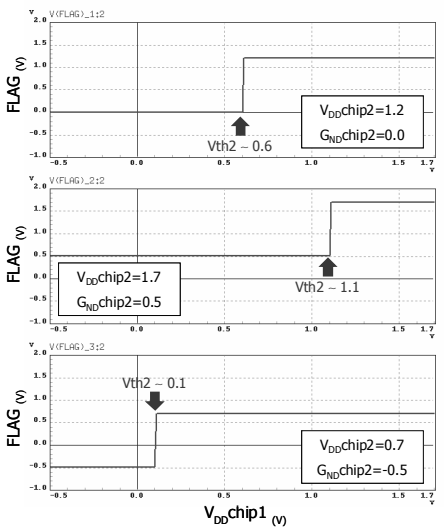


Figure 10: Transfer characteristics with power/ground range variations

Finally, transient simulations have been performed to illustrate the ability of the on-chip monitor to alert on potential logic errors at the interface between non-coherent digital blocks. The experimental setup is described in figure 11. It involves three identical logic blocks, two of them with the same internal power/ground lines and one with different power/ground lines. In presence of SSN, the two driven blocks may produce different outputs as one is coherent with the first block and therefore robust to SSN, while the other is non-coherent with the first block and therefore may be affected by logic errors.

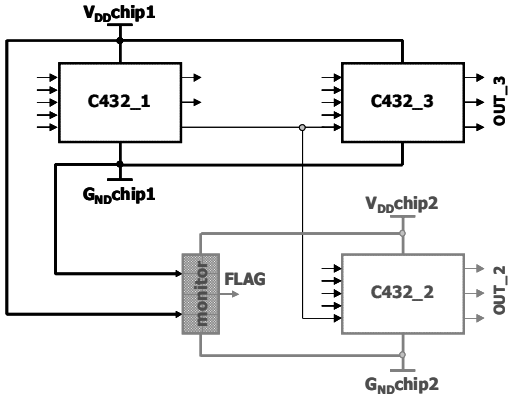


Figure 11: Experimental setup

Transient simulation results are illustrated in figures 12 and 13. Figure 12 gives the fluctuations of the power and ground voltages of the two non-coherent blocks. At a first view, these varaitions are in the same range, so one could expect that the two blocks are able to correctly communicate. However these variations are not directly correlated and may result in logic errors.

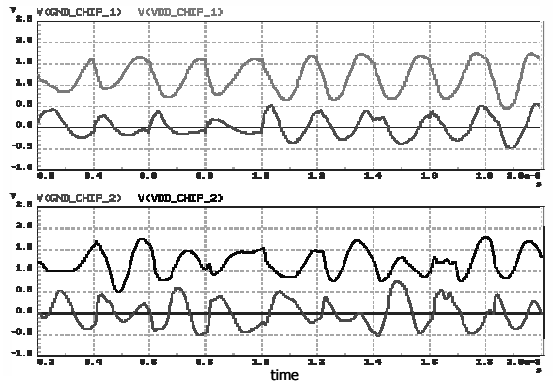


Figure 12: Power/ground voltage variations of the two non-coherent blocks

Figure 13 gives the logic interpretation of the driven blocks outputs (upper graph) together with the on-chip monitor output (lower graph). It can be seen that most of the time, the output signal of the on-chip monitor follows the V_{DD} line indicating a safe situation. But there are 3 areas where it goes to the G_{ND} line indicating a risky situation. There areas indeed correspond to areas where we can observe discrepancies between the outputs of the two driven blocks. This example validates the ability of the on-chip monitor to detect logic errors during the operation of the circuit.

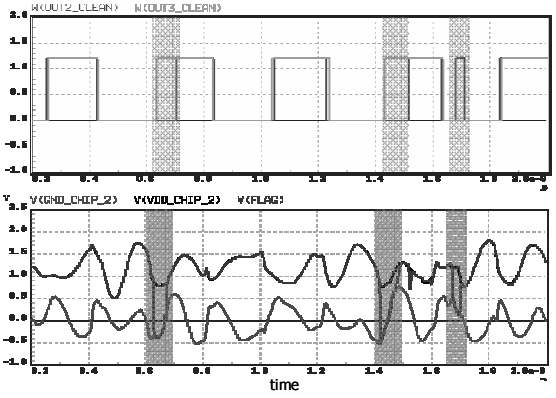


Figure 13: SSN-induced logic error detection

5. Conclusion

This paper proposes a novel on-chip monitor to detect potential logic errors in digital circuits due to the presence of SSN. Thanks to a preliminary analysis of the impact of SSN on the logic behavior of digital circuits, it is demonstrated that coherent digital blocks are quite robust to SSN, while the interface between non-coherent digital blocks is the potential source of logic errors in presence of SSN. Consequently, it is useless to integrate a monitor that checks the variations of the power and ground lines of a single coherent block. On the contrary, it is of great interest to check the variations of the power and ground lines of different non-coherent blocks in order alert that a logic error is likely to occur at the interface between these blocks. In this objective, a very simple circuitry has been developed. This monitor can therefore be integrated at low-cost. The information delivered by the monitor can then be used to develop corrective schemes.

6. References

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