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### ► **To cite this version:**

Bettina Rebaud, Marc Belleville, Christian Bernard, Michel Robert, Patrick Maurine, et al.. A Comparative Study of Variability Impact on Static Flip-Flop Timing Characteristics. ICICDT 2008 - IEEE International Conference on IC Design and Technology, Jun 2008, Grenoble, France. pp.167-170, <10.1109/ICICDT.2008.4567271>. <lirmm-00305246>

**HAL Id: lirmm-00305246**

**<https://hal-lirmm.ccsd.cnrs.fr/lirmm-00305246v1>**

Submitted on 23 Jul 2008

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# A Comparative Study of Variability Impact on Static Flip-Flop Timing Characteristics

B. Rebaud, M. Belleville, C. Bernard, M. Robert, P. Maurine, N. Azemard

**Abstract**—With the event of nanoscale technologies, new physical phenomena and technological limitations are increasing the process variability and its impact on circuit yield and performances. Like combinatory cells, the sequential cells also suffer of variations, impacting their timing characteristics. Regarding the timing behaviors, setup and hold time violation probabilities are increasing. This article aims at comparing a set of representative static flip-flop architectures used in digital designs and at studying their sensitivity to process variations. Clock-to-Q delay, hold time and setup time means and standard deviations are compared for a low power 65nm technology and commented. Then, a study of the hold/setup time failure probabilities according to the flip-flop used in a critical path is given to illustrate their robustness toward process variations.

**Index Terms**—Variability, Clock-to-Q delay, Setup Time, Hold Time, Flip-Flop

## I. INTRODUCTION

VARIABILITY in advanced processes gathers many different aspects and has to be considered at all the design stages. The main classifications that have been proposed in the literature are [1]: spatial and temporal, random and systematic, global and local, physical and environmental. Depending on which aspect of this classification is considered, different techniques to reduce the variability impact are proposed. With the decreasing transistor dimensions, the sensitivity to variations, which have always existed, increases and variability becomes one of the major challenges to address for the integrated circuits.

Previous works have described the timing issues induced by variability in a complete circuit [2-3]. Here, we look at the consequences of process variations more precisely on the timing characteristics of sequential cells. In clock-based digital designs, the use of good flip-flops (FF) is essential to reach strict timing specifications. In a traditional approach, the designers try to minimize setup and hold time violations at synthesis and place and route stages by using corner-based libraries. Several studies and very recent CAD tools [4-9] are

proposing to use statistical methods, more realistic and efficient, considering the variability issue, instead of increasing the corner margins. In this work, a statistical comparison of different flip-flops is conducted on a low power 65 nm technology to see which one presents the best robustness to process variations.

The next part will present the FFs chosen and justify these choices. Then results of simulations and interpretations will be given on the Clk-to-Q delay, setup and hold times variations. Finally, the methodology proposed in [9] is applied on critical paths with the set of chosen FFs to get a comparison in a real test case and to compute violation probabilities.

## II. FLIP FLOP CHARACTERISTICS

In this work, the term “flip-flop” designates edge-triggered sequential cell, different from the latches which are always level-triggered. A good overview is given in [10] where the most usual sequential cells are described, with their main power and timing characteristics.

In our study, the timing comparison was made on different variants of FFs based on “static master-slave latches” architectures. This structure is the most widely used in the standard cell libraries. Dynamic structures are mostly targeting high speed processors, and are not the scope of this work. Two other types of FF are also integrated to extend this comparison: the true NAND based DFF and a Race-free NAND based DFF [11].

Descriptions and schematics of the set of FFs are given below (fig.1).

### *Typical Master Slave FF based on transmission gates*

This is the simplest implementation. The transmission gates provide two balanced levels on “0” and “1”. The memory point is classically made of two cross-coupled inverters. The clock signal is buffered through two inverters.

### *Typical Master slave FF based on NAND gates*

This implementation is based on D-latches made of RS latches (Reset-Set latches). It is based on NAND gates and is consequently bigger.

### *Modified C<sup>2</sup>MOS FF #1*

This FF is based on the C<sup>2</sup>MOS design style, often used for dynamic structures. Here, the feedback makes this FF static.

Manuscript received on April the 11th. 2008

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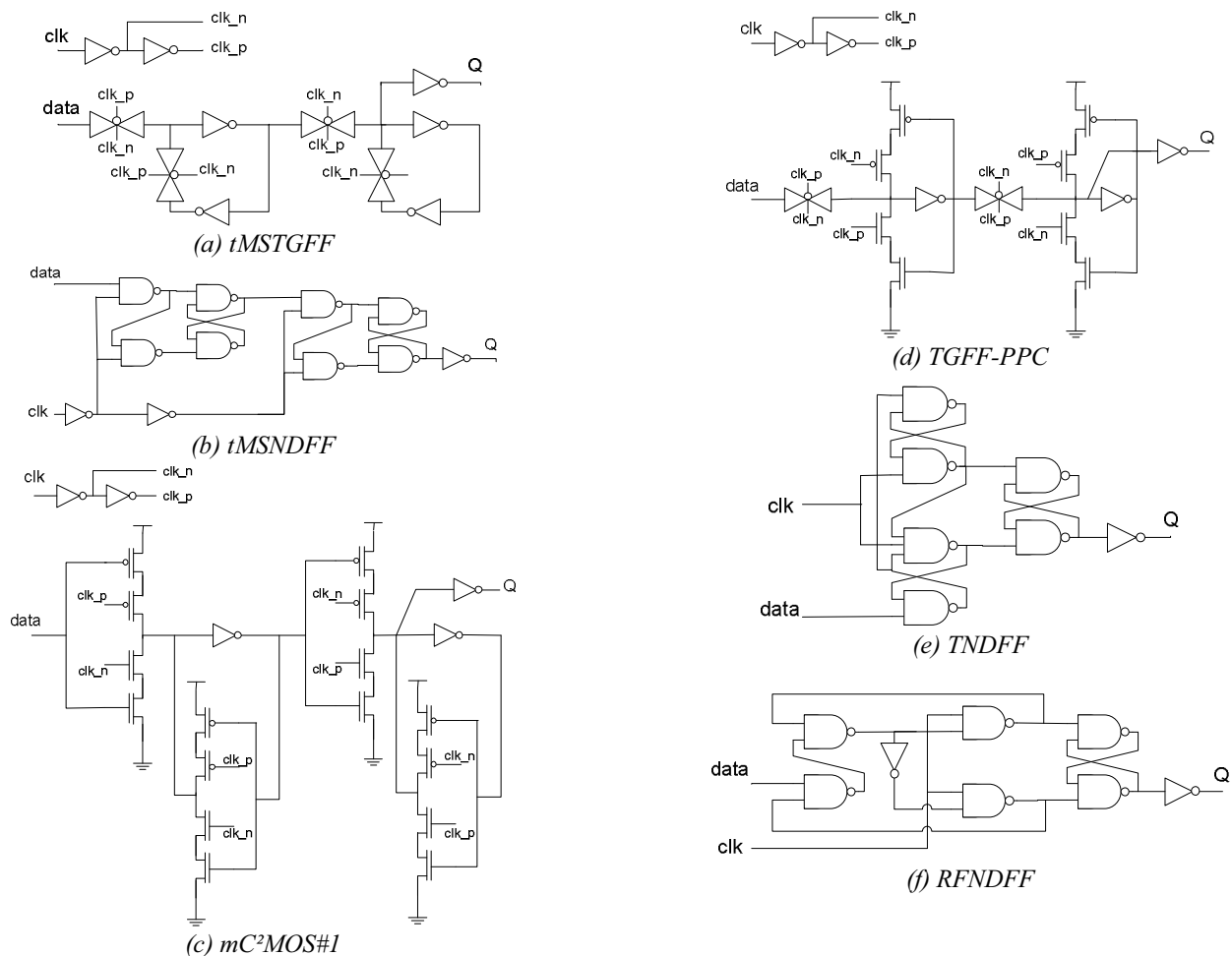


Fig. 1. Schematics of the FF chosen in the study. All are static flip-flops. (a) is the *Typical Master Slave FF based on transmission gates* (b) is the *Typical Master slave FF based on NAND gates* (c) is the *Modified C<sup>2</sup>MOS FF #1* (d) is the *PowerPC 603 FF/ TGFF* (e) is the *True NAND-based DFF* (f) is the *Race-Free NAND-based DFF*

#### Modified C<sup>2</sup>MOS FF #2

This is a variant of the preceding FF, where the C<sup>2</sup>MOS gate before the output driver is replaced by a transmission gate.

#### PowerPC 603 FF

Also called TGFF (Transmission Gate FF), this architecture is one of the fastest structures thanks to its small Clk-to-Q delay. Its small number of transistors and an efficient feedback also makes it interesting regarding the power consumption.

#### True NAND-based DFF

Made of NAND gates with RS latches structure, this FF is not like the previous master-slave latches: it does not have any transparency time with metastable state. In counterpart, it is rather large.

#### Race-Free NAND-based DFF [11]

This implementation has neither transparency time. The main memory cell remains a RS latch, but the feedbacks are different in the entrance stage. It is also a “true single phase clock” FF.

All the transistors of these FFs were sized to minimize the global area, and every transistor length is 65 nm. The minimum width that has been used in each design is 0,2  $\mu\text{m}$ .

This minimum sizing rule was adopted to highlight as much as possible the variability effects. As we can see on the schematics, each FF is ended by an output inverter sized for a same drive strength. All the simulations regarding delays and setup/hold times were made with a constant output capacitance of 40 fF.

TABLE I  
FLIP-FLOP SIZE

	# transistors	Wtot (um)
<b>tMSNDF</b>	38	82
<b>RFNDF</b>	28	52
<b>TNDF</b>	28	62
<b>mC<sup>2</sup>MOS1</b>	26	65
<b>mC<sup>2</sup>MOS2</b>	24	65
<b>TGFF-PCC</b>	22	55
<b>tMSTGFF</b>	22	55

This table represents the number of transistors in each Flip-Flop and the total width according to our sizing specifications.

Tab. I summarizes the FF chosen and their dimensions.

### III. FLIP-FLOPS TIMING SENSITIVITY TO VARIATIONS

Clk-to-Q delay, setup time and hold time are the intrinsic timing parameters which characterize the performance of a FF. Clk-to-Q delay indicates the speed of the sequential cells, setup time the amount of time needed for the data to be stable before the clock edge, hold time the amount of time needed after the clock edge. Clk-to-Q can be defined by the path from the clock to the output after the first memory point. Setup time is represented by the path beginning by the input data which leads to a stable first memory point before the new incoming data comes to compete the former signal. Hold time depends on the race between the data and the clock path. These timings are essential because they take part in the maximum frequency and functionality determination. That is why good timing elements are needed to optimize a design.

In this part, results of simulations about Clk-to-Q delay, setup time and hold time are briefly presented. The simulations made with Monte Carlo (MC) analysis to take into account process variations were performed at 1,2V, 25C. To determine the setup (respectively hold) time, the function Clk-to-Q versus setup (hold) time was plotted and the setup (hold) time value determined for an increase of 10% of the Clk-to-Q minimum delay. A curve is drawn for each MC draw. Note that in our results, we have not taken into account interdependency between the setup and the hold time [12]. Setup (resp. hold) time has been characterized with the assumption that the hold (setup) skew lasts a long time. Tab. II sums up the results obtained for Q rising slopes, and Clk fast slopes (5ps). Falling slopes are speedier because of a shorter

TABLE II  
Clk-to-Q delay, setup time, hold time distributions

	delai Clk-to-Q (ps)		
	mean	sig	dev
<b>tMSNDF</b>	296	21,9	22,20%
<b>RFNDF</b>	236	17	21,61%
<b>TNDF</b>	247,5	18,89	22,90%
<b>mC<sup>2</sup>MOS1</b>	224	16,77	22,46%
<b>mC<sup>2</sup>MOS2</b>	215	16,47	22,98%
<b>TGFF-PPC</b>	199	14,15	21,33%
<b>tMSTGFF</b>	197	14,09	21,46%

	Setup (ps)		Hold (ps)	
	mean	sig	mean	sig
<b>tMSNDF</b>	51,59	6,76	-46,84	6,65
<b>RFNDF</b>	64,14	12,27	-26	4,7
<b>TNDF</b>	59,07	6,69	11,19	4,02
<b>mC<sup>2</sup>MOS1</b>	46,34	6,22	-62,42	14,6
<b>mC<sup>2</sup>MOS2</b>	55,75	6,71	-24,78	4,05
<b>TGFF-PPC</b>	5,61	5,51	24,34	3,06
<b>tMSTGFF</b>	13,02	6,94	24,25	3,36

These tables represent the simulation results for balanced fast input slopes (5 ps) and output load of 40fF, in nominal design corner.

logic depth. The results presented in the tab. II are easily explainable for the mean values, if we consider the cell paths concerned. The Clk-to-Q delay deviation  $3\sigma/\mu$  is around 22%

for the entire set of FFs, which corresponds to variations on a path of about 4 cells. Considering the sigma deviation, we can see that *RFNDF* has the worst setup time variation: this can be explained by the fact that the first memory point is not decorrelated from the data entrance, which is in direct competition with the feedback in the NAND gate. This is not the case for the other FFs. (For *TNDF*, the memory point for rise slope is not in competition with the data). *mC<sup>2</sup>MOS1* has the worst hold time variation; transmission gates are better than C<sup>2</sup>MOS gates in hold definition regarding clock entrance. Other results show that Clk slow input slopes slightly increase the variability of the Clk-to-Q delays, except for *TNDF* and *RFNDF*. This can be explained by the fact that these FFs are the only ones which have no clock buffering (stabilizing and straightening the slopes) and consequently exhibit disorderly behaviours. For the others, they follow the trend that slower slope timings increase delay variations [13]. With this information, we can predict that *tMSNDF* (worst Clk-to-Q) and *RFNDF* (worst setup time variation) will be one of the worst FFs in critical paths. On the other hand, TGFF-PPC will be among the worst FF in term of hold violation (fast Clk-to-Q delay and bad hold time). These figures point out the fact that even if variability deeply impacts timing characteristics, mean values due to FF structures remain significant in the violation probability calculation.

### IV. VIOLATION PROBABILITIES ON A CRITICAL PATH

To get an exhaustive comparison of these FF in a functional environment, we were considered a real case. Data and clock paths were extracted from a multiplier design at its place and route level, and then we replaced the initial FF by those of this study.

To get the efficiency of one FF, we compute the hold/setup time violation probabilities thanks to the methodology described in [9]. This method allows us to take into account Clk-to-Q delay variations in the same time than setup/hold time variations, and then use all data available in part III. It is based on a SSTA (Statistical Static Timing Analysis) [4-9] for the combinatory paths, mixed with MC timing data coming from the sequential cells. Fig. 2 illustrates the method.

We took the longest and the shortest timing path of our design to compute the setup (hold) time violations. We recall that probabilities can be found thanks to the equations given below :

$$Pv_{setup} = \Pr(P - d_{path} + d_{clock} < d_{setup})$$

$$Pv_{hold} = \Pr(d_{path} - d_{clock} < d_{hold})$$

with  $P$  the period,  $d_{path}$  the delay distribution function of the data path,  $d_{clock}$  the delay distribution function of the clock,  $d_{setup}/d_{hold}$  the distribution function of the setup/hold time.

The worst design case was taken at 1,1V, 125C for the long path (setup) and the best design case at 1,3V, -40 C for the short path (hold). Regarding the setup and hold time variation definitions, the same design corners were taken for all the simulations, even if it is hard to predict common worst cases for all the FFs [9]. However, these differences remain small

and the comparison can be relevant.

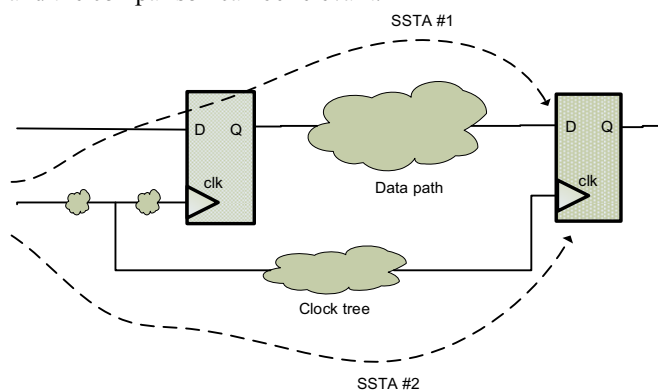


Fig. 2 : Two SSTA are performed : one on the data path, the other on the clock path. The information obtained allows to calculate the setup/hold time violation probability on the second D-flip-flop.

Fig. 3 presents for each FF of this study the setup time violation probabilities of a critical path. These results show few differences between the variations of each case, suggesting that intrinsic setup time FF deviations do not play a major role once integrated into the whole path analysis. On the other hand, the setup time and Clk-to-Q means are major parameters. The period difference between the worst and the best flip-flop is about 0,2 ns, equivalent to a performance difference of about 7%, which can be determining for high speed chips.

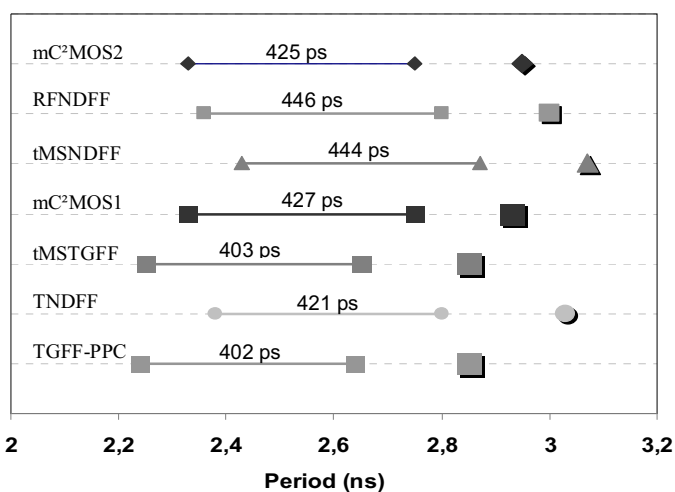


Fig. 3 : This graph represents the period range corresponding to a setup time violation probability between 90% and 10%. The single points refer to a violation probability of 0.5%.

*TGFF-PPC* and *tMSTGFF* are the best flip-flops in this case, benefiting of the fast Clk-to-Q delay in the data path, combined with a low setup time with weak variations.

For the hold time violation probabilities, the only flip-flops with no negligible probabilities are the *tMSTGFF* (0,29%) and the *TGFF-PPC* (0,26%). These two FFs have similar Clk-to-Q paths and data paths, made of transmission gates and inverters. Indeed, hold time depends on clock race until the beginning of the second memory point versus data race until this same point. The other flip-flop hold time violations are close to 0.

Tab. III presents the hold time failure probabilities found when forcing the input slopes of the data and the clock to a very slow slope (about 240 ps, 20%-80%) to underline the differences between FFs, but in keeping the same data and clock delay distributions. We can find that *tMSTGFF* and *TGFF-PPC* are still the worst flip-flops for hold time violations, as predicted in part III. The next one is *mC<sup>2</sup>MOS2* which is very similar to the previous FFs, but with a longer data path, which decreases the violation probability.

TABLE III  
Hold time violation probabilities (%)

mC <sup>2</sup> MOS2	RFN DFF	tMSN DFF	mC <sup>2</sup> MOS1	tMS TGFF	TN DFF	TGFF PPC
40,49	17,83	0,82	0,12	79,5	0,02	74,66

Hold violation probabilities according to the Flip-Flop used with very slow input data and clock slopes.

## V. CONCLUSION

This article presents a comparative study of several master-slave flip-flops, taking into account process variability. Their performances are evaluated by looking at their timing characteristics like Clock-to-Q, Setup and Hold times. Simulations regarding these aspects and a functional study on real paths allow to better classify their performances. It is clearly shown that the optimal FF is not the same for long and short paths: a good setup time FF can have the worst performances in hold time.

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